13. The introduction of synchronous DRAM offered a potentially promising solution to the memory bottleneck. Yet the success of synchronous DRAM depended importantly upon the ability of the computer industry to adopt standards governing the design and implementation of synchronous DRAM.

JEDEC

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18. The JEDEC Manual provides that all JEDEC meetings "shall comply with the current edition of EIA Legal Guides." These Legal Guides – which are explicitly "incorporated … by reference" into JEDEC's own governing rules, and currently are posted on JEDEC's own website under the heading "Manuals" – provide that standardization programs must be "conducted under strict policies designed to promote and stimulate our free enterprise system and to make sure that laws for maintaining and preserving this system are vigorously followed."

19. The EIA/JEDEC Legal Guides establish a "basic rule" that standardization programs conducted by the organization "shall not be proposed for or indirectly result in … restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market."

20. Consistent with its commitment to promoting unfettered competition, at all times relevant herein JEDEC also has maintained a commitment to avoid, where possible, the incorporation of patented technologies into its published standards, or at a minimum to ensure that such technologies, if incorporated, will be available to be licensed on royalty-free or otherwise reasonable and non-discriminatory terms. Toward this end, JEDEC has implemented

required that no standard be drafted to include "patented items" – or "items and processes for which a patent has been applied" – absent both

(1) a well-supported technical justification for inclusion of the patented item; and

(2) express written assurance from the patent holder that a license to the patented technology will be made available either "without compensation" or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination."

23. The JEDEC Manual, at least since October 1993, has expressly provided that the disclosure and licensing obligations discussed above apply "with equal force" when JEDEC members, subsequent to the adoption of a standard, discover new information about existing patent rights – or otherwise obtain new patent rights – involving that standard. In such situations, the JEDEC member must make the same disclosures and provide the same assurances as would be required if the member knew of such patent rights prior to adoption of the relevant standard.

24. Fairly interpreted, the policies, procedures, and practices existing within JEDEC throughout all times relevant herein imposed upon JEDEC members certain basic duties with regard to the disclosure of relevant patent-related information and the licensing of relevant patent rights:

a. First, to the extent any JEDEC member knew or believed that it possessed patents or pending patent applications that might involve the standard-setting work that JEDEC was undertaking, the member was required to disclose the existence of the relevant patents or patent applications and to identify the aspect of JEDEC's work to which they related.

b. Second, in the event that technologies covered by a member's known patents or patent applications were proposed for inclusion in a JEDEC standard, the member was required to state whether the technology would be made available either "without compensation" or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination." Absent the member's agreement to one of these two conditions, the JEDEC rules would not allow the technology to be incorporated into a proposed standard.

JEDEC Work Involving SDRAM Standards

25. The JEDEC committee responsible for overseeing the development of standards relating to memory devices is known as the JC-42 Committee on Solid State Memories ("JC-42"), which has several subcommittees, one of which is particularly relevant for purposes of the instant

complaint: the JC-42.3 Subcommittee on RAM Devices ("JC-42.3").

26. Beginning in or around 1990, JC-42.3 commenced work on standards relating to the design and architecture of synchronous DRAM, referred to within JC-42.3 as "SDRAM." JEDEC members involved in the SDRAM-related work of JC-42.3 have over time included virtually all leading memory designers, manufacturers, and users, whether based in the U.S. or abroad.

27. During the 1990s, JEDEC issued several SDRAM-related standards, the first of which was published in November 1993 and was identified as Release 4 of the 21-C Standard. Subsequent releases of the 21-C Standard followed after that, only small portions of which related to SDRAM, as opposed to other memory-related technologies. In August 1999, however, JEDEC published a substantially augmented SDRAM standard – Release 9 of the 21-C Standard – which introduced a second generation of SDRAM. This second-generation standard became known as "double data rate," or "DDR," SDRAM.

28. Although the second-generation SDRAM standard was not issued until 1999, the work that culminated in that standard commenced, at the very latest, shortly after the first-generation SDRAM standard was adopted in 1993. Indeed, it may have commenced even earlier than that, inasmuch as at least one of the technological features initially considered (but ultimately rejected) for the first-generation SDRAM standard was later adopted in the second-generation standard. In addition, most, if not all, of the technologies encompassed in the first SDRAM standard were carried forward in the second-generation standard as well.

29. The process through which JEDEC adopted and published these standards proceeded essentially as follows:

    a. At regularly scheduled meetings of the JC-42.3 Subcommittee, which typically occurred on a quarterly basis – as well as affiliated committee and task group meetings, which were scheduled as needed – members were allowed to make presentations concerning specific concepts or technologies they proposed for inclusion in a standard under development.

    b. Such presentations generally were accompanied by written materials, which, in addition to being shared with all members present at the meeting, were reproduced and attached to the official meeting minutes.

    c. Before any proposal could be considered for adoption, it was necessary that it be presented a second time at a later subcommittee meeting.

    d. At that point, a member could move that the proposal be presented to the

subcommittee membership for approval through a formal balloting process, pursuant to which written ballots were distributed and received by mail.

e. Votes were then tabulated at the subsequent meeting of the subcommittee, at which time members voting "No" were required to explain their reasons for opposing the proposal.

f. Technically, a two-thirds majority was required, but in practice proposals rarely passed without a consensus of all voting members.

g. Individual proposals, once approved by JC-42.3, were often held at the subcommittee level until a complete package of related proposals was ready to be forwarded to the Council for final ratification.

30. JEDEC's – specifically, the JC-42.3 Subcommittee's – work on SDRAM standards continues today, and a third-generation SDRAM standard, known as "DDR II," is expected to be completed later this year.

Rambus and Its Proprietary RDRAM Technology

31. Rambus was founded in 1990 by two electrical engineers, Mark Horowitz and Michael Farmwald, who together developed their own, proprietary synchronous DRAM architecture. They named the new architecture Rambus DRAM, or simply "RDRAM," and contributed the technology to the new corporation upon its formation.

32. RDRAM, as originally designed, differed from traditional DRAM architectures in several ways, including but not limited to the following:

a. First, the RDRAM architecture specified the use of many fewer bus lines than was common in traditional DRAM designs. Thus, RDRAM was said to be a "narrow-bus" architecture. By comparison to RDRAM, traditional DRAM incorporated what was referred to as a "wide-bus" or "broad-bus" design.

b. Second, in the RDRAM architecture, each bus line was capable of carrying three types of information essential to memory functionality: (1) data; (2) "address" information, specifying the location where needed data could be found, or should be placed, in memory; and (3) "control" information, specifying, among other things, the relevant command (*e.g.*, whether the computer should "read" data from memory or "write" new data to memory). By comparison, in traditional DRAM architectures, each bus line was generally dedicated to carrying only one of these three types of information. Thus,

the RDRAM bus was sometimes said to be "multiplexed" or "triply multiplexed."

c. Third, rather than transmitting data, address, and control information separately, as was common in a traditional DRAM architecture, RDRAM transmitted such information together in groupings, called "packets." For this reason, RDRAM is also sometimes referred to as a "packetized" system.

33. Though Rambus has designed, and obtained patents on, various DRAM-related technological concepts or features, Rambus does not itself manufacture such technologies, choosing instead to license its designs for a fee to downstream memory manufacturers. Beginning in the early 1990s and continuing through the present, Rambus has sought to market and license its proprietary RDRAM technology to manufacturers of computer memory and related products, including a number of companies holding membership in JEDEC.

Rambus's '898 Patent Application and Its Progeny

34. On April 18, 1990, Rambus filed its first DRAM-related patent application with the United urportting to escri be(Rambus's DRAM-relatedinvtentiors. In, additio,h theo market an297e ii s,r,euPpte

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earlier-filed patent application are sometimes said to be within the same “family” as the

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statements, in a manner that affected the timing, but not the core substance, of Rambus's scheme. For instance, although Rambus's '898 application was pending at the time these statements were written, not until 1996 was Rambus – through a separate application claiming priority back to the '898 application – able to obtain its first patent broad enough to arguably cover aspects of the wide-bus DRAM architecture incorporated into the JEDEC standards. In addition, Rambus ultimately elected to wait until late 1999, after DRAM manufacturers and their customers had become "locked in" to the JEDEC standards, before seeking to enforce its patents against memory manufacturers producing JEDEC-compliant SDRAM.

46. Aside from such timing issues, the Rambus business plans quoted in Paragraphs 43 and 44 set forth quite accurately the basic scheme upon which the company would embark – that is, a scheme whereby Rambus would actively seek to perfect patent rights covering technologies that were the subject of an ongoing, industry-wide standardization process, in which Rambus itself was a regular participant, without disclosing the existence of such patent rights (or the pertinent patent applications) to other participants, many of whom, by producing products compliant with the standards, would later be charged with infringing Rambus's patents.

Implementation of Rambus's Scheme

47. During the course of its participation in JEDEC, from late 1991 through mid-1996, Rambus observed multiple presentations regarding technologies, proposed for (and later included in) JEDEC's SDRAM standards, that Rambus either (1) knew or believed to be covered by claims contained in its then-pending patent applications, or (2) believed could be covered through amendments to those applications expanding the scope of the patent claims while adding no new matter to the underlying technical specification.

48. That is, at all times relevant herein, Rambus believed that a number of the specific technologies that were proposed for, and later incorporated in, the relevant JEDEC standards were encompassed by the 62-page technical specification and 15 related drawings common to Rambus's '898 application (filed in 1990) and the numerous amended, divisional, and continuation applications that stemmed from temmed from temmed from muTo8t0 T spbus's patentu 199c 0.2 h

perfect Rambus's patent rights over such technologies. In executing these steps, Rambus placed heavy reliance upon two individuals: Richard Crisp, Rambus's designated representative to the JC-42.3 Subcommittee, and Lester Vincent, an attorney with the law firm of Blakely, Sokoloff, Taylor & Zafman, who served as Rambus's outside patent counsel.

50. Richard Crisp, an electrical engineer, joined Rambus in 1991. He attended his first JC-42.3 meeting in February 1992 and continued to attend such meetings regularly through December 1995. (In addition to Crisp, David Mooring, at that time Rambus's vice president for business development, and Billy Garrett, another Rambus engineer, sometimes attended JC-42.3 meetings.) In May 1992, Crisp became Rambus's designated representative to JC-42.3. As such, he personally received any information, such as meeting minutes and ballot forms, that JEDEC furnished to Rambus by mail.

51. Throughout the duration of Crisp's participation in the JC-42.3 Subcommittee, it was his customary practice to send comprehensive reports to his superiors and others within Rambus describing in detail the technologies that were being proposed for inclusion in the JEDEC SDRAM standards. Typically, these reports were communicated via e-mails authored and sent while the JC-42.3 meetings were still in progress.

52. Lester Vincent and his law firm, Blakely, Sokoloff, were retained as patent counsel by Rambus in the summer of 1991, at which time Vincent assumed primary responsibility for prosecuting Rambus's '898 application before the PTO. For several years thereafter, Vincent and his colleagues assisted Rambus with its DRAM-related patent strategy, providing frequent advice to Rambus on patent-related issues and assuming primary responsibility for drafting, filing, and prosecuting the various continuation and divisional patent applications that stemmed from the '898 application.

53. In late March 1992, Vincent met with Crisp and Allen Roberts, the Rambus vice president with responsibility for patents, to discuss, among other things, Rambus's participation in JEDEC. At this meeting, Vincent, Crisp, and Roberts discussed whether Rambus, having joined JEDEC and participated in JEDEC meetings, was at risk of forfeiting – on grounds of equitable estoppel – its rights to enforce future patents covering aspects of the JEDEC standards. Vincent advised that there could be an equitable estoppel problem if Rambus were to convey to other JEDEC

54. Throughout its four and one-half years of participation in the JC-42.3 Subcommittee, Rambus engaged in a continuous pattern of deceptive, bad-faith conduct. Rambus's bad-faith participation in JEDEC, although evidenced in other ways as well, was perhaps best exemplified in the coordinated activities of Crisp and Vincent. During his four-year tenure as Rambus's representative to JC-42.3, Crisp observed multiple presentations relating to technologies Rambus believed were covered – or, through amendment, could be covered – by pending Rambus patent applications. In fact, in a number of instances, Crisp, while participating in JC-42.3 meetings, sent e-mails back to Rambus headquarters expressing a belief that Rambus had pending applications covering certain technologies being discussed in such meetings, or otherwise suggesting that Rambus's pending patent applications be reviewed, and if necessary amended, to ensure they covered such technologies. On several occasions, Crisp – based in part on information learned through attending JC-42.3 meetings – developed specific proposals for amending Rambus's pending patent claims and communicated such proposals directly (or via a Rambus colleague) to Vincent. Likewise, in some cases, Vincent sent copies of draft amendments to Rambus's patent applications to Crisp, among others, soliciting his input before finalizing such amendments. Plainly, in light of Rambus's failures to disclose pertinent patent-related information to JEDEC, the activities described in this paragraph constituted bad faith.

55. As underscored elsewhere in this complaint, Rambus never disclosed to JEDEC the fact that, throughout the duration of its membership in the organization, Rambus had on file with the PTO, and was actively prosecuting, patent applications that, in its view, either covered or could easily be amended to cover elements of the existing and future SDRAM standards.

Technologies Impacted by Rambus's Scheme

56. Among other specific technologies adopted or proposed for inclusion in the SDRAM standards during the period of Rambus's participation in JEDEC, which Rambus believed were covered by its then-pending patent applications or could be covered through amendments to such applications, were the following: (1) programmable CAS latency; (2) programmable burst length; (3) on-chip PLL/DLL; and (4) dual-edge clock.

57. Column address strobe (or "CAS") latency refers to the amount of time it takes for the memory to release data after receiving a signal, known as the column address strobe, in connection with a read request from the CPU. The technology known as programmable CAS latency allows memory chips to be programmed such that this aspect of the memory's operation can be

known as programmable burst length allows memory chips to be programmed to adjust this aspect of the memory's operation in order to facilitate compatibility with a variety of different computer environments.

59. From December 1991 through May 1992, Crisp and other Rambus representatives observed multiple JC-42.3 presentations pertaining to programmable CAS latency and programmable burst length, both of which were proposed to be incorporated in the first JEDEC SDRAM standard. Soon thereafter, in the summer of 1992, Crisp received, and voted upon, a ballot calling for inclusion of both technologies in the standard. This was the only time that Crisp voted on a JEDEC ballot, and he voted "No," for technical reasons that he was called upon to, and did, explain, but without saying anything to suggest that Rambus might possess relevant intellectual property.

60. At the time of these events, Crisp and others within Rambus believed that both programmable CAS latency and programmable burst length were encompassed by the inventions set forth in the specification and drawings of the '898 application and related applications that were then pending at the PTO, and that Rambus – by amending the claims in those pending applications – had the ability to perfect patent rights covering such technologies as used in the SDRAM standard. Indeed, beginning in May 1992, Crisp, Roberts, and other Rambus representatives began a series of consultations with Vincent for the purpose of drafting new claims, linked to the '898 application, that would cover use of certain technologies in the wide-bus architecture adopted by the SDRAM standard. Programmable CAS latency and programmable burst length were both among the technologies discussed for inclusion in these new wide-bus claims.

61. In March 1993, a Rambus representative attended the JC-42.3 meeting at which both programmable CAS latency and programmable burst length were approved for inclusion in the

been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed pending patent applications purporting to cover – or that could be amended to cover – programmable CAS latency and burst length technologies in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

63. Phase lock loop ("PLL") and delay lock loop ("DLL") are closely related technologies, both of which are used to synchronize the internal clock that governs operations within a memory chip and the system clock that regulates the timing of other system functions. The former, PLL, synchronizes the two clocks by adjusting the internal clock's frequency to match the system clock's frequency, whereas the latter, DLL, achieves synchronization by delaying the internal clock. "On-chip" PLL/DLL refers to the approach of placing these technologies on the memory chip itself, as opposed to the alternative approach of placing these technologies on, for instance, the memory module or the motherboard – the latter being known as "off-chip" PLL/DLL.

64. Beginning in September 1994, Crisp observed presentations and other work in the JC-42.3 Subcommittee involving proposals to include on-chip PLL in the second generation of the SDRAM standard. At that time, Crisp and others within Rambus believed that on-chip PLL was encompassed by the inventions set forth in the specification and drawings of the '898 application and related applications then pending at the PTO, and they had already discussed with Vincent their desire to perfect patent rights covering use of this technology in SDRAMs. Indeed, in June of 1993 Vincent's law firm filed, on Rambus's behalf, an amendment to a pending patent application – Application No. 07/847,692 – adding claims that, on their face, covered use of on-chip PLL/DLL technology in either a wide-bus or narrow-bus DRAM architecture. From June 1993 through the present, Rambus has continued its efforts to perfect patent rights covering use of on-chip DLL technology as ultimately incorporated in the second-generation SDRAM standard published in August 1999.

65. The design objectives served by inclusion of on-chip DLL technology in the second-generation JEDEC standard likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed pending patent applications purportedly covering – or that could be amended to cover – on-chip PLL/DLL technologies in a wide-bus synchronous DRAM architecture,

such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

66. Dual-edge clock is a technology that permits information to be transmitted between the CPU and memory twice with every cycle of the system clock, thereby doubling the rate at which information is transmitted compared to the first generation of SDRAM, which incorporated a "single-edge clock" and hence permitted information to be transmitted only once per clock cycle.

67. Between December 1991 and April 1992, Crisp and other Rambus representatives attended JC-42.3 meetings at which they observed presentations and other work involving dual-edge clock technology and a closely related technology known as "toggle-mode." Ultimately, the JC-42.3 Subcommittee decided not to incorporate these technologies into the first-generation SDRAM standard. At the time this decision was reached, however, certain JC-42.3 members expressed the view that such technologies would be appropriate for reconsideration in connection with the next generation of SDRAM. Dual-edge clock technology was again discussed by the JC-42.3 Subcommittee in May 1995. Soon thereafter, in October 1995, a survey ballot relating in part to dual-edge clock technology was distributed to JC-42.3 members, and the same ballot was later discussed at a JC-42.3 meeting in December 1995. A formal proposal to include dual-edge clock technology in the second-generation SDRAM standard was made at a JC-42.3 Subcommittee meeting in March 1996. Following Rambus's withdrawal from JEDEC in June 1996, dual-edge clock technology was the subject of further presentations, and the technology ultimately was incorporated into the second-generation SDRAM standard.

68. In September 1994, Vincent's law firm, on behalf of Rambus, filed an amendment to Rambus's Patent Application No. 08/222,646, adding dual-edge clock claims that were not limited to a narrow-bus RDRAM design, but rather purported to cover use of dual-edge clock technology in any synchronous DRAM architecture, including a wide-bus architecture of the sort that was the focus of JEDEC's SDRAM standards. This application, as amended to include dual-edge clock claims, issued as U.S. Patent No. 5,513,327 (hereinafter, "the '327 patent") in April 1996, while Rambus was still a member of JEDEC. From September 1994 through the present, Rambus has continued its efforts to perfect patent rights covering use of dual-edge clock technology as used in a wide-bus synchronous DRAM architecture.

69. The design objectives served by inclusion of dual-edge clock technology in the second-generation SDRAM standard likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3

Subcommittee that it possessed patents or pending patent applications arguably covering (or that, with respect the applications, could be amended to cover) dual-edge clock technology in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

Rambus's Limited and Misleading Disclosures to JEDEC

70. At no time during its involvement in JEDEC did Rambus ever disclose to the organization the fact that it possessed an issued patent – the '327 patent discussed in Paragraph 68 above – that purported to cover use of a specific technology proposed for inclusion in the JEDEC SDRAM standards. Nor did Rambus ever disclose to JEDEC that it had on file with the PTO various pending patent applications that purported to cover, or could be amended to cover, a number of other technologies included or proposed for inclusion in the JEDEC SDRAM standards. More generally, Rambus never said or did anything to alert JEDEC to (1) Rambus's belief that it could claim rights to certain technological features not only when used in the context of its proprietary, narrow-bus, RDRAM designs, but also when used in the traditional wide-bus architecture that was the focus of JEDEC's SDRAM standard-setting activities; or (2) the fact that Rambus, while a member of JEDEC, was actively working to perfect such patent rights.

71. On the contrary, Rambus's very participation in JEDEC, coupled with its failure to make required patent-related disclosures, conveyed a materially false and misleading impression – namely, that JEDEC, by incorporating into its SDRAM standards technologies openly discussed and considered during Rambus's tenure in the organization, was not at risk of adopting standards that Rambus could later claim to infringe upon its patents.

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additional applications that Rambus believed could be amended to cover such technologies without the addition of any new matter. Rambus never disclosed these critical facts to JEDEC.

Rambus's Withdrawal from JEDEC

81. In December 1995, Vincent learned of, and discussed with Anthony Diepenbrock, an in-house Rambus attorney, the Commission's proposed consent order in *In re Dell Computer Corporation*, which involved allegations of anticompetitive unilateral conduct occurring within the context of an industry-wide standard-setting organization. In January 1996, Vincent advised Rambus that it should terminate "further participation in any standards body," including JEDEC.

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alert JEDEC to Rambus's belief that it could claim rights to certain technological features not only when used in the context of its proprietary, narrow-bus, RDRAM designs, but also when used in the traditional wide-bus architecture that was the focus of JEDEC's SDRAM standard-setting activities.

87. But this was not all the June 1996 letter failed to disclose. As of June 1996, when Rambus submitted its formal withdrawal letter to JEDEC, the company actually possessed 24 issued patents, not 23. That is, one – but only one – of Rambus's issued patents was omitted from the list attached to the June 1996 withdrawal letter. The omitted patent was Rambus's '327 patent, which issued in April 1996, two months before Rambus's withdrawal from JEDEC. As discussed in Paragraph 68 above, the '327 patent contained claims purporting to cover use of dual-edge clock technology in any synchronous DRAM architecture. As such, it was the only patent actually obtained by Rambus while a member of JEDEC that arguably covered use of a specific technology included, or considered for inclusion, in JEDEC's wide-bus SDRAM standards.

88. Even after withdrawing from JEDEC, Crisp and others within Rambus continued to closely monitor JEDEC's ongoing work on SDRAM standards, including work involving specific technologies on which Rambus sought to perfect patent rights.

Industry Adoption of the JEDEC Standards

89. In the years following the issuance of JEDEC's first SDRAM standard in November 1993, DRAM manufacturers and their customers began designing, testing, and ultimately manufacturing memory and memory-related products incorporating, or complying with, JEDEC's standardized SDRAM designs. By 1995, JEDEC-compliant SDRAM had begun to replace older-generation, asynchronous DRAM architectures. Thereafter, the shift to the more modern SDRAM technology progressed rapidly. By 1998, total worldwide sales of JEDEC-compliant SDRAM, on a revenue basis, exceeded sales of asynchronous memory. And by 1999, JEDEC-compliant SDRAM had largely replaced asynchronous DRAM in virtually all relevant uses. Toward the end of this period – roughly 1999 to 2000 – some DRAM manufacturers and their customers also began using RDRAM, but only in very limited end uses, accounting for a relatively small portion (*i.e.*, in the range of 5%) of overall DRAM production.

90. Leading up to and following the issuance of JEDEC's second-generation SDRAM standard – or DDR SDRAM – in August 1999, DRAM manufacturers and their customers began designing, testing, and (to a limited extent) producing memory and memory-related products incorporating, or complying with, the DDR SDRAM standard. By 2000, DDR SDRAM was beginning to be manufactured in increasing volumes. This trend continued during 2001, and a number of DRAM manufacturers and their customers began to replace first-generation

SDRAM and RDRAM with DDR SDRAM for certain high-end uses. Current projections indicate that total sales of DDR SDRAM, on a revenue basis, may account for as large as 40% of all DRAM produced worldwide in 2002, and by 2004 this figure is expected to exceed 50%.

Success of Rambus's Scheme

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96. With the signing of the Hitachi license, combined with the seven additional licenses discussed above, Rambus had succeeded in obtaining licenses covering roughly 50% of total worldwide production of synchronous DRAM technology. At current market prices for SDRAM, such licenses entitle Rambus to royalties in the range of $50-100 million per year, a number that could increase significantly in the event Rambus were to prevail in the ongoing litigation and secure licenses from the remaining manufacturers of SDRAMs. Indeed, under such circumstances, Rambus's SDRAM-related patent rights could allow Rambus to extract royalty payments well in excess of a billion dollars from the DRAM industry over the life of the patents.

97. In August 2000, Rambus filed suit against another DRAM manufacturer – Infineon – in federal district court in Virginia, accusing Infineon of patent infringement. Infineon later asserted various affirmative defenses and counterclaims. In April 2001, the case proceeded to trial, resulting in a jury finding of fraud against Rambus relating to its involvement in the standard-setting activities of JC-42.3 and a legal ruling that Rambus's patents were not infringed by

101. Upon information and belief, Rambus also possesses additional patents and patent applications, some claiming priority back to the '898 application, that it has not yet sought, but could in the future seek, to enforce against memory manufacturers producing JEDEC-compliant SDRAM, absent issuance of the relief requested below.

102. In addition to the foregoing, Rambus is involved in other litigation in various foreign countries relating to foreign patents that cover, or purport to cover, many of the same DRAM-related technologies that are at issue in the U.S. litigation.

103. Notably, while Rambus has licenses covering roughly 50% of the synchronous DRAM industry, Rambus asserts in litigation that all or virtually all synchronous DRAM produced worldwide incorporates Rambus technology and that those synchronous DRAM manufacturers that are not paying royalties to Rambus are liable in damages. In addition to facing the threat of potential damages, those companies that have chosen to litigate against Rambus have been forced to incur substantial litigation costs, reaching into the millions, if not tens of millions, of dollars. Unless they prevail against Rambus in litigation, such companies also face the prospect of being denied licenses to Rambus's patents, or otherwise being required to pay royalties significantly in excess of the amounts paid by the memory manufacturers that acquiesced to Rambus's licensing demands without resort to litigation.

104. Rambus also has licensed companies, such as Intel, that do not produce memory chips but do produce related computer components – in Intel's case, chipsets – that are designed to be compatible with synchronous DRAMs.

Inability of DRAM Industry to Work Around Rambus's Patents

105. Given the extensive degree to which the DRAM industry has become locked in to the JEDEC SDRAM standards, it is not economically feasible for the industry to attempt to alter or work around the JEDEC standards in order to avoid payment of royalties to Rambus. Any such effort would face innumerable practical and economic impediments, including but not limited to the out-of-pocket costs associated with redesigning, validating, and qualifying SDRAM products to conform with a revised set of standards. On top of this, such manufacturers could be forced to absorb potentially massive revenue losses if, as a result of modifying the JEDEC standards, their introduction of new products were delayed.

106. Agreeing upon revised SDRAM standards could in itself be a very costly and time-consuming process. Indeed, it is unclear whether the industry would be able to reach any such consensus, given complications inherent in the current market environment, including the fact that some DRAM manufacturers have acquiesced to Rambus's licensing demands while others have not.

107. Added to these complications is the fact that purchasers and other users of JEDEC-compliant SDRAM technology – including manufacturers of computers, chipsets, graphics cards, and

order to address or solve issues, or problems, that arise in the course of developing such chips. The alternative technologies available to address a given technical issue arising in the course of synchronous DRAM design together may comprise a separate, well-defined product market. At least four such markets are relevant for purposes of the instant complaint, including the following:

a. The market for technologies used to specify the length of time – or "latency" period – between the memory's receipt of a read request and its release of data corresponding with the request (hereinafter, the "latency technology market"). This market includes programmable CAS latency and any alternative technologies that may be economically viable substitutes for the use of programmable CAS latency in synchronous DRAM design.

market encompassing the group of complementary technologies and their close substitutes. Thus, in addition, or in the alternative, to the four product markets identified above, there is a fifth well-defined product market that is relevant for purposes of this complaint – namely, a market comprising, collectively, all technologies falling within any one of these narrower markets (hereinafter, the "synchronous DRAM technology market").

Geographic Scope of Relevant Product Markets

119. The foregoing conduct by Rambus, during and after its involvement in JEDEC's JC-42.3 Subcommittee, has materially caused or threatened to cause substantial harm to competition and will, in the future, materially cause or threaten to cause further substantial injury to competition and consumers, absent the issuance of appropriate relief in the manner set forth below.

120. The threatened or actual anticompetitive effects of Rambus's conduct include but are not limited to the following:

a. increased royalties (or other payments) associated with the manufacture, sale, or use of synchronous DRAM technology;

b. increases in the price, and/or reductions in the use or output, of synchronous DRAM chips, as well as products incorporating or using synchronous DRAMs or related technology;

c. decreased incentives, on the part of memory manufacturers, to produce memory using synchronous DRAM technology;

d. decreased incentives, on the part of DRAM manufacturers and others, to participate in JEDEC or other industry standard-setting organizations or activities; and

e. both within and outside the DRAM industry, decreased reliance, or willingness to rely, on standards established by industry standard-setting collaborations.

Rambus's Knowing Destruction of Documents

121. Rambus has engaged in a systematic effort – blessed if not orchestrated by its most senior executives – to destroy documents and other information. Upon information and belief, among other pertinent files destroyed as a result of this campaign were notes and other documentation relating to, among other things, Rambus's involvement in the JC-42.3 Subcommittee. Upon information and belief, this document-destruction campaign was undertaken, wholly or in substantial part, with the purpose of avoiding or minimizing the adverse legal repercussions of the anticompetitive conduct described in the instant complaint. Partly as a consequence of these document-destruction activities, in combination with other bad-faith litigation conduct, Rambus was required by the federal district court presiding over the *Infineon* litigation to pay a sanction exceeding $7 million.

First Violation Alleged

122. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has obtained monopoly power in the synchronous DRAM technology market and narrower markets encompassed therein – namely, the latency, burst length, clock synchronization, and data acceleration markets discussed above – which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Second Violation Alleged

123. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, with a specific intent to monopolize the synchronous DRAM technology market and narrower markets encompassed

Third Violation Alleged

124. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has unreasonably restrained trade in the synchronous DRAM technology market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Notice

Notice is hereby given to the Respondent that the eighteenth day of September, 2002, at 10:00 a.m., or such later date as determined by an Administrative Law Judge of the Federal Trade Commission, is hereby fixed as the time and Federal Trade Commission offices, 600 Pennsylvania Avenue, N.W., Room 532, Washington, D.C. 20580, as the place when and where a hearing will be had before an Administrative Law Judge of the Federal Trade Commission, on the charges set forth in this complaint, at which time and place you will have the right under the FTC Act to appear and show cause why an order should not be entered requiring you to cease and desist from the violations of law charged in the complaint.

You are notified that the opportunity is afforded to you to file with the Commission an answer to this complaint on or before the twentieth (20^{th}) day after service of it upon you. An answer in which the allegations of the complaint are contested shall contain a concise statement of the facts constituting each ground of defense; and specific admission, denial, or explanation of each fact alleged in the complaint or, if you are without knowledge thereof, a statement to that effect. Allegations of the complaint not thus answered shall be deemed to have been admitted.

If you elect not to contest the allegations of fact set forth in the complaint, the answer shall consist of a statement that you admit all of the material facts to be true. Such an answer shall constitute a waiver of hearings as to the facts alleged in the complaint and, together with the complaint, will provide a record basis on which the Administrative Law Judge shall file an initial decision containing appropriate findings and conclusions and an appropriate order disposing of the proceeding. In such answer, you may, however, reserve the right to submit proposed findings and conclusions under § 3.46 of the Commission's Rules of Practice for Adjudicative Proceedings and the right to appeal the initial decision to the Commission under § 3.52 of said Rules.

Failure to answer within the time above provided shall be deemed to constitute a waiver of your right to appear and contest the allegations of the complaint and shall authorize the Administrative Law Judge, without further notice to you, to find the facts to be as alleged in the complaint and to enter an initial decision containing such findings, appropriate conclusions, and order.

The ALJ will schedule an initial prehearing scheduling conference to be held not later than 14 days after the last answer is filed by any party named as a respondent in the complaint. Unless otherwise directed by the ALJ, the scheduling conference and further proceedings will take place at the Federal Trade Commission, 600 Pennsylvania Avenue, N.W., Room 532, Washington, D.C.

Notice of Contemplated Relief

Should the Commission conclude from the record developed in any adjudicative proceedings in this matter that Respondent's conduct violated Section 5 of the Federal Trade Commission Act as alleged in the complaint, the Commission may order such relief as is supported by the record and is necessary and appropriate, including but not limited to:

1. Requiring Respondent to cease and desist all efforts it has undertaken by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technohandgy (cluding bufurine vartion, sf prDEC-compliant SDRAM and DDR SDRAM

equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), for import or export to or from the United States, infringes any of Respondent's foreign patents, current or future, that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other Patent Application filed before June 17, 1996.

5. Requiring Respondent to employ, at Respondent's cost, a Commission-approved compliance officer who will be the sole representative of Respondent for the purpose of communicating Respondent's patent rights related to any standard under consideration by any standard-setting organization of which Respondent is a member.

6. Such other or additional relief as is necessary to correct or remedy the violations alleged in the complaint.

WHEREFORE, THE PREMISES CONSIDERED, the Federal Trade Commission on this eighteenth day of June, 2002, issues its complaint against said Respondent.

By the Commission.

Donald S. Clark
Secretary