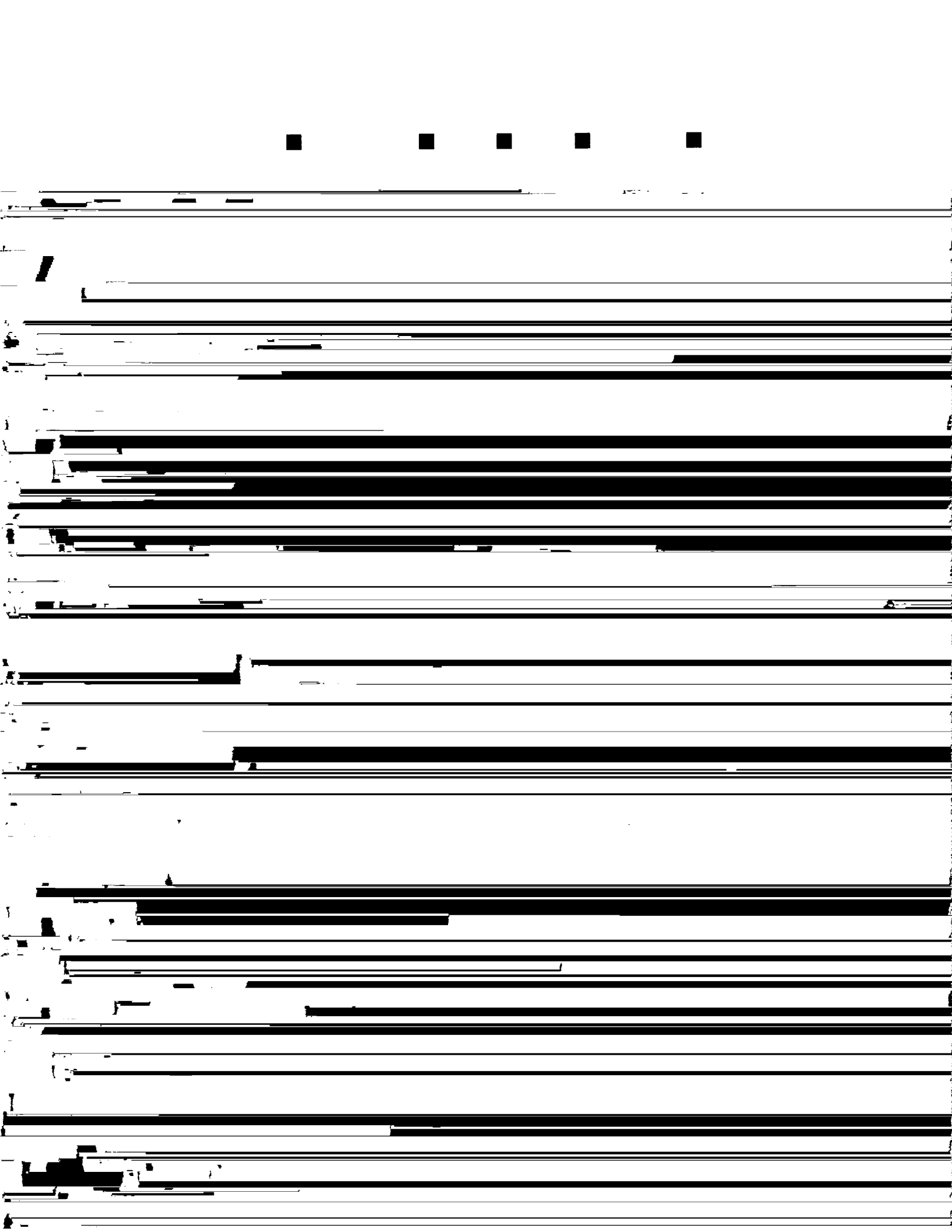
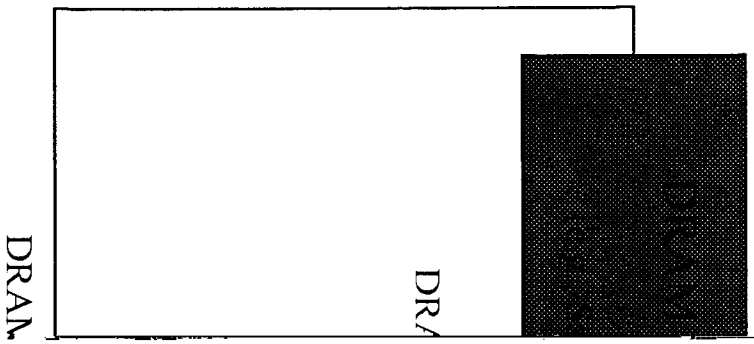
Interviews Conducted

- DI engineers
- DI plant managers
- JE participants
- DI users





TEXAS INSTRUMENTS

Micro

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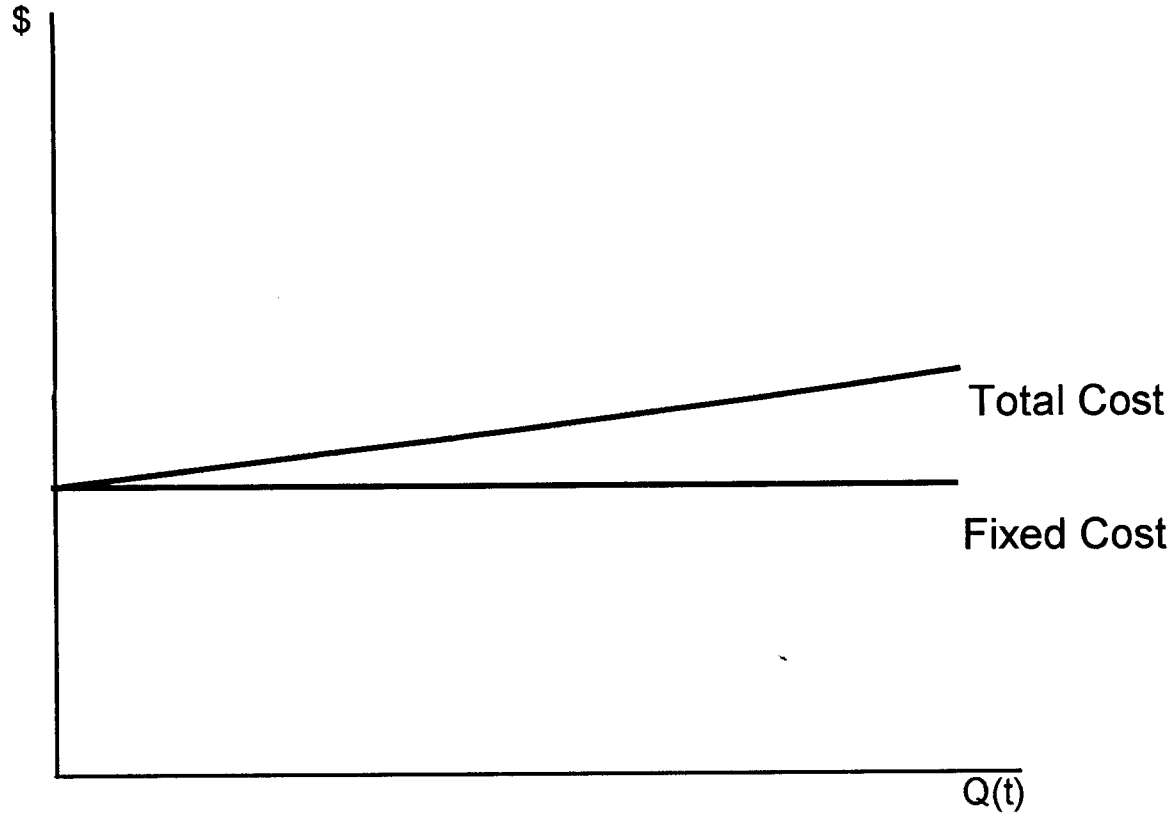
Economics of DRAM Production

- High fixed costs
- Volatility / cyclicality
- Intense price competition
- Maximize capacity utilization / yield
- Intense cost cutting

Total Cost and Fixed Cost



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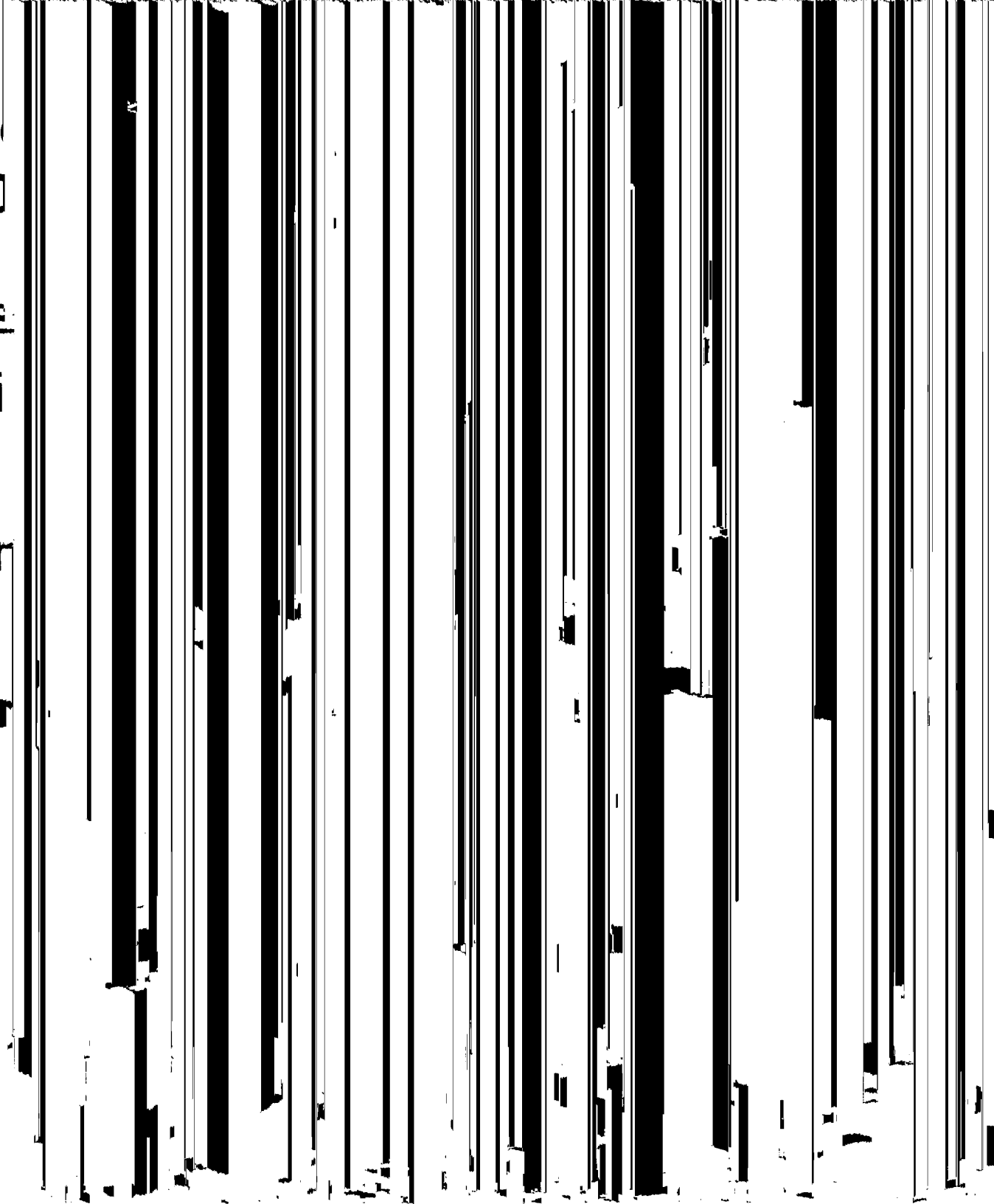
Economic Fa
D

- Open, consens
- Open availabili
- Royalties
- Implementatior
- Manufacturing
- Evolutionary / r

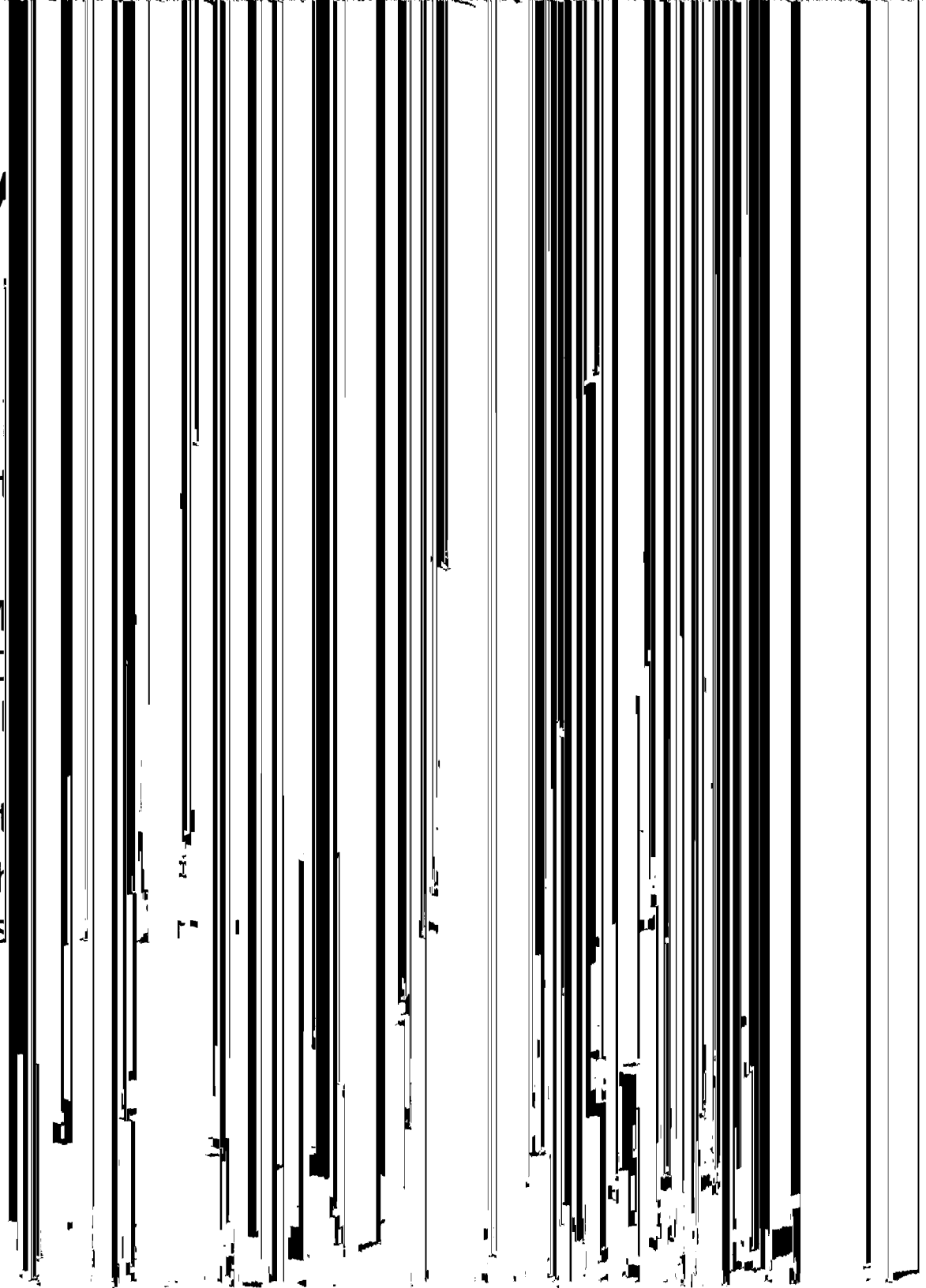


JEDEC: IP Disclosure

- Preference to avoid patents
- Early disclosure / good faith
- Disclosure applies to patents / patent applications relevant to JEDEC standards / work
- RAND: mandatory for JEDEC; voluntary for members
- Valid technical justification

Latency

- Fixed CAS late
  - Presented at J
    - NEC Presentat
  - Cost impact
    - "A fixed DRAM
      feature to the D
      point of view, t
      every function
      and burst lengt
    - Potentially high
      Macri Trial Tes



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Latency Technology Market

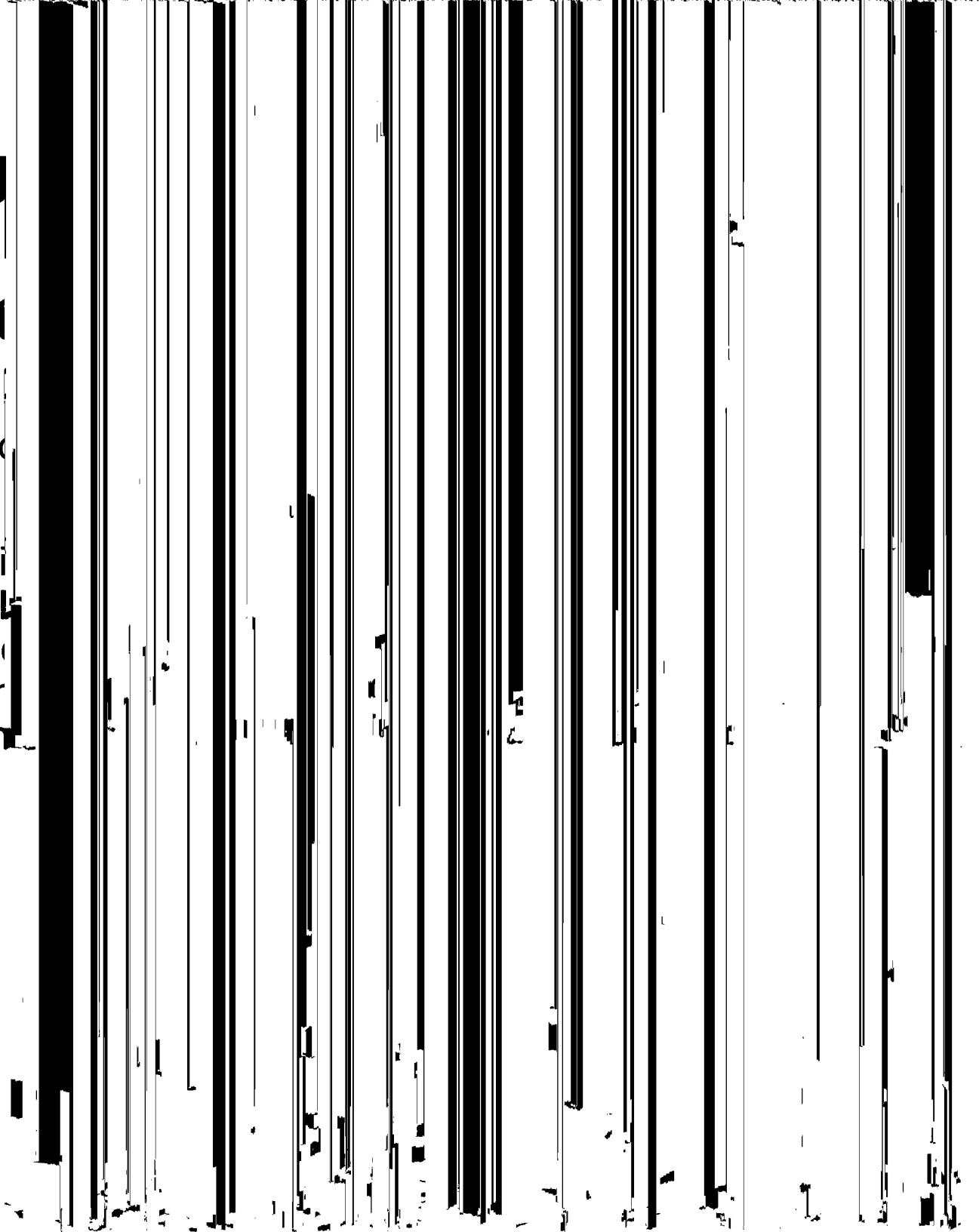
- Programmable in read command
  - Not presented at JEDEC
    - Mitsubishi Presentation at 42.3 Committee Meeti (12/91) (Programming Burst Length)
  - Cost impact
    - "The advantage would be that you would eliminat register and the circuitry required to decode spec commands and put that information into the mod so it would make the part potentially smaller and *Jacob Trial Testimony at 5391-92*

Latenc

- Set by fuses
  - Presented at
    - Cray Presen
  - Cost impact
    - "It would be
      eliminate the
      design and t
      fuse, you wo
      instead of ha
      would be a c
      Testimony a

Burst Leng

- Fixed burst lengt
  - Presented at JE
    - NEC Presentati
  - Cost impact
    - "A fixed DRAM i
      feature to the DI
      point of view, th
      every function ir
      and burst length



Burst Length Technology Market

- Programmable by pin strapping
  - Not presented at JEDEC
    - Micron Presentation at Special 42.3 Committee Meeting (7/00) (Programming CAS latency)
  - Cost impact
    - "The cost associated with each of those was relatively similar in the large scheme of things, so I would say from a cost standpoint, that was a large factor in our decision." *Kellogg Trial Testimony at 5132*

Burst Length Technology M

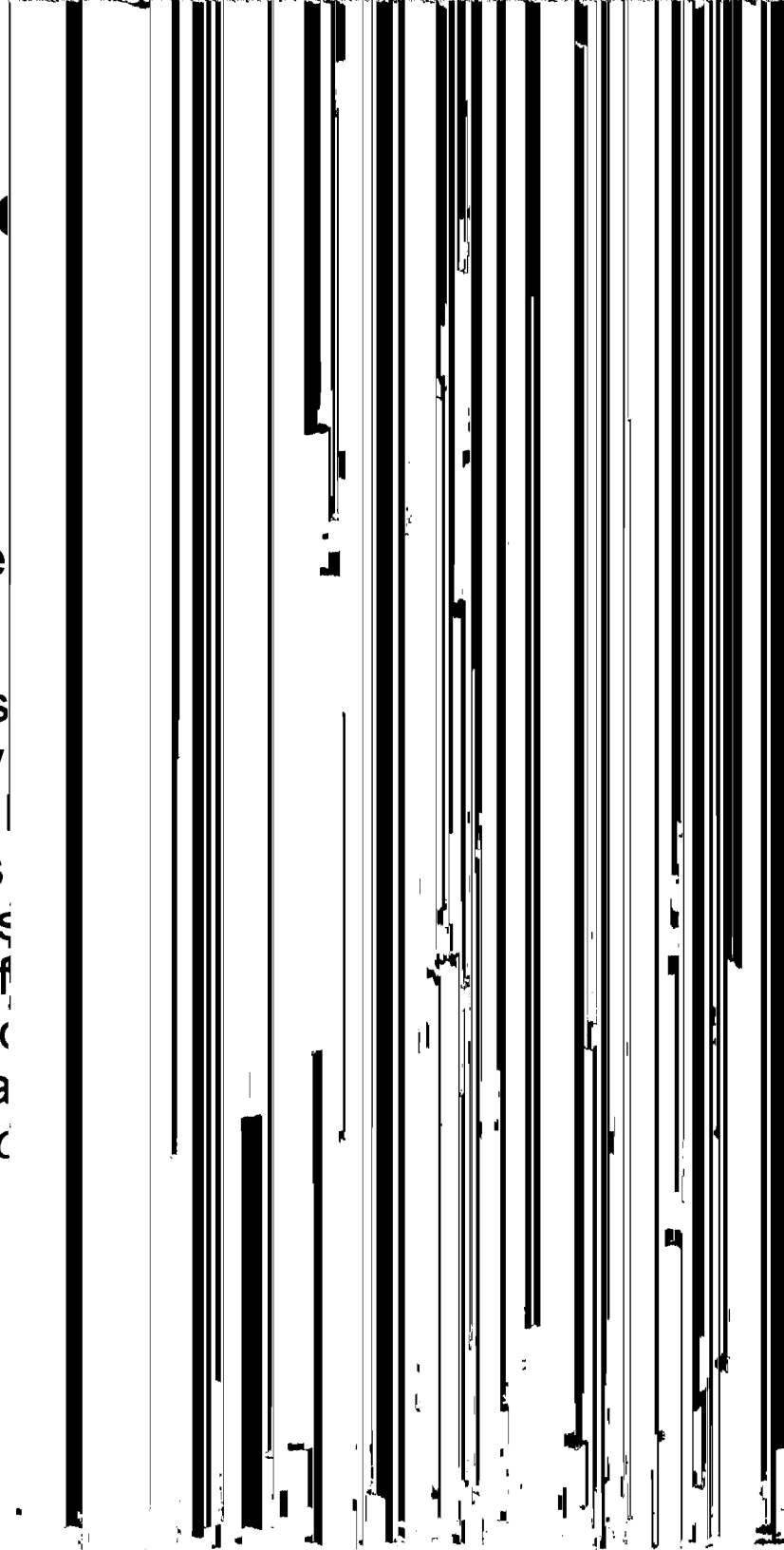
- Programmable in read command
  - Presented at JEDEC
    - Mitsubishi Presentation at 42.3 Committee M (12/91)
  - Cost impact
    - "Well, again, you would get rid of the mode r therefore the circuitry required to initialize it, make the part simpler to design and test and cheaper to manufacture." *Jacob Trial Testin*

Burst L

- Burst interr
  - In SDRAM
    proposed
  - Cost impa
    - "I mean,
      burst inte
      DRAM d
      words, th

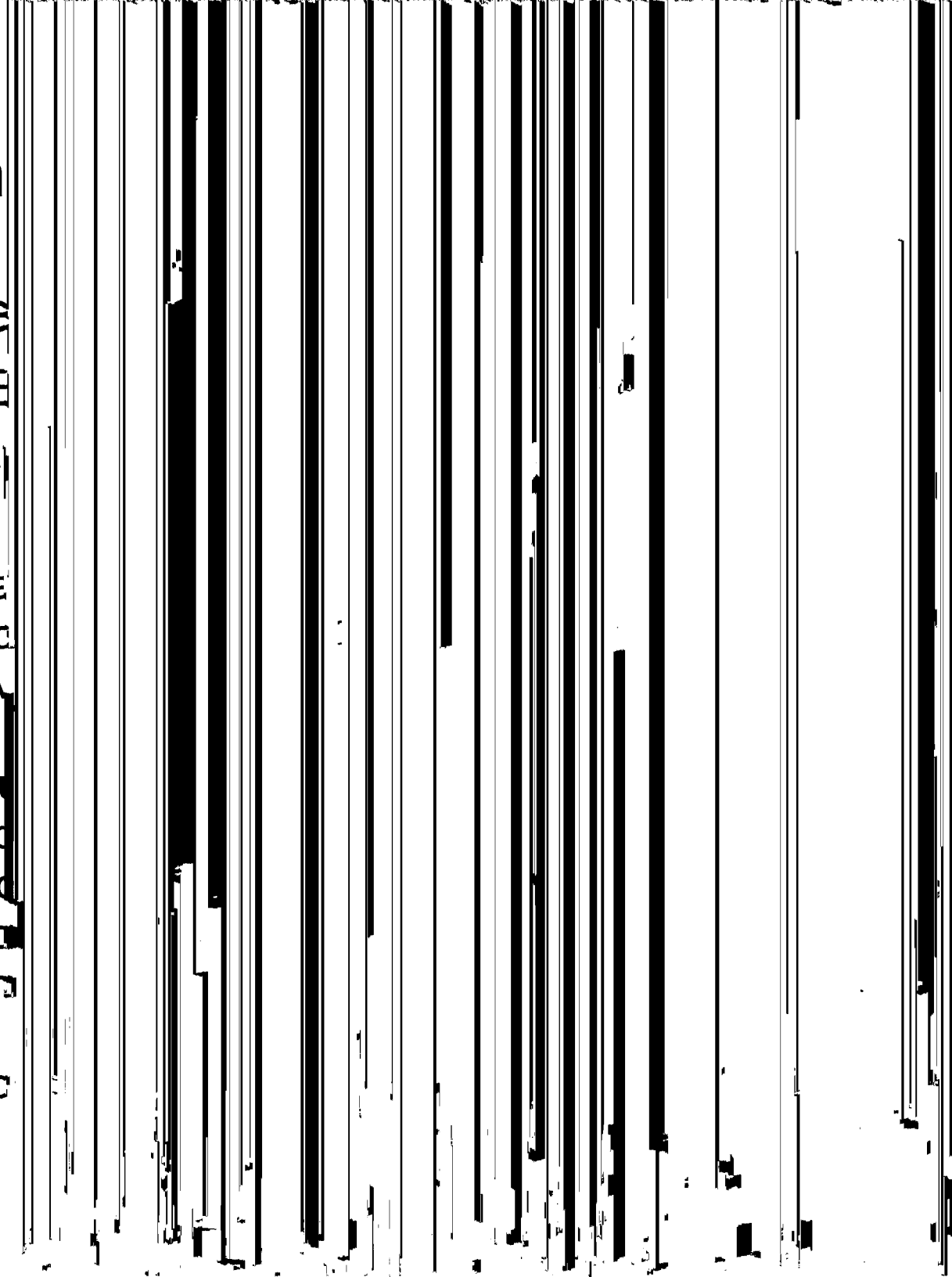
Data Acceleration Techn

- Double the clock frequency
  - Presented at JEDEC
    - VLSI Presentation at 42.3 Committe
  - Cost impact
    - "Well, a faster single edge clock has benefits in that we don't have to pay called duty cycle. Duty cycle -- you pulse that is high and a pulse that is is the length of the high pulse versus pulse, and managing that is very diff conditions. It sounds simple; very c clocking doesn't have that issue at a benefit to single edge clocking." *Mac 4779-4780*



Clock Synch

- Put the DLL on the
  - Presented at JEDE
    - Samsung Presenta
  - Cost impact
    - "You would elimina the power consump die size of the DRA cost of the DRAM. DRAM because yo that would be part c because it would nc take less time. And uncertainty than sin itself, so you could than just using an c at 5446-5447

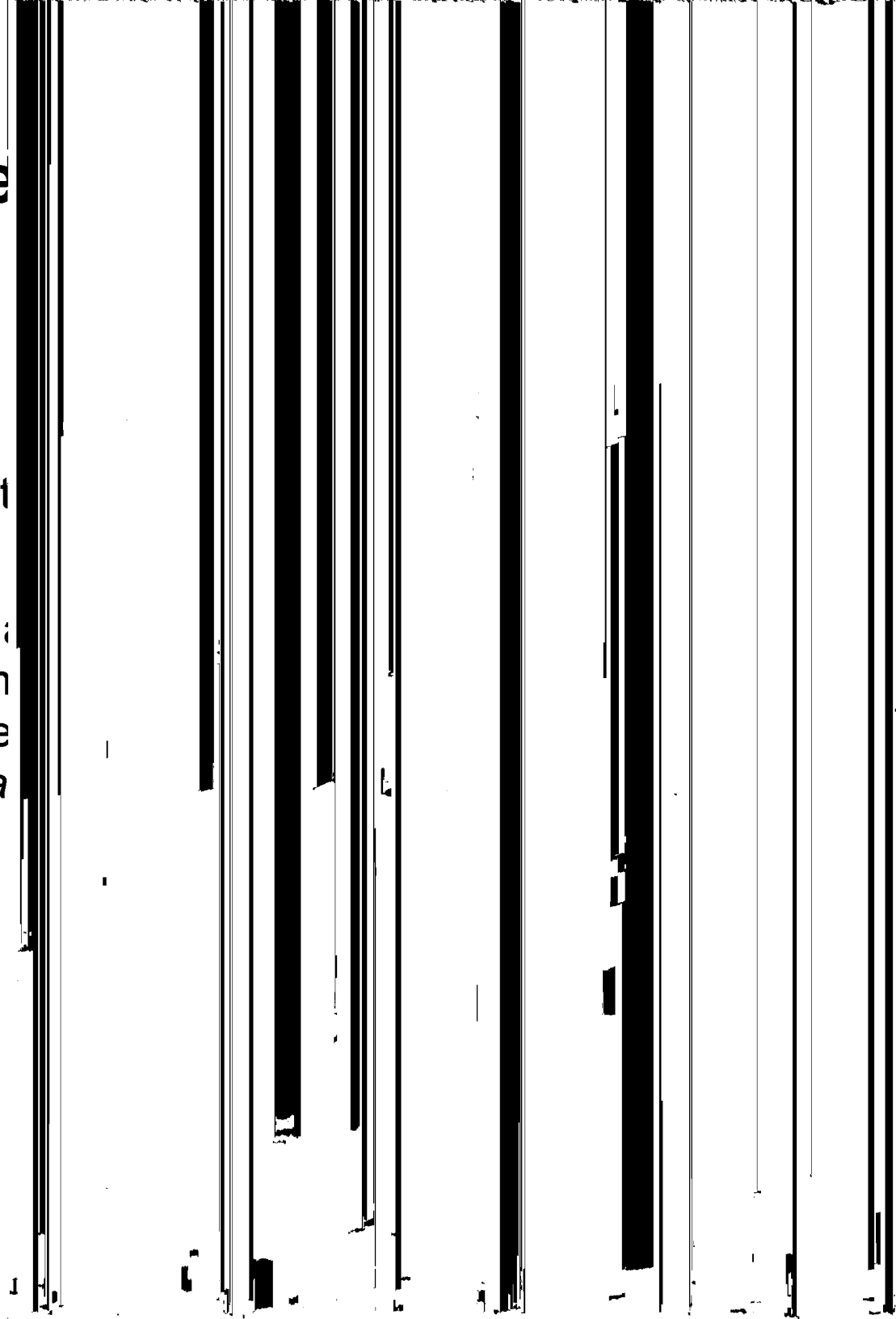


Clock Synch Technology Market

- PLL/DLL on module
  - PLL on DIMM in registered DIMMs and in Kentron QBM DIMM
  - Cost impact
    - "You eliminate the on-chip DLL from the DRAM, thereby reducing its power consumption, reducing its cost, reducing the design time. … [Y]ou then move that design complexity onto a special DLL chip that goes onto the module, so you would be trading one for the other." *Jacob Trial Testimony* at 5450

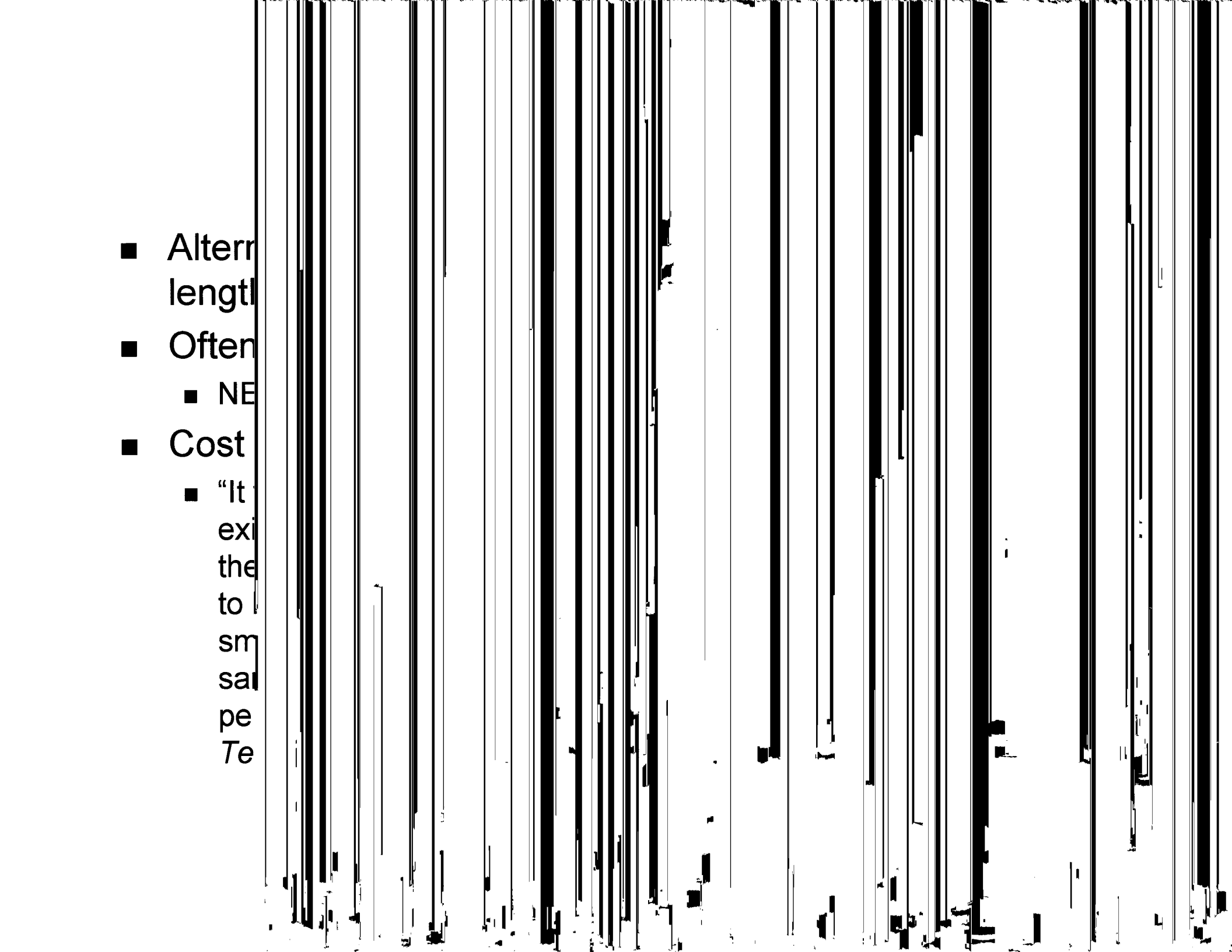
Clock Synch Te

- Vernier
  - Presented at JEDEC
    - Synclink Presentation at
  - Cost impact
    - "It's simpler to design th
      potentially more skew th
      achieve higher data rate
      Jacob Trial Testimony a



Clock Synch

- No DLL at all
  - Presented at JEDE
    - SGI Presentation a
  - Cost impact
    - "Q. Now, what, if a a DQS data strobe chip DLLs?
    - A. Well, you would your design simple design would be sn forth."
    - *Jacob Trial Testimo*



Reasons Why
Conduc

- Distorted JEDEC'
  concealing (or mis
  information
- Excluded alternati
  technologies
- Entailed a conscic
  enforceability of p

If Rambus Had D
No R

- Rambus documents st
  business model
- Rambus wanted flexib
  rates
- Rambus wanted RDRA
- Not issuing RAND lette
- Without RAND letter, J
  standard

Exclusion
Rambus's Cc

- By not disclosing IP *ex*
  incurred risk of having
- Implication is that Raml
  benefits from non-disclo
- Like predatory pricing,
  absent expected benefi
  competition