Complaint Counsel's Proposed List Of Rambus Expert Testimony To Be Covered In Rebuttal	Pages In Rambus Expert Reports And Depositions Where Issues Were Addressed
1. it is reasonable to assume that a first-tier manufacturer would run only 20 million units of a product iteration (Geilhufe, Tr. 9562:10-9563:4; 9725:1-9726:23)	Geilhufe Report at 10. ("The cost estimates in Tables 1-4 below are my best estimates based on my 30 years of integrated circuit manufacturing experience and are based on a mature product generation at a volume of 20,000,000 units per product produced by a leading manufacturer.") Geilhufe Depo. At 72:13-16 ("Q. . . . You are talking about a mature product generation at a volume of 20 million units per product produced by a leading manufacturer? A. Correct.") Geilhufe Depo. at 75:2-6 ("Q. Why did you use the number 20 million bits per product? A. I was trying to estimate what volume a top-tier manufacturer at this stage in production would be outputting. It's a best estimate that I took.")
2. use of fixed CAS latency parts is difficult and costly because (a) based on all options contained in the JEDEC standard as adopted (and not on industry usage or practice), 3 separate parts would be required (Geilhufe, Tr. 9578:10-23, Tr. 9682:20-9683:2)	Geilhufe Report at 11 (first column of table relating to the fixed CAS latency alternative shows that Geilhufe was basing his cost estimates on three separate parts) Geilhufe Depo. at 122:7-17 ("Q. Now, you concluded in this table, first column under Inventory, that there would be three parts -- A. Right. . . . Q. What did you base your conclusion on that there would be three parts manufactured? A. The JEDEC spec provides for the option for three parts.")

(b) it would cost
approxia)separate parts would be   c39.36 0 TD -0.036 Tc (-) T 3.96 0 TD -0.05:9 66.4l383:2)

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	the mode register, or does that refer to the cost of the product design itself? A. Good question. First your example has very little design effort per se. It just has the effort related to a simulation being able to create the tools. Given that for fixed CAS latency you now have more than one product, each product has to have its own photo tools. So to do each one of those products in my estimation is about 100,000, given that I have a baseline and I have a product that's done.")
(c) it would require assumptions about the speed grade of the parts (Soderman, Tr. 9347:8-9348:11)	Soderman Report at 24 ("Moreover, manufacturing a number of different fixed latency parts would have a s

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	however, in order to maintain acceptable yields for a wafer many of the fastest parts that currently command premium prices would have to be fixed with a latency value that would result in the full performance capability of the part not being realized and, consequently, could no longer be sold at a premium price.")
(e) it would add expense due to decreased die yield (Geilhufe, Tr. 9577:1-9578:9)	Geilhufe Report at 11 (first column of table relating to the fixed CAS latency alternative shows that Geilhufe was estimating an additional expense of approximately $.03 per unit due to decreased die yield)

3. use of fixed burst length parts is difficult and costly because (a) based on all options in the JEDEC standard as adopted (and not on industry usage or practiceRre0.0008 T0.48 4.8 r2.66.48 n 544.8 655.68 0.48 59.52 rn
            23.8 TD -0 110.0053 Tw6485.76 j 59.6look Tj my eRr inif I Tj f ap4149 Tw (CAS la f

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4. based on all options in the JEDEC standard as adopted (and not on industry usage or practice), use of both fixed CAS latency and fixed burst length would require 12-15 separate parts (Geilhufe, Tr. 9601:7-16)	Geilhufe Report at 15 ("JEDEC Standard 21-C specifies three different CAS Latency values for the SDR SDRAM, and five different values for the DDR SDRAM. Four different Burst Length values are specified for the SDR SDRAM and three different Burst Length values are specified for the DDR SDRAM. To fulfill the JEDEC Standard with fixed CL and B.L. products could require 12 or more different SDR DRAM products and 15 or more different DDR DRAM products for each current product – a major increase in manufacturing complexity, in inventory management, in distribution channel complexity, and in systems manufacturing complexity.") Geilhufe Depo. at 152:9-21 ("Q. So I understand, I had asked you if you made a determination of the number of DRAM products that would be manufactured if JEDEC went to a fixed CAS latency and fixed burst length structure. As I understand it, you said you did. What was that determination based on? . . . A. It was based on the JEDEC specification. Q. Was it based on anything else besides the JEDEC specification? A. No, it was based on the JEDEC specification.")
5. use of fixed CAS latency would not permit the mode register to be removed from the DRAM (Geilhufe, Tr. 9736:24-9737:19)	Geilhufe Depo. at 152:2-4 ("The mode register, in addition to CAS latency and burst length, has another element called burst type . . . .")
6. (a) electrically blown fuses and anti-fuses are not reliable (Soderman, Tr. 9356:18-9357:2)	Soderman Depo. at 149:18 – 150:6 ("Q. Are you saying it's no longer technically feasible to use electrically-fused DRAMs? A. It depends on what type you are talking about. If you're talking about an anti-fuse, everything is possible. The question is what is economically profitable. And that's what drives the DRAM industry. The anti-fuse technology does not have the same reliability as required for the DRAMs. They use it for programmable logic. And there is some percentage of those that we'll call regrade; in other words, have a defect either change with time or just don't get programmed correctly initially. So it's not a -- the electrically-programmed anti-fuse is not 100 percent

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	reliability like a laser fuse would be.") Geilhufe Depo. at 86:13-23 ("Q

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(d) the use of laser blown fuses would lead to reduced yield due to speed distribution (Geilhufe, Tr. 9585:21-9586:9)	Geilhufe Report at 11 (third column of table relating to the alternative of programming CAS latency using fuses shows that Geilhufe estimated that there would be reduced yield due to speed distribution, leading to an additional cost of $.03 cents per unit) Geilhufe Depo. at 131:24 -132:18 (Q. The next column -- the next element I would like to talk about is the final test and good unit yield for programming CAS latency with a fuse. A. Yes. Q. Now, you note in here your belief that it would lead to a reduced yield due to speed distribution, and that you were adding three cents per unit, approximately? A. Approximately. Q. Why do you believe that? A. As we discussed earlier, manufacturing process results in a distribution of speed, and fixed CAS latency has the potential of not using the entire speed range that the process turns out. And, therefore, has, if you will, potentially fewer good parts, certainly for the fast parts. Q. Is it an assumption of this column -- and by "this column" I mean the programming CAS latency with fuse column -- that the fuses are being burned by a laser prior to packaging? A. Absolutely.")
7. (a) based on the number of bits provided for in the JEDEC standard as adopted (and not on industry usage or practice), setting CAS latency and burst length via pins each would require three bits of information (Geilhufe, Tr. 9589:22-9590:6;	

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	Professor Jacob's report. He suggested that you add a pin possibly to provide voltages with the CAS latency information. In other words, you are programming the DRAM with an additional pin.") Soderman Report at 30 ("To allow for several latency values without using multiple voltage levels on a pin, would require the addition of two or three pins to the DRAM.") Soderman Depo. at 140:14 – 141:12, 143:6-13 (Q. Let me direct your attention to paragraph 63, first sentence, The first implementation proposed by Professor Jacob would be expensive to implement because of the necessity of adding pins. What is your basis for the conclusion that it's necessary to add pins? A. If you look at the package options that are available, and we're talking about -- the common packages at the time were frequently 54 pin TSOP, there were not a lot of extra pins, the pins in which configuration you have chosen there. If you have a by four, there are a couple of extra pins; if you have it by eight, there are fewer. If you have it by 16, I think there's one. Obviously it would not work if you're trying to encode all of this information with one pin. Q. Okay. But even with a by 16 there is one no-connect pin; isn't that right? A. A no-connect pin means that JEDEC has not specified the function. It does not mean it's not connected to something. It just means that JEDEC has not defined it. Q. Okay. A. It could be used in testing. So you're not necessarily free to go and use it for something else. . . . A. Actually, some of these parts come in a 32-bit output where there are no extra pins. They've used them all. So it depends on which flavor of the number of -- the organization of the array, by four, eight, 10, 16, 32, and we're talking about the 16 does not leave many left, there's either one or two that are not defined, not necessarily not connected, they are just not defined.")

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10. SLDRAM was unable to design a high speed DRAM using Vernier circuitry, without an on-chip DLL (Soderman, Tr. 9412:22-9415:9)	Soderman Report at 51 ("The inadequacy of the vernier alternative to on-chip DLL is illustrated by the failed efforts of a group of DRAM manufacturers to develop a DRAM without on-chip DLL. . . . In order to account for differences in the timing of various SLDRAMs in the system, the SyncLink design provided a vernier circuit on the controller that would analyze the timing difference and insert a programmable delay for data received from each SLDRAM. . . . Apparently, SyncLink determined that forgoing an on-chip DLL was not a workable solution. Ultimately, when an SLDRAM test chip was built, it incorporated an on-chip DLL.")
11. because the proposed alternatives didn't include circuit designs, they were poorly thought out (Geilhufe, Tr. 9673:17-9674:5)	Geilhufe Depo. at 206:16-24 (Vernier alternative): "Again, the description was inadequate for me to do a very clear analysis. . . . I don't know what specifically Professor Jacobs had proposed. Certainly there were no block diagrams or schematics.") Geilhufe Depo. at 232:25 – 233:7 ("THE WITNESS: The analysis of the alternatives is totally inadequate for a -- let's say if my design manager came to me in my general management role with these alternatives and said decide one, I would say go take another five engineers and go to work and do a better job and find serious alternatives analyzing carefully and give me the pros and cons of each one of them.")
12. DDR II (a) expands the use of programmable CAS latency (Soderman, Tr. 9351:7-9353:3)	Soderman Report at 23. ("The current proposal for the next generation 'DDR II' standard includes programmable latency values of 2, 4 5 and 6 (optional) plus a programmable additive latency of 0, 1, 2, 3, and 4, resulting in 8 possible read latency values . . . .")
(b) initially planned to use a single burst length, but subsequently reverted to programmable burst length (Soderman, Tr. 9369:12-23)	Soderman Report at 32 ("The JEDEC JC-42 Memory committee initially proposed fixing the burst length at 4 for the DDR2 specification . . ., but now intend to provide the variable burst length feature with burst lengths of 4 or 8.")

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