FEDERAL TRADE COMMISSION

I N D E X

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EXHIBITS*	FOR ID	ADMITTED	WITHDRAWN
JX			
Number 28		484	
Number 29		489	
Number 54		353	
Number 56		458	
Number 59		357	
DX			
Number 1		274	
Number 2		291	

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UNITED STATES OF AMERICA

FEDERAL TRADE COMMISSION

In the Matter of:	)
Rambus, Inc.	) Docket No. 9302
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Thursday, May 1, 2003

9:30 a.m.

TRIAL VOLUME 2

PART 1

PUBLIC RECORD

BEFORE THE HONORABLE STEPHEN J. McGUIRE

Chief Administrative Law Judge

Federal Trade Commission

600 Pennsylvania Avenue, N.W.

Washington, D.C.

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P R O C E E D I N G S

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JUDGE McGUIRE: This hearing is now in order and convened at 9:30 a.m. Counsel, how is everyone this morning?

Before we start today with the presentation of the case in chief by the Government, are there any issues that should come at this time to the Court's own attention?

If not, the Court seeks to inquire of the parties, have they made any progress toward the issue raised by the Court on the agreement the parties had entered into on what items of evidence were going to be offered and entered into this record?

MR. ROYALL: Your Honor --

JUDGE McGUIRE: Mr. Royall?

MR. ROYALL: -- good morning.

JUDGE McGUIRE: Good morning.

MR. ROYALL: Mr. Stone and I did speak about that last night, and I think the short answer is we have made progress. We're not at a point at which we've finalized something that we can present to you, but we hope that we will be at that point soon. Part of it involves obviously reviewing and paring down the evidence, and that may take a little while, but we do

expect that we are going to be able to do that and then have a stipulation that also maybe includes some of the features of the other stipulation but will have the effect of paring down what we're presenting at this time.

JUDGE McGUIRE: All right, Mr. Stone, do you want to comment?

MR. STONE: Yes, that's correct, Your Honor.

JUDGE McGUIRE: All right, then let me advise then on that basis and clarify even further the Court's concern over this issue. It has decided to vacate the earlier order entered into by the parties, and until such time that the parties are able to agree on an agreement on evidence that can be approved by the Court, any items offered into this evidence shall be I think ruled upon one at a time.

Are we clear on that?

MR. STONE: Yes, Your Honor.

JUDGE McGUIRE: Any evidence that is offered in this hearing and excluded shall still be preserved for any possible appeal purposes, okay? Are we clear?

MR. STONE: Yes.

MR. ROYALL: Yes, Your Honor.

JUDGE McGUIRE: Is there anything else either side wants to comment on?

MR. ROYALL: Not at this time.

JUDGE McGUIRE: If not, then at this time we will hear presentation of the case in chief by the complaint counsel.

MR. OLIVER: Good morning, Your Honor.

JUDGE McGUIRE: Good morning.

MR. OLIVER: Complaint counsel calls to the stand Mr. Desi Rhoden.

JUDGE McGUIRE: Mr. Rhoden, could you please approach the bench and be sworn.

Whereupon--

DESI RHODEN

a witness, called for examination, having been first duly sworn, was examined and testified as follows:

JUDGE McGUIRE: Please have a seat right there, Mr. Rhoden. Thank you.

DIRECT EXAMINATION

BY MR. OLIVER:

Q. Good morning, Mr. Rhoden. How are you today?

A. Good morning, fine.

Q. Could you state your full name for the record?

A. My name is Desi Rhoden.

Q. Are you currently employed, Mr. Rhoden?

A. I currently hold the title of president and CEO for Advanced Memory International, that position being

unpaid at this time.

THE REPORTER: Could you speak into the microphone, please?

A. Yes, my name is Desi Rhoden.

Q. And where are you currently employed, Mr. Rhoden?

A. I currently hold the title of president and CEO for Advanced Memory International, a position that is unpaid at this time.

Q. What is AMI-2?

A. AMI-2 is a consortium, a nonprofit consortium of memory suppliers and infrastructure providers that have banded together for the coordination and development of infrastructure for the memory industry.

Q. Could you please describe your responsibilities as president of AMI-2?

A. Yes, my responsibilities as president, I work with companies within the industry, all of the infrastructure players, people that are involved in the industry to help coordinate the development and infrastructure, if you will, all of the bits and pieces that have to go into making a complete system work in the industry.

Q. Mr. Rhoden, what is your educational background?

A. I have a Bachelor's and a Master's Degree in electrical engineering from Colorado State University.

Q. Could you please give us a brief description of

your work experience?

A. Yes, I attended college. I was drafted, I spent some time overseas in Vietnam. I returned. I spent about ten years or a little more working as an electrician, returned to school, worked as an instructor for one of the colleges at the university, and upon receiving my Master's, I worked at Storage Technology for a short period of time, spent about eight years at Hewlett Packard, about five or six years at VSLI Technology, and the last three years, I have been at Advanced Memory International.

Q. Could you please briefly describe your work at Hewlett Packard?

A. Yes, while I was at Hewlett Packard, I was a design engineer and worked as -- Hewlett Packard calls them scientist people that work as the technical leads for their technical development programs, working together with the development of integrated circuits, chips, if you will, and high-speed systems and interfacing with outside customers.

Q. You mentioned chips. What types of chips did you work with at Hewlett Packard?

A. This would be silicon chips, interface chips for memory, interface chips for graphics development, a number of different things inside the computer itself.

Q. Now, you mentioned that you had worked for a company named VLSI after leaving Hewlett Packard. Is that right?

A. Yes, VLSI is the company name. It also happens to be a common industry acronym. The acronym stands for very large-scale integration, but the company is just VLSI Technology.

Q. What does VLSI Technology do?

A. VLSI Technology is a -- well, it is no longer. It was purchased by Phillips a few years ago. It was at the time an ASIC development house, and this is a company that would develop custom integrated circuits for particular customers. They also developed some of their own chips that they sold on the open market. They were one of the first providers of computer chipsets for the personal computer industry.

Q. You mentioned the term "ASIC." Could you please spell that and describe what that is?

A. Yes, ASIC is A-S-I-C and stands for application-specific integrated circuit.

Q. Could you please describe your work at VLSI?

A. Yes, when I was at VLSI, I came there as a -- to start a program for them, to develop a design team and -- as well as continue my work inside of the industry memory coordination and standardization and

worked as the liaison -- I worked as a manager, director and eventually I was an engineering fellow, which is sort of the technical liaison, if you will, or technical lead for a lot of programs inside the company.

Q. Turning now to your work at AMI-2, what types of companies do you interact with in your work at AMI-2?

A. Okay, the kinds of companies that I would work with and still do work with inside of AMI is -- would include memory suppliers, the people who actually manufacture memory chips; motherboard providers, the people who actually make the boards that go into your computers; processor suppliers, people who make the processors; chipset providers; logic providers; module makers; people who make basically all the different pieces that make up computers or gaming machines or whatever.

Q. Mr. Rhoden, you have referred to memory now a few times. Could you please explain first, when did you first begin working with memory?

A. One of my primary roles inside of HP is -- as part of high-speed system development, memory is a critical element inside of any computer system, and in that system, I started working early with memory, and

I've been doing that almost my entire career.

Q. Mr. Rhoden, if we could perhaps turn now to explore memory in a little more detail. Are you familiar with the term DRAM?

A. Yes, I am.

Q. What is DRAM?

A. Well, DRAM is a type of memory that's -- DRAM is dynamic random access memory.

Q. Are there other types of memory?

A. Well, there's many types of memory. Three come to mind. The three major types of memory would be DRAM and SRAM and flash.

Q. What is SRAM?

A. SRAM is static random access memory as opposed to the dynamic that we talked about before.

Q. What is the difference between static and dynamic ram?

A. Okay, in static, the SRAM, in static, static memory is a type of memory where the information that is stored stays in the memory without refresh until it moves from the chip. On the other hand, dynamic is something that is a temporary storage, if you will, and it does require refresh.

Dynamic memory, you can have a lot more bits and pieces that you actually store than you can in

contained in all of the devices that you see around here, DRAM.

Q. How is DRAM used in a computer?

A. DRAM is actually the scratchpad, if you will. It is the -- it's the area where all transactions and information is stored and processed, stored and retrieved in the computer while it's in operation, during the operation, so it's the scratchpad where you are jotting down notes before you are actually trying to save anything permanently.

Q. Where in the computer is DRAM located?

A. Perhaps a picture or two would be helpful. I think I have some pictures that would show you better.

MR. OLIVER: Excuse me, Your Honor, I am technically challenged and need help for a moment.

MR. STONE: Your Honor, we had had an understanding that we were going to exchange demonstratives 24 hours in advance of the witness' testimony where the demonstratives are going to be used. Obviously there is nothing particular about this demonstrative, but I do think that's our understanding, and if it's not, I think we should just be clear we are not going to exchange demonstratives.

JUDGE McGUIRE: Is that the understanding, Mr. Oliver, that you had entered into?

MR. OLIVER: Your Honor, I had actually proposed that and I had not heard back.

MR. STONE: Then that's my -- I had said at the time it was fine. I said anything you wanted to propose in that regard was fine.

MR. OLIVER: That apparently was a miscommunication, Your Honor.

MR. STONE: My fault, then.

MR. OLIVER: We do have a hard copy here --

JUDGE McGUIRE: Well, if it is not going to be an understanding, it is going to be an order of the Court that that occur. So, if you want to take some time, I don't know if we need to take time here --

MR. STONE: We don't need any time on this one, Your Honor.

JUDGE McGUIRE: -- but in the future, let's abide by that rule, that 24-hour exchange, all right?

MR. OLIVER: Yes, Your Honor.

JUDGE McGUIRE: All right, then let's proceed.

MR. PERRY: Thank you.

BY MR. OLIVER:

Q. Mr. Rhoden, I had asked you to explain where DRAM is found in a computer.

A. Certainly. What you see here in this first foil is a picture of a computer with the three major

elements. You have the display, the keyboard and then the box that contains all of the computer elements.

If you go to the next foil, you will see that you can open up the box, the tower, the pizza box, whatever you -- people have lots of different names for it depending upon its configuration, and inside, what you can see is the inside where there is a motherboard, which is the principal backbone, if you will, that everything plugs into.

It's a little difficult to see here, but perhaps if you go to the next picture, you can see a picture of a motherboard that actually has been extracted, and memory itself is -- the DRAM itself is contained at the bottom right-hand corner. You see some slots across the -- I think perhaps if you hit the next display key, there you see the memory module is actually located at the bottom of the display. You can see it right here, yes.

MR. OLIVER: Your Honor, I see that Mr. Rhoden is trying to point to the figure on the screen. Would it be possible to turn one of the screens towards you so that he could point out certain aspects to you?

JUDGE McGUIRE: I'm sorry, is it possible to do what?

MR. OLIVER: To turn one of these screens

towards you so that Mr. Rhoden could point out certain aspects of the picture to you?

JUDGE McGUIRE: Well, I've got it right here, I mean --

THE WITNESS: Yes, you have. I will do my best to describe the location.

JUDGE McGUIRE: Just describe what corner it's in, and if we have any other concerns in that regard, then we will turn around the screen. I'm trying to help everyone here.

MR. PERRY: Could I suggest that you might have a hard copy and you could draw on it, where he's describing, you could circle it for your future use? I don't know, maybe --

JUDGE McGUIRE: What we'll do, and I think I had indicated this earlier prior to starting the hearing, that if there was a time when I had to have a hard copy, then I would ask for it. So, that's what we'll do in the future, but I don't think I have to have it here.

MR. OLIVER: Okay, thank you, Your Honor.

THE WITNESS: Okay.

BY MR. OLIVER:

Q. Mr. Rhoden, I note that on the drawing there's a reference to a CPU microprocessor. What is that?

A. Actually, CPU is a terminology that stands for the central processing unit, also known as the microprocessor. This is the central brain, if you will, of the computer. It's the one that processes information and makes decisions based on the information that it's processing. And all of this immediate storage that it uses, temporary storage it uses, would be there in the memory modules located in the DRAM.

Q. I also see a reference to memory modules. What is a memory module?

A. Okay, if you look there between the yellow lines that are defined as memory modules, you will see individual integrated circuits, individual chips, if you will, that look in a vertical position. They are actually mounted onto a separate PC board, a very small one, and that PC board is a combination, a grouping, if you will, of memory devices, and the grouping comes in something that we term as a module.

So, you see -- in this one, you see eight memory devices on a particular module, and then you see three module sections plugged into the computer here.

MR. OLIVER: Your Honor, may I approach?

JUDGE McGUIRE: Please.

MR. OLIVER: I would like to show this to the

witness, please.

JUDGE McGUIRE: All right.

BY MR. OLIVER:

Q. Mr. Rhoden, I have handed you an object. What is that object?

A. This is an example of a memory module, much like the one that you see in the picture here. You see the eight memory devices that are actually on the module. The module itself is just a small printed circuit board, and it's connected through an edge connector that would then plug into what is this motherboard. The motherboard is essentially the place where everything gets connected together.

MR. OLIVER: Your Honor, could I invite Mr. Rhoden to step up and opposing counsel to step up so Mr. Rhoden could point out the memory module to you?

JUDGE McGUIRE: Yes, that's fine.

BY MR. OLIVER:

Q. Mr. Rhoden, if you could please approach the Bench, and if you could point out to His Honor the parts of the module that you just explained.

A. Yeah, the memory device itself is this chip that you see here. You'll see this repeated eight different times across here. This would be -- the module itself is interconnected through the wires, the

traces that you see on the circuits and on the back, and there's also some inner layers inside this printed circuit board. These would be some of the support

BY MR. OLIVER:

Q. Mr. Rhoden, are you familiar with the term "chipset"?

A. Yes, I am. Chipset is the term inside -- that we use in the industry that defines a grouping of chips that actually are the traffic cops for the motherboard. They connect all these pieces together, the memory, the CPU, all of the different I/O devices, the input, output, things like keyboard, graphics display, all of that that would be contained to the left-hand -- most left-hand half of that picture that you see of the motherboard, and you'll see two main chips on either side and one of the primary support chips that goes along with the chipset itself in the middle.

Q. How are these various components connected together?

A. Well, on the motherboard, you can actually see there's a number of traces, but rather than try to figure out how they're connected here, perhaps a logical drawing -- this is a physical layout, and I think the next demonstrative has a physical layout -- this is actually the logical description of what goes on, much more simplified than what takes place.

Q. Mr. Rhoden, perhaps before we move to the logical diagram, if I could approach again, Your Honor,

I would like to present you with an actual motherboard --

A. Okay.

Q. -- and again, I would like you to point out the components on the motherboard itself.

A. Sure.

JUDGE McGUIRE: All right, you may approach.

THE WITNESS: The -- in this particular -- what you see here --

JUDGE McGUIRE: Hold on until opposing counsel has a chance to --

MR. PERRY: I'm sorry.

THE WITNESS: That's okay. This would be the CPU, the central processing unit, microprocessor, if you will. Then there are -- the chipset that is here, contained with a few others that are separated around here, and this would be then memory modules that would plug into this device, and this being the traffic cop that connects, as the memory controller, the communication to the memory, and it also has other bits and pieces that communicate with the rest of the system.

This is what communicates with the outside world, the I/O, if you will, that would be your keyboard, monitor, those types of things. Those memory

modules, actually the modules that you have, would actually plug right into here, okay?

JUDGE McGUIRE: Okay, thank you.

MR. OLIVER: Your Honor, I will need to double-check to see if I have permission to use this before it's entered into the record.

JUDGE McGUIRE: Okay, okay.

MR. OLIVER: If I am able to get such permission, then perhaps later today I will --

JUDGE McGUIRE: Yes.

MR. OLIVER: -- request that.

JUDGE McGUIRE: And if so, we will have it marked as DX-2, if you decide to do that.

MR. OLIVER: Okay, thank you.

BY MR. OLIVER:

Q. Mr. Rhoden, you had referred to a demonstrative that you believed could help explain the bus. Could you please explain this demonstrative?

A. Certainly. This interface that you see here, the one that says DRAM basic interface, is actually a very simplified block diagram of what you saw on the motherboard. It's much easier to explain, because there's a lot of pieces on a motherboard, and rather than jump right into the middle, it's easier to start with a block diagram, if you will.

it depends on the speed obviously of the particular machine, but the clock itself is a signal that provides time blocks of information.

Q. Is the clock specific to DRAM or does it operate on components more generally?

A. The clock is more general. It's existed in DRAM and memory controller, CPU. There's a clock that generally runs inside the whole system, sometimes many clocks, sometimes quite a few.

Q. Now, you referred to control lines. What exactly are control lines?

A. The control lines themselves have specific functions, and in the case of what we're looking at here between the memory controller and the memory itself, the control lines would be determining what type of operation. Perhaps we're reading from the memory or we're writing to the memory.

Remember, the memory itself is just a scratchpad, so we have to decide whether we are going to write something to the scratchpad or whether we are going to retrieve it from the scratchpad. It's sort of the language, if you will, saying here, you're placing data out there or you're bringing data back, and the control lines are the ones that determine what type of operation.

Q. With respect to the signals traveling over the control lines, do those signals travel from the chipset to a module or from a module to the chipset or both?

A. The -- the control lines and the address lines in this case that you see actually are one-direction kind of operations. They originate in the memory controller and then travel to the DRAM, provide -- so, the memory controller will make the request and send that request across to the DRAM.

The data, by definition, would need to go in both directions, because I'm writing to it and I'm reading back from it at another time.

Q. If I could ask you to explain in a little more detail what the address lines do.

A. Okay, the address lines provide -- as you see here, you see a number of chips. You see eight just like the memory module that you had a copy of, and those address lines address locations within these memory modules. The typical system today, you would address one location in each of these memory devices that will broadcast information, each one broadcasting their own bits of data back across for a read or accepting data on a write. So, the address are the particular location, and to understand the address, you need to understand the -- a little bit inside the

memory itself.

Q. Okay, we'll look at that a bit later today.

A. Okay.

Q. Now, the lines here are illustrated in different colors. Do any of the types of lines illustrated in the bus ever carry other types of information? For example, would control lines ever carry data?

A. No, the control lines -- the data lines themselves are the only data that -- are the only lines in this drawing that actually carry information in both directions, and the address lines and control lines actually are one-direction lines, and so it's not very useful to be able to send something out to memory and never see it again in terms of data. So, data are the only ones that are bi-directional. The address and control are not used for data.

Q. What I was trying to understand is whether any of the lines in this bus would be multifunctional, whether there would be any lines that would carry, for example, control information and address information and data.

A. There are no lines in this particular bus that carry control, address and data, no.

Q. We'll come back to memory technology later

today in some more detail.

A. Okay.

Q. At this time, I'd like to turn to JEDEC.

A. Okay.

Q. Are you a member or a participant in any industry standard-setting organizations?

A. Yes, I am a member of JEDEC. I actually am the chairman of the board of directors for JEDEC.

Q. What is JEDEC?

A. JEDEC is a -- it's a standard-setting body for primarily the semiconductor industry, and there are some 50 committees, about 1800 participants from about 250 companies around the world that come together to set standards on a variety of things; memory, quality of reliability, electrical interfaces, any number of things, all relating -- most all of it relating to the semiconductor industry itself. It works inside the Electronic Industries Alliance, the EIA, with other organizations to ensure -- one of them, for instance, is the Consumer Electronics Association that delivers these products to the rest of the world as well.

Q. How did you first learn of JEDEC?

A. Actually, when I was working at HP and working with memory, the desire at the time was to improve some of the communications path, the operations, perhaps

speed even of the memory itself, and so as I investigated how best to do that in the industry, I became aware of JEDEC. JEDEC is the place where industry standards are set for the DRAM, one of the things -- one of the functions JEDEC provides, and in that capacity, JEDEC actually had a committee that was set up to standardize memory, and that is the best place that I have found to actually work and create and make changes, modifications, in memory devices themselves.

Q. Did you ever attend the JEDEC meetings?

A. I have been attending JEDEC meetings, still do, for quite a number of years. I've attended many.

Q. When did you attend your first JEDEC meeting?

A. In the late eighties sometime.

Q. Focusing now in the early 1990s, particularly in the time period between 1991 and 1996, did you attend JEDEC meetings regularly?

A. Yes, I did.

Q. Did you attend meetings of any particular JEDEC committees or subcommittees?

A. Yes, actually, my -- during that particular period of time, my primary focus was in memory and more specifically in -- in memory related to the PC and also related to graphics, and so all of that would have been

inside the JC-42 committees. It's just a number that we use inside JEDEC to represent memory devices, and so the -- inside JC-42 and the subcommittees associated with that, I would attend those meetings regularly and did.

Q. What are the subcommittees associated with JC-42?

A. Well, there's a number of them, and over the years, we have done some reorganization based on the needs, but primarily 42.3 is the DRAM committee. There's 42.2, that is the SRAM committee, if you will. There's also a 42.5, which is where we develop the memory modules. So, they all are related, if you will, to memory. And there's other 42. committees that would deal, for instance, with flash memory and any other type of programmable devices.

Q. Are you still active in the JC-42.3 subcommittee today?

A. Yes, I am. I'm actually the chairman of the JC-42 overall committee.

Q. Now, you mentioned that you are currently the chairman of the board of directors of JEDEC. Is that correct?

A. That is correct.

Q. How did you assume that position?

A. Actually, the chairman of the board of directors, I was elected to that position by my peers in the industry. JEDEC used to be part of the Electronic Industries Association, and in about '98-'99, we split EIA into multiple, separately incorporated associations, and at that time, the governing body of JEDEC itself became a board of directors, and I was elected as the board chairman at that time.

Q. I'm sorry, could you state for the record when you were elected as chairman?

A. About 19 -- prior to -- JEDEC became independently incorporated in about 19 -- December I think of 1998, and prior to that, I was chairman of the JEDEC Council, which was the JEDEC governing body, and I was chairman of the board from that time forward. From the time that JEDEC has become a corporation, I have been chairman of the board since that time.

Q. What are your duties as chairman of the board of directors of JEDEC?

A. Well, chairman of the board of directors is, frankly, a pretty thankless job, because it's -- like everything else in any standards organization, it's all volunteer, and so it's a lot of work for essentially nothing in return. You have -- my responsibilities at

JEDEC actually encompass -- or as chairman of the board, it's the business aspect of JEDEC, trying to make sure that we have office space, staff, relationships with other organizations, and to make sure that we take care of the business aspects of the corporation itself.

Q. By the way, what is the approximate size of the board of directors at JEDEC?

A. The approximate size of the board of directors, about 25 or so people. It varies over time. It has a

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A. I do not.

Q. You also mentioned that you serve as chairman of the JC-42 committee. Is that correct?

A. Yes, that is correct.

Q. What are your duties as chairman of the 42 committee?

A. As chairman of the 42 committee, 42 is responsible for, as I said, all of the memory components, and there are the other point committees, as we call them, 42.3, 42.2, 42.5. As chairman of the 42 overall committee, one of my main responsibilities is to make sure that we have -- we can coordinate all of the different committees, the modules, the DRAMs themselves, and we would meet in conjunction with some other committees, JC-40, for instance, that is a logic committee, and JC-16, which is an interface committee, we would meet all at the same time, at the same location. So, the coordination of all of those committees and all of the activities that go on inside those committees is one of my primary responsibilities.

Q. Mr. Rhoden, you also referred to EIA. Would

number of different groups within the Electronic Industries Association that operated in many segments of the electronics industry, and at that time, the executive committee and board of governors of EIA decided to split it into multiple -- actually I think five separate corporations to then create an alliance of associations. Rather than having one association, an alliance of associations, primarily to encourage other people, other associations to become part of that.

Q. Between 1990 and 1998, what was JEDEC's status within EIA?

A. Between 1990 and 1998, JEDEC was a subpart of JEDEC, actually existed inside the engineering department, if you will, inside of JEDEC, and their role was to take care of the standardization of semiconductors and standardization of chips, if you will, much the same as it does today independently.

MR. OLIVER: Your Honor, at this time I'd like to use the first exhibit with the witness, but I would like to ask the o the day indec3parate corporations to po p

JUDGE McGUIRE: I'm sorry, I couldn't hear your final statement there.

MR. OLIVER: Whether you would prefer to have me present you, the witness and opposing counsel with a set of the exhibits or --

JUDGE McGUIRE: I thought I had indicated earlier, and at this time I will take whatever input either side has, but I don't need the entire set. I could just use it as you go through it, but it's whatever is easier.

Does opposing counsel have any suggestion?

MR. PERRY: Whatever Your Honor wants is fine with us. It might be easier --

JUDGE McGUIRE: Then I will do whatever you have already planned to do. If you have the whole set, then I'll take the whole set, and then just be sure opposing counsel has their set.

MR. OLIVER: All right, thank you, Your Honor.

JUDGE McGUIRE: We'll proceed that way.

MR. OLIVER: If you could give us just a moment, please, Your Honor.

JUDGE McGUIRE: Sure.

(Brief pause.)

MR. OLIVER: I'm sorry, could you please give us just a moment, Your Honor?

JUDGE McGUIRE: All right, let's go off the record for a couple of minutes.

(Pause in the proceedings.)

JUDGE McGUIRE: Counsel, we were talking off the record, and I had indicated that as a consequence of having entered DX-1 into this evidence, we had posters offered at the time of the opening comments by respondent, and then I received copies of those posters. So, at this time, we had discussed about also having those marked, and I believe I understand counsel at this time is to have those copies of the posters marked as DX-2. Is everyone clear on that?

MR. STONE: Yes, Your Honor, and I'll take care of providing a copy to the court reporter of that.

JUDGE McGUIRE: Thank you, Mr. Stone.

(DX Exhibit Number 2 was admitted into evidence.)

JUDGE McGUIRE: Yes, you may approach. Thank you.

MR. OLIVER: Thank you.

JUDGE McGUIRE: All right, Mr. Oliver.

MR. OLIVER: Are we on thk,E v7bl rightm*t93)

in the documents in front of you, I believe it's the top document.

A. Yes, I have it.

Q. It bears the title Are Standards Worth the Effort? Do you have that document?

A. I do.

Q. Do you recognize that document?

A. Yes, I do.

Q. Did you prepare this document?

A. Yes, I did.

Q. When did you prepare it?

A. I actually put this particular presentation together from a series of other presentations that I had made, oh, perhaps many times previously, and I prepared it I believe in December or so of last year for a presentation to IBM.

Q. When did you prepare this document?

A. In the latter part of last year.

Q. If I could ask you to turn to page 8 of CX-302.

A. Okay.

Q. This is a page bearing the caption A Few JEDEC Members. Do you see that page?

A. Yes, I see that.

Q. Could you please explain what this page demonstrates?

A. When I put this page together, it was intended to show an overview of some of the members that would be a part of JEDEC. As I said, there is some 250 companies, and I couldn't really put all of them on one page. So, I took a few of them just to kind of give a cross-section of some of the companies and types of companies that would be part of it.

Q. What types of companies are illustrated on this page?

A. Well, there's a number of types of companies. If you take ALi in the top left corner and VIA perhaps in the bottom right, those would be chipset companies. AMD and Intel are microprocessor companies, perhaps even at some level a system house. Amkor is primarily a packaging company. We have already talked about ALi. Celestica does computer memory modules and is also a PC board manufacturer. Elpida is a -- Elpida, Hynix, Samsung and Micron, Infineon, those would be memory suppliers. Hewlett Packard, IBM are system -- OEMs, if you will, that make themselves computer systems, among other things, printers, lots of things.

There's -- and you can go to Lucent. Lucent is -- if all of you are familiar with Lucent, they are in networking and other types of things. Motorola, cell phones. Those kinds of companies.

Q. Do you have an understanding as to why so many different types of companies are members of JEDEC?

A. Well, the need and breadth of the development in standardization, all of these companies participate because standards provide good business for themselves and for their customers. The customers drive them into standards I'm sure perhaps probably more than themselves.

Q. In terms of worldwide sales, do you have an understanding of the approximate percentage of worldwide sales that are represented by the DRAM manufacturers that are members of JEDEC?

A. It's -- I'm sure it's in excess of 90 percent, perhaps in excess of 99. Almost all DRAM manufacturers in the world are members of JEDEC.

Q. Are JEDEC members all United States companies?

A. Oh, certainly not. You can see even from this page, they come from a wide range of companies -- a wide range of countries, as well. ALi, VIA are a Taiwanese company. You can see Elpida is -- Toshiba, Sanyo would be Japanese companies. Samsung, Hynix are Korean. Infineon, German. We have companies from around the world.

Q. How does a company become a member of JEDEC?

A. Companies become a member of JEDEC by paying

dues.

Q. If I could direct your attention back to the first page of that document, the title reads Are Standards Worth the Effort? Do you see that?

A. Yes, I do.

Q. And let me ask you, are standards worth the effort?

A. Well, the question I was asking when I created this is to give some people something to think about, and yes, they certainly are worth the effort.

Q. Why are they worth the effort?

A. Well, standards actually provide a broad supply from many different -- a broad supply base, a broad customer base. Standards provide a number of things, and I think there's even some details of my opinions about what makes them good inside this presentation.

Q. If I could direct your attention to page 5 of CX-302, the page bearing the caption What Standards Mean.

A. Okay.

Q. Do you see that page?

A. I have it, yes.

Q. And if I could direct your attention to the first bullet, which reads, "To the End Users."

Do you see that?

A. Yes, I do.

Q. Who are the end users referred to in this slide?

A. Well, the end users actually exist on a number of different levels. They exist from the mom and pop that go down to CompUSA or Sam's Club or wherever to buy their local computer, all the way up to the Fortune 500 companies that also would buy -- in reference to memory, obviously they would buy memory from the suppliers themselves. So, a broad range, from big companies all the way down to individuals. That's what users are.

Q. What, if any, is the importance of standards to the end users?

A. Well, I show a list. The low price and broad supply, the uniform terms and definitions, consistent quality and reliability, common packaging. Essentially what they're asking for is they want interchangeability where they can get it from multiple places, get the same thing from multiple places. It gives them a great deal of advantage in the market.

Q. Now, if I could direct your attention to the second main bullet point towards the bottom of the page, it states, "To the Supplier."

Do you see that?

A. Yes. Yes, I do.

Q. Who are the suppliers that you're referring to on this slide?

A. It -- when I originally created this slide, it was about the memory industry, and the suppliers themselves would be the primary memory suppliers, and that would be like Samsung, Micron, Infineon, Hynix, those types of companies.

Q. There's a sub-bullet underneath that that reads, "Large demand, pre-sold customer base."

Do you see that?

A. Yes, I do.

Q. What did you mean when you included that in the slide?

A. Well, the suppliers -- there's a great deal of investment, billions of dollars, that go into the creation of factories and designs that are necessary to produce DRAM, and the supplier gets a large demand, because working with the customer inside an area like JEDEC, because you're working together with your customers and with the supply base, and when everyone agrees, then they have essentially an automatic market, because they're working together -- on something together, and now they have basically a presold customer base just by complying and working with the

standard.

Q. If I could direct your attention to page 3 of CX-302, please. This is a page that bears the caption Challenges for Standards.

A. Yes, I see it.

Q. And if I could direct your attention to the first bullet point and sub-bullet point, "Everyone wants a competitive edge -- but the customers want standardization."

In that second line, customers, what were you referring to with the term "customers"?

A. Well, yes, I actually put this particular foil together for a presentation that I made at the Intel Developers Forum, and that was a memory presentation, and the customers that I was referring to in this case would be the major system houses, the OEMs, HP, IBM, Compaq, Dell, that kind of company.

Q. What types of products are produced by customers, as you were using the term in this slide?

A. Those customers would be the kinds of customers that would be the major manufacturers for PCs, perhaps other things, but certainly for personal computers, networks and servers, a lot of things that use DRAM.

Q. Why do the customers want standardization?

A. Well, they -- frankly, they like to have a

broad customer supply base so they can pit one supplier against the other and get the lowest possible price. They also like to make certain, besides price, control and price -- beside price leverage, they also have the capability that if one supplier disappears or whatever, they still have a continuous supply. So, standardization is something that they -- they -- going to basically demand. It's one of the things that all of these customers -- that customer base, the OEMs, have -- they insist upon.

Q. Let me direct your attention to the last line of that slide. This is still page 3 of CX-302.

A. Yes.

Q. The line reads, "Delay is not a viable market option."

Do you see that?

A. Yes, I do.

Q. What does that line mean?

A. This line is an indication that the customer base can -- wants continuous improvement, and they push for it, they demand it, and trying to sit around and wait for something to happen is not basically in their nature. So, the delay is not a viable market option. You can't really wait until after you develop something and then decide to standardize it. You have to move in

real time at the time that technology is being developed to create the standards.

Q. What happens if a standard is delayed?

A. Well, it depends on what scale. Customers would like to have it yesterday always, and suppliers would prefer to ship what they have today, but for some reasonable amount of time, as long as everybody continues to work, delay is still acceptable.

What I was trying to point out here is that there is an urgency in the development of standards, because if you delay and if you wait too long, then sooner or later someone else will replace and do the job for you.

Q. If I could direct your attention, please, to page 9.

A. Okay. Okay.

Q. It's a page bearing the caption Guiding Principles.

A. Yes, I have it.

Q. The first bullet point there reads, "Promotion of open standards."

Do you see that?

A. Yes, I do.

Q. What did you mean when you used the term "open standards" in this presentation?

A. Well, open standards inside of JEDEC essentially means that we want to set up a mechanism where everyone can participate that wants to, and in the end, the end product is then available to everybody in the world. So, open participation, open accessibility, if you will.

Q. Just to be clear, were you distinguishing between two different concepts there?

A. Yeah, actually, open standard is open in the development process and open in the final end product. So, it would be open from the standpoint of the creation of the standard, and then the final product needs to be available and usable by everybody who chooses to use it.

Q. Now, what, if any, is JEDEC's position with respect to open standards?

A. JEDEC insists upon open standards. That's the way we work actually. All JEDEC standards are available for free on the web.

Q. Why does JEDEC insist on open standards?

A. Well, the whole premise behind JEDEC is the concept of developing things that are good for the industry. It is the industry working together for the benefit of the industry and the end users, all of the people that would actually use the product, and there

wouldn't be any benefit from the JEDEC perspective to developing anything except open standards.

Q. If I could direct your attention to the last line on page 9 of CX-302, it reads, "Uphold the principles of Anti-trust."

A. Yes.

Q. Do you see that?

A. Yes, I do.

Q. What did you mean when you included that line on this slide?

A. When I included this line, what I intended to convey was that the principles of antitrust are such that every -- it's available to everyone, so we would eliminate discrimination. So, not only can everybody participate, everyone else does have access to the standards, so elimination of discrimination.

Q. By the way, Mr. Rhoden, I see the term "JEDEC" in the lower right-hand corner of this document.

A. Lower right-hand corner?

Q. Yes. Does that mean that the guiding principles listed here refer specifically to JEDEC?

A. Yes, it does. JEDEC is the -- this is the guiding principles for all of the JEDEC operation.

Q. Why is it a guiding principle of JEDEC to uphold the antitrust laws?

A. Well, first of all, it's a law, so that's probably first and foremost the reason we do it, but it's also the principles of antitrust to produce and create standards that are free of discrimination is important to the people that are involved, because otherwise, we could not achieve our first goal that you see there of open standards. We have to have free availability of the standards.

Q. Mr. Rhoden, if I could ask you to locate a document labeled CX-204.

actually has abstained as a perfectly viable place to vote, and we encourage you to abstain if you do not have any interest. That way we prevent the possibility of passing irrelevant standards.

JUDGE McGUIRE: All right, thank you.

THE WITNESS: So, only people that are interested vote.

JUDGE McGUIRE: Okay, thank you.

Mr. Oliver, you can proceed.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

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A. This is a document that's available and produced for all people who were involved in EIA activities at the time, EIA and JEDEC both for that matter.

Q. Could I please direct your attention to page 5 of CX-204, and in the upper --

A. Okay.

Q. -- in the upper left-hand corner, there's a part beginning Section C, Basic Rules for Conducting Programs.

Do you see that?

A. Yes, I do.

Q. If I could begin to read a passage for you, "All EIA standardization programs shall be conducted in accordance with the following basic rules: 1, they should be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation."

Do you see that?

A. Yes, I do.

Q. Do you have an understanding of the term "good faith" as used in that passage?

A. Yes, I do. The term "good faith" as used in this passage is that the people that come -- are coming under the premise that they're going to work toward the

betterment of the industry and the betterment of the -- work toward the benefit of the end user of the industry itself, and operating in good faith means that you would expect other people to do the same thing.

Q. Mr. Rhoden, if I could also direct your attention to number 5 under that heading. Again, this is still under the caption, "All EIA standardization programs shall be conducted in accordance with the following rules," and number 5, "They shall not be proposed for or indirectly result in effectuation of a price fixing arrangement, facilitating price uniformity or stabilization, restricting competition, giving a competitive advantage to any manufacturer, excluding competitors from the market, limiting or otherwise curtailing production, or reducing product variations except where required to meet one or more of the objectives set forth in section D of this Part II."

Do you see that?

A. Yes, I do.

Q. Do you have an understanding of that provision?

A. Yes, I do.

Q. What is your understanding of that provision?

A. We use these rules to make certain -- this is how we control the discussion topics. Nothing that's listed here is ever allowed as part of the discussion

inside of any JEDEC meeting, for instance, and this basically makes certain that we uphold the law here.

Q. Mr. Rhoden, what, if anything, did JEDEC do to implement its goal of developing open standards?

A. Well, in development of open standards, besides the policies that you see listed here, we wanted to make sure that -- to eliminate and make certain that everybody can be available, we had certain policies in place, and perhaps the most important is our patent policy, to make sure that we have standards that we produce that are open and available to everyone involved.

Q. What is the JEDEC patent policy?

A. The JEDEC patent policy is essentially if you have IP, IP that may relate to any of the discussions that are going on inside JEDEC, that you are required to disclose that IP to the people who are participating.

Q. Are there any other aspects to the patent policy?

A. The disclosure is one aspect of it, and after it's been disclosed, before additional discussion can take place on that particular topic, assurances from the IP holder have to come in a way that guarantees unfair discrimination for the users of that. So,

there's -- I think there's two basic. You either offer it for free to all of the people who are creating the standards or you offer it on usual and nondiscriminatory conditions for the industry.

MR. PERRY: Your Honor, can I just ask what time period we're talking about here?

JUDGE McGUIRE: Sir, can you answer that?

THE WITNESS: The time period?

JUDGE McGUIRE: Yes.

THE WITNESS: The time period, it has been the same for approximately the whole period of time I've been a part of JEDEC.

BY MR. OLIVER:

Q. Mr. Perry actually asked my next question, which is --

JUDGE McGUIRE: You're clairvoyant, Mr. Perry.

MR. PERRY: Thank you.

BY MR. OLIVER:

Q. If I could ask simply about the time period for a moment from late 1991 to 1996, and if the answer would differ for any subperiods, please let me know, but could you please describe the JEDEC patent policy specifically with respect to time period between late 1991 and mid-1996?

A. Well, the JEDEC patent policy has been

basically the same throughout all of that. The only thing that actually changed, we did update some documents throughout that period of time, so some wording perhaps could change, but the requirement for disclosure has always been the same, and the disclosure requirement applies to the people who hold the IP.

It also applies to anyone who has knowledge of it. So -- and we have multiple examples of that inside of JEDEC, but these legal guidelines that you see here would be the ones that would have been in effect throughout that time period.

Q. Looking again at the time period from late 1991 to mid-1996, what level of detail was required in a disclosure?

A. There are details. The level of disclosure, you had to disclose that you -- well, as I say, anyone who has knowledge of the IP is required to disclose it, whether it's the holder or someone else, but once that's been disclosed, before additional discussion can proceed on those topics, it's necessary that the holder of the IP provide assurances to the JEDEC committee that they would be willing to license on reasonable, nondiscriminatory or free.

Q. Mr. Rhoden, if I could ask you to locate a document bearing the Exhibit number CX-208 in front of

you. It should bear the --

A. 208?

Q. Yes, CX-208.

A. Okay.

Q. It should state JEDEC Publication, JEDEC Manual of Organization and Procedure.

A. I have it.

MR. OLIVER: Actually, Your Honor, a quick housekeeping matter. Before I proceed, at this time, could I offer into evidence CX-302?

JUDGE McGUIRE: Mr. Perry, any opposition to -- you said CX, did you say?

MR. OLIVER: Yes, I offer into evidence CX-302.

MR. PERRY: No objection.

JUDGE McGUIRE: All right, if there is no objection, it shall be entered at this time.

Could I inquire, however, as to CX-1 and 2, have they not been entered or --

MR. OLIVER: I'm sorry, Your Honor?

JUDGE McGUIRE: This is CX-3?

MR. OLIVER: No, this is CX-302.

JUDGE McGUIRE: Oh, 302, I apologize.

MR. OLIVER: Yes.

JUDGE McGUIRE: Okay, right, offered and entered at this time.

(CX Exhibit Number 302 was admitted into evidence.)

MR. OLIVER: Your Honor, at this time I would also like to offer into evidence CX-204.

MR. PERRY: No objection.

JUDGE McGUIRE: If there is no objection, also entered.

(CX Exhibit Number 204 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, do you have in front of you a document bearing the exhibit number CX-208?

A. Yes, I do.

Q. Do you recognize this document?

A. Yes, I do.

Q. What is it?

A. This is the JEDEC Manual of Organization and Procedure. We refer to it as 21, JEDEC Publication 21.

Q. By the way, Mr. Rhoden, do you recall seeing this document while you were a participating member of the 42.3 subcommittee?

A. Oh, certainly. All of the people that are members of JEDEC would have access and would have seen this document.

what was nonresponsive and speculation in that last part after he answered that he had seen it.

JUDGE McGUIRE: Restate the whole question, if you could, Mr. Oliver, so I can hear again the answer.

BY MR. OLIVER:

Q. Yes, I asked whether you had seen this document, CX-208, while you were a participating member of the JC-42.3 subcommittee.

A. Yes, I saw it in two presentations at the subcommittee.

Q. Excuse me, you said that you saw it in --

A. I did see it while I was at JEDEC and through -- and in relation to JC-42.3, I saw this document, and this was updated in October 1993, so revisions were presented at the JC-42 subcommittee.

Q. How were revisions presented at the JC-42.3 subcommittee?

A. These would have been presented at that time probably by Mr. Townsend or Mr. Gordon Kelley. Mr. Kelley was the editor, if you will, of this document, actually created it. So, one of the two of them, perhaps both of them, certainly talked about it.

Q. Who would -- excuse me, who was Mr. Gordon Kelley?

A. Gordon Kelley was the chairman of JC-42.3 at

that time. He was also in this same time frame, he -- or sometime about this time, Mr. Kelley became part of the JEDEC Council, and I'm not actually clear what his position was, but he was the chairman of JC-42.3.

Q. Do you have an understanding of the purpose of CX-208?

A. Yes. This is the manual that is for all of the participants inside JEDEC to operate and for JEDEC committees to operate under.

Q. Did you ever hear Exhibit 208 referred to as a chairman's manual?

A. Never.

Q. If I could direct your attention to page 18, please.

A. Okay.

Q. And specifically, I'd like to direct your attention to the paragraph under Section 9, Legal Requirements, under that, 9.1, Legal Guides, and to the last sentence of that paragraph. It reads, "EIA Legal Counsel can advise the Council and committees from time to time concerning interpretation of legal guides."

Do you see that sentence?

A. Yes, I do.

Q. Now, in the 1993 to 1996 time frame, who was EIA legal counsel?

A. That would have been John Kelly.

Q. Is Mr. John Kelly still EIA's legal counsel today?

A. Yes, he is.

Q. Do you know if he holds any other positions today?

A. Yeah, Mr. Kelly is also president of JEDEC.

Q. Mr. Rhoden, if I could direct your attention to Section 9.3 at page 19. Under the caption 9.3, Reference to Patented Products in EIA Standards, I would like to direct your attention in particular to the second sentence of that paragraph. "While there is no restriction towards drafting a proposed standard and terms that include the use of a patented item," two asterisks, "if technical reasons justify the inclusion, committees should ensure that no program of standardization shall refer to a product on which there is a known patent unless all of the relevant technical information covered by the patent is known to the formulating committee, subcommittee or working group."

Do you see that?

A. Yes, I do.

Q. Do you have an understanding of the meaning of that sentence?

A. Yes, I do.

Q. Could you please explain your understanding of the meaning of that sentence?

A. Yes, this is -- this is what I said before, the -- no discussion will continue if a patent or any IP is disclosed inside the committee on work that's taking place in the committee until there have been assurances from the IP holder.

Q. Okay. After the term "patented item," there are two asterisks.

A. Yes.

Q. Do you have an understanding of what those asterisks refer to?

A. Yes, that would refer to a footnote.

Q. That would be the footnote at the bottom of the

to anything within the patent process, and the author of this particular version wanted to make certain that everyone knew and understood that there -- it applied to all aspects of patent, patent applications and what have you.

MR. PERRY: Your Honor, again, I'll move to strike his answer to the extent it refers to others' understandings and the purpose of the author, as opposed to his own understanding, which was the question.

JUDGE McGUIRE: Was that to your understanding or to all others' understanding?

THE WITNESS: It is my understanding and in direct communication with the people who wrote it.

JUDGE McGUIRE: Then sustained to that extent.

MR. PERRY: Thank you, Your Honor.

JUDGE McGUIRE: To the extent he just answered that question, it's in, and I am going to entertain it. I am going to entertain his answer as he just responded to that last question.

Are you unclear, Mr. Oliver?

MR. OLIVER: I am unclear.

JUDGE McGUIRE: All right, restate your answer so that everyone is clear as to what the answer is first.

THE WITNESS: Okay. Could you please reread the question, and I'll try my best to answer it directly?

JUDGE McGUIRE: Okay, court reporter, would you read it.

(The record was read as follows:)

"QUESTION: Do you have an understanding of the meaning of that footnote?

"ANSWER: Yes, I do.

"QUESTION: And what is your understanding?"

THE WITNESS: Okay, the understanding that I have for the footnote that is here is that this footnote was added to further emphasize for anyone reading the document and to myself the word "patent" has always applied to all things within the patent process inside of JEDEC, and that's the explanation that has always been given by myself inside of JEDEC committees, and the footnote was added to add -- make sure that everyone understood that the word "patent" involved everything within the patent process.

BY MR. OLIVER:

Q. What do you mean by "everything in the patent process"?

A. Essentially, if -- everything in the patent process is -- if you -- the best way to answer it is if

term "the obligation of all participants"?

A. The obligation of all participants is essentially what we just talked about. It is the requirement that you are obligated to disclose -- you have an obligation to disclose everything that is in the patent process. It must be disclosed.

Q. Did everybody at JC-42.3 subcommittee meetings make proposals for standards?

A. Not everyone makes proposals, no, not even today.

Q. The term "the obligation of all participants," did that refer only to people making presentations, or did that refer to a larger group?

MR. PERRY: Objection to the extent you're asking for beyond his understanding.

JUDGE McGUIRE: That's inferred in that question. He's asking his understanding. So, overruled.

THE WITNESS: It has always been my understanding that the rule has applied to every participant. It says every participant, is referred to as every participant, and we -- the chairman and all the people that produced this and all of the committees always say every participant.

BY MR. OLIVER:

Q. I'm trying to clarify for the record the definition, if you will, of the term "participant." Did that refer just to people making presentations or did that refer to some other group?

A. In -- the clarification of the term "every participant," it's everyone who is a member either in attendance or not in attendance, a guest, a -- whoever is either in the room at the time discussions are held or has access to any of the JEDEC information outside of the meetings themselves.

Q. And if I could direct your attention to the term "pending patents" in the phrase that we just read, between October 1993 and mid-1996, did you have an understanding of the term "pending patents" --

A. Yes, I did.

Q. -- as it's used in this section?

A. Yes.

Q. What was your understanding of the term "pending patents" at that time?

A. Once again, it's anything that's in the process of -- of a patent, from disclosure all the way through to the actual obtaining a patent. It's not pending once it's been granted, so anything up to that process regarding the invention itself.

Q. When you refer to "disclosure," what were you

referring to?

A. The -- what I'm referring to is the requirement of the participants inside JEDEC to make known to the standards formulating committee their knowledge of intellectual property.

Q. Are you familiar with the term "patent application"?

A. Yes, I am.

Q. Would patent applications be included in your understanding of the term "pending patents"?

A. Yes, it would.

Q. If I could direct your attention to the phrase "might be involved" in the passage that I just read the part of the passage, "that might be involved in the work they are undertaking."

Do you see that?

A. Yes, I do.

Q. Between October 1993 and mid-1996, did you have an understanding of the term "might be involved" as it was used in that passage?

A. Yes, I did.

Q. What was your understanding?

A. My understanding has always been for this particular passage that it -- if the intellectual property has any relevance to the work that's going on,

it might be involved -- we're not asking the people that are disclosing to actually try to do a determination of whether it applies or doesn't apply. We're saying if it's related, in the same general area, then you must disclose it. You are obligated to disclose it.

Q. The passage that I read for you begins, "The Chairperson of any JEDEC committee, subcommittee or working group must call to the attention of all those present."

Do you see that?

A. Yes, I do.

Q. In your experience attending JC-42.3 subcommittee meetings, did committee chairmen, in fact, call attention to the obligation of all participants at the meetings?

A. Yes, numerous times, often times many times per day. At all meetings, there was discussion about this type of activity, all that I can remember.

Q. Mr. Rhoden -- excuse me, Your Honor.

(Brief pause.)

MR. OLIVER: I'm sorry, Your Honor, I'm experiencing some throat difficulties.

JUDGE McGUIRE: Taufteour exmes

Q. Mr. Rhoden, if I could direct your attention to page 29 of CX-208, please. This is a page that bears the caption Appendix F, and titled at the top, F1, Patent Policy Application Guidelines.

Do you see that page?

A. Yes.

Q. If I could direct your attention to the third bullet point, please, which reads, "By its terms, the EIA Patent Policy applies with equal force to situations involving: 1, the discovery of patents that may be required for use of a standard subsequent to its adoption."

Do you see that?

A. Yes.

Q. Between October 1993 and mid-1996, did you have an understanding of the meaning of that passage?

A. Yes.

Q. And what was your understanding at that time?

A. The EIA patent policy has applied to patents even after the fact, those granted after the issuance of a standard. So, the policy applied directly -- the discovery of that IP information has always applied, before and after.

Q. Now, focusing again on the time period from late 1991 to mid-1996 -- and again, if your answer

differs for any subperiod during that time, please let me know.

A. Okay.

Q. During that time period, what steps, if any, did JEDEC take to inform members of the patent disclosure policy?

A. At every JEDEC meeting, every committee meeting, there would be review of the JEDEC patent policy. In every subcommittee, there would be a review of every -- of the JEDEC patent policy, such that every participant that was at all of these meetings could be made aware.

There were documents that were made available, the standards, the Manual of Organization and Procedures, that informed everybody about the patent policy. And in addition, the sign-in log, the sign-in sheet that everyone signs at every meeting when they come in to a particular meeting also reiterates that policy on the sign-in sheet itself.

Q. Let's take those one at a time, if we could, please.

I believe you mentioned presentations.

A. Excuse me?

Q. I believe that you mentioned presentations.

A. Yes.

Q. At the JC-42.3 subcommittee, again, looking at the time between late 1991 and mid-1996, who generally made those presentations?

A. Generally, during that period of time, it would have been Mr. Jim Townsend who would have made those presentations. He made presentations about the patent policy. He also distributed copies of it, as well as his notes about patents that he had been made aware of through the course of the work inside JEDEC. He called that his patent tracking list, which was a collection of IP that had been disclosed, applications, patents and things that -- perhaps IP that did not yet have any kind of number or whatever. All that was disclosed, and he called that the patent tracking list. That's what he called it.

Q. Who is Mr. Jim Townsend?

A. Well, Mr. Jim Townsend -- it's the late Mr. Townsend now -- he was a long-term participant of JC-42, actually one of the original members of JC-42.3, and he was chairman of a number of past groups, a number of committees and had -- and when Jim finally passed away, he was the chairman of the JC-42 committee.

MR. OLIVER: Excuse me, Your Honor, actually, before we move on, at this time, could I offer into

evidence CX-208?

JUDGE McGUIRE: Okay, Mr. Perry, any opposition?

A. This is meeting minutes from a JC-42.3 RAM committee meeting from September of 1992.

Q. What are meeting minutes from the 42.3 subcommittee?

A. Meeting minutes are copies of the highlights that take place in a committee meeting and the relevant actions that were taken. It's sort of where we keep the record of the decision-making process that takes place inside of JEDEC.

Q. Who prepares these minutes?

A. This would be a staff member from JEDEC, in this case it would have been Mr. Ken McGhee, M-C-G-H-E-E.

Q. Mr. Rhoden, if I could ask you just to flip through the first few pages of these meeting minutes, you'll see that pages 1 through 12 appear to be consecutive, if you will, then starting at page 13, there's an Attachment A, and the documents beginning at page 13 and going thereafter appear to be somewhat different.

Could you please explain the -- I guess could you please explain first what pages 1 through 12 consist of?

A. Yes, pages 1 through 12 are the -- is basically a chronological reference of what was taking place in

the meeting, and by reference, it will then refer to the rest of what's attached, which would be attachments of presentations that were made at the meeting. This is just a document of the highlights that took place in the meeting.

Q. When you said "this" in that last answer, you are referring to the 12 pages?

A. I'm sorry, pages 1 through 12 of the document would be the key decision points, motions and votes and the references to presentations would be documented in these things we call minutes.

Q. I note there are quite a few additional pages, appears to go to page 171. What do pages 13 through 171 consist of?

A. Yeah, pages 13 through 171 are copies of presentations that were made at the JEDEC meeting, at this particular JEDEC meeting, and they are referenced through the order presented in the previous 12 pages.

Q. Who prepared the various documents appearing between pages 13 and 171?

A. The preparation of the documents was handled by many companies, the many member companies that were involved. So, it's whoever was making a presentation would have been the preparer or their company or somebody else associated with them would have been the

preparer.

A JEDEC staff person takes care of the first 12 pages. The rest of these are pages that were created by member companies.

Q. So, in other words, each company making a presentation prepares its own attachment for their presentation?

A. That is correct.

Q. Is there always an attachment for a presentation?

A. Not necessarily. Almost always I would say. There have been times when people stand up and make -- have verbal discussions, and sometimes those unfortunately do not get reported.

Q. Okay. If I could direct your attention, please, to page 3 of CX-42 --

A. Okay.

Q. -- and specifically to item number 4. It reads, "Patent Issues. Chairman Townsend reported on the EIA patent policies and showed the patent tracking list (See Attachment A)."

Do you see that?

A. Yes, I do.

Q. Does this reflect Mr. Townsend's presentation of the patent disclosure policy that you described a

few moments ago?

A. Yes, this would have been one of Mr. Townsend's presentations about the JEDEC patent policy and his patent tracking list that he always made at the meetings.

Q. How often did Mr. Townsend give this or similar presentations?

A. He made this at virtually every meeting, certainly every meeting that I -- that I can recall.

Q. How frequently, if at all, do you recall sitting through Mr. Townsend's presentations?

A. Frequently, not -- perhaps not every time, but certainly many times.

Q. What do you recall Mr. Townsend saying in these presentations?

A. Mr. Townsend would reiterate the JEDEC patent policy. He would show examples, and by example with his patent tracking list, he would show a representation of the patent policy at work, if you will, to demonstrate to everyone that was there -- new, old or otherwise, whether somebody was first attending, people that had been there for a long time or otherwise -- just so that everybody in the room became completely aware of it.

Q. Do you recall whether Mr. Townsend ever made

any specific references to patent applications?

A. Yes, he did.

Q. Do you recall --

A. Yes, I do recall, and yes, he did make reference. I do recall that.

Q. Do you recall what Mr. Townsend said about patent applications?

A. Well, as I said, anything within the patent process is how it was explained, how I used to explain it, including everything involved in the creation of IP. Essentially, if you believe you have ownership for it, that's how he determined it. That's my understanding.

MR. PERRY: Your Honor, what I heard is that he switched to what he always explained in his answer, and I would move to strike that, and I think the question was about what he heard from Mr. Townsend.

JUDGE McGUIRE: I think his answer otherwise speaks for itself, Mr. Perry.

MR. PERRY: All right, thank you.

JUDGE McGUIRE: Overruled.

BY MR. OLIVER:

Q. Mr. Rhoden, just to be clear, I believe in your previous answer you explained the role of patent applications, if you will, in the patent process.

What, if anything, did Mr. Townsend say with respect to disclosure relating to patent applications?

A. Mr. Townsend would always make reference that disclosure was required of patent applications.

Q. Mr. Rhoden, let's talk a little bit more about the patent tracking list that I believe you referred to, if I could direct your attention to CX-42, Attachment A, page 13.

A. Okay.

Q. Do you recognize what appears as Attachment A on page 13?

A. Yes, I do.

Q. What is that document?

A. This would have been Mr. Townsend's presentation of the patent -- the patent policy and his patent tracking list.

Q. When you say "this" would have been his presentation, could you please identify which specific pages you're referring to?

A. Okay, let me see the -- starting with page 13 and continuing through page 17, so it looks like CX-42-13 through CX-42-17 would have been presentations and detailed discussion by Mr. Townsend about patents, patent policy, patent tracking list.

Q. Could I direct your attention, please, to page

16.

A. Page 16? Okay.

Q. It bears the caption Patent Issues to Track.

A. Yes.

Q. Do you see that page?

A. Yes, I do.

Q. All right. Do you recognize that document?

A. Yes, I do.

Q. What is it?

A. This was Mr. Townsend's personal notes about issues that had been -- he had become aware of through the disclosure about various IP relating to the work going on inside JEDEC.

Q. What, if anything, did Mr. Townsend do with this document?

A. He presented it and used it as an example for how the patent policy was at work, and he kept this list to distribute to everyone, to make companies aware of it and make new members aware that this was the policy, this was the policy at work.

Q. If I could direct your attention to the left-hand column that reads Patent Number, do you see that?

A. Yes, I do.

Q. And underneath that is the item 3,771,145. Do

you see that?

A. Yes.

Q. Do you have an understanding of what that number refers to?

A. Yes, this would -- this is actually a patent number for an issued patent.

Q. If I could direct your attention two lines further down on that same column, it reads "pending," and reading across that line, it reads, "pending, Fujitsu, VSMP, Fujitsu, 42.3."

Do you see that line?

A. Yes, I do.

Q. What does the word "pending" refer to in that line?

A. "Pending" refers to a pending patent application that had been disclosed. In this case, the holder was Fujitsu, and the disclosure was also Fujitsu.

Q. Now, is it your understanding that the document entitled Patent Issues to Track appearing at pages 16 and 17 of CX-42 lists all patents and applications that were disclosed during the 42.3 subcommittee up until this time?

A. I do not have that understanding. This, again, was Mr. Townsend's personal list, and I'm not sure that

everything was included in it.

Q. If I could direct your attention back to page 13 of CX-42.

A. Okay.

Q. A document that bears the title Toshiba American Electronic Corporation, and there's an address, phone number, fax number and appears to be a list of recipients.

Do you see that document?

A. Yes, I do.

Q. Can you please explain what this document is?

A. This first page was a fax list. Mr. Townsend prior to meetings would also send this patent tracking and patent policy issue, send out by fax to all of the people on the list that you see here.

Q. And do you have an understanding as to why Mr. Townsend sent this out to the people on the list?

A. I received this particular one, and yes, I received many other copies prior to being at meetings.

Q. Do you have an understanding of why Mr. Townsend sent this document out to the people on this list?

A. The -- Mr. Townsend wanted to make certain that all of the people who had any kind of leadership role inside of JEDEC had copies of it for themselves and for

their committees to distribute.

Q. If I could direct your attention to the beginning of the first paragraph of the text, it reads, "Please refer to the existing rules of the EIA governing patentable matters, which follow."

Do you see that?

A. Yes, I do see that.

Q. Do you have an understanding of the term "patentable matters"?

A. Yes, I do.

Q. What is your understanding?

A. As I said, anything that would be in the patent process. Essentially if you believe that you have ownership of a particular topic or a particular item, then that is what he's referring to. Patentable, whether a patent had actually been applied or not.

MR. OLIVER: Well, I'll try to do it in logical order this time, if I could now at this time offer into evidence CX-42.

JUDGE McGUIRE: Mr. Perry?

MR. PERRY: No objection.

JUDGE McGUIRE: So entered.

(CX Exhibit Number 42 was admitted into evidence.)ted into

icJUDGE McGUIRE: So enjT*fm*(16 wh tsring to. Patenta

Q. Mr. Rhoden, are you familiar with a so-called new member orientation at JEDEC?

A. Yes, I am.

Q. What does that refer to?

A. The new member orientation -- excuse me a moment.

The new member orientation inside -- in JEDEC was -- there were a number of things, one of which was a lunch that we would have at each of the JEDEC meetings, and it still continues even today, for new participants that attend JEDEC meetings, and they have the opportunity then to at this lunch participate in the lunch with other senior people within JEDEC, people who have been attending, perhaps chairmen, perhaps just long-term members, where they can ask whatever questions that they would like to ask about JEDEC.

And there was also an orientation about other activities to try to help people learn the function of the committees themselves, presentations, how you make presentations, the format of them, that sort of thing.

Q. Let me be clear about the time period. Focusing on the time period between late 1991 and mid-1996, did JEDEC conduct new member orientations during that time period?

A. Yes, Mr. Townsend was -- this was one of his

passions, if you will. The passion for the patent policy and the passion for helping new members. Since he was one of the original members of the JC-42 committee, he had an in-depth knowledge of the need to help new people coming in understand how and what was taking place. So, yes, this activity took place at I think almost every meeting.

Q. And was this activity conducted at the JC-42.3 subcommittee level?

A. Yes. Actually, it was conducted throughout the -- it would be a particular day or a particular day through the week, and as part of his patent tracking policy, often he would make other presentations to try to help people come up to speed and then offer the lunch and things afterwards to anybody who wished to have additional information.

Q. You referred to events during the week. Could you explain what you meant by that, please?

A. Oh, of course. The JC-42 committee, as I mentioned, is made up of multiple point committees, and the meetings would occur sequentially such that we all had the opportunity to attend each of the committee meetings. And so the events that I'm talking about are particular committee meetings. Some may take a whole day, some may not, and they would be sequentially

organized, much the same way -- we still do it pretty much the same way today.

Q. Just to be clear, you are referring to the meeting of the 42.1 subcommittee would occur, followed by the meeting of the 42.2 subcommittee?

A. It's not necessarily in order, 42.1, .2, .3, but certainly there would be a relationship of certainly the meeting of point committees. There would be a meeting of JC-42.3, that would some block of time. The meeting of JC-42.1 would be some other block of time. And all of these would be -- the reference that I'm using as these events would be committee meetings that would take place during the course of the time that we met for a few days or for a week.

Q. By the way, was there much common membership among the various pointed subcommittees within JC-42?

A. Quite a bit. I would not say 100 percent. That's one of the reasons that we made certain that we repeated the patent tracking throughout each of the subcommittees to make certain that everybody hadh of the

Q. Just to clarify for the record now, would it -- would it be logical to assume, then, that many companies or many individuals attending the 42.3 subcommittee might actually be in attendance at other 42 committee meetings for the course of a week or so?

A. Yes, that is correct. Many members still do attend every single point committee or at least the vast majority of them.

Q. How many 42 committee meetings are there per year?

A. Well, there are four regular meetings, once a quarter, and depending upon the workload for the committee, the amount of work that we have to do, we often times hold special committee meetings in between meetings, and so somewhere between four and eight. In times of high activity, we will have eight meetings per year and almost always have five. Four is a pretty rare occurrence.

Q. Was that also the case between late 1991 and mid-1996?

A. Yes, there were a lot of meetings during that period of time.

Q. By the way, looking again at late 1991 through mid-1996, approximately how many members were there in the 42.3 subcommittee?

A. The number of members, probably on the order -- when we talk about members, there are member companies. Many companies would send multiple people, so in a typical room would be, say, 50, 60, 70 people or so, but the number of member companies present would usually be somewhere around 40 or 50, something like that.

Q. Please correct me if I'm wrong, but would it be fair to assume from what you've just said that there might be 60 or 70 individuals attending meetings up to a week per time four to five times per year?

A. Yes, that is correct.

Q. Coming back now to the new member orientations, did you ever participate in any new member orientations?

A. Yes, on many occasions I did.

Q. And what was your role?

A. My role as a long-term member and sometimes chairman was to participate and help the new members in their understanding of what took place inside JEDEC.

Q. What, if any, discussion of patent issues took place at the new member orientations?

A. The patent issues would be reviewed to see if anyone had any questions, but by that time usually everyone had heard the patent presentation by Mr.

Townsend, perhaps numerous times. So, it would -- it occurred occasionally, but not often, with new members; only if they had any kind of questions, obviously.

Q. Mr. Rhoden, if I could ask you to find CX-306 in the pile in front of you, I believe it should be in the small pile. It should be a JEDEC sign-in sheet.

A. Okay, I've found it. I'm sorry.

Q. That's quite all right.

A. I'm trying to keep this straight, but it's a pretty big stack of papers. I'm sorry.

Q. This is a document that bears a number of seals across the top and underneath that reads Meeting Attendance Roster.

Do you see that?

A. Yes, I do.

Q. Do you recognize this document?

A. Yes.

Q. What is it?

A. This is a sign-in sheet, and you can see the JEDEC logo or the old logo at least in the upper left-hand corner and the EIA logo in the middle of the page. This is a sign-in sheet that we would use at every meeting. People would sign in here, and this would be transferred to the head of the minutes, would be from a sheet like this.

Q. Between late 1991 and mid-1996, do you recall signing a sheet similar to this?

A. Yes, every attendant would have signed something like this.

Q. Just to be certain I understand, I believe you said that the names are transferred from this sheet to the minutes. Is that correct?

A. Oh, yes. Actually, the people sign in, and then such that they are more legible, they are transferred from or -- transferred from this sheet then to the printed document, and you see at the head of all of the meeting minutes, the names that appear at the head of the meeting minutes would necessarily have signed a sheet just like this to be transferred to that point.

Q. Let me direct your attention to the first page of this document, please, and specifically to the caption underneath the box reading Committee Identification and Meeting Location but just above the columns where it says, Name (Please Print).

In that box it reads, "To all Participants: Subjects improper for consideration under the EIA Legal Guides shall not be discussed at this meeting or elsewhere, see Part 1, General Guides (reverse side). See Special Guides in Parts II and III for engineering

standardization and marketing date programs, respectively."

Then it continues, "Subjects involving patentable or patented items shall conform to EIA policy (reverse side). Consult the EIA General Counsel about any doubtful question."

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the obligation to disclose. The patent policy is very important to the operation of JEDEC, and so it's repeated as many places as essentially we could put it, here, the sign-in sheet, it's referred to in the meetings, put on all the documents.

Q. And then the final part that I read, "Consult the EIA General Counsel about any doubtful question," again, between late 1991 and mid-1996, would that reference also have been to Mr. John Kelly?

A. Yes, that would be to Mr. John Kelly during that period of time.

Q. Mr. Rhoden -- actually, strike that, please.

Your Honor, at this time I would like to offer into evidence CX-306.

JUDGE McGUIRE: Mr. Perry?

MR. PERRY: No objection.

JUDGE McGUIRE: So entered.

(CX Exhibit Number 306 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, if I could ask you to locate JX-54 in front of you, it should be the EIA Style Manual.

A. Okay.

MR. OLIVER: Your Honor, could I request --

THE WITNESS: I'm sorry, I'm having trouble

finding it.

MR. OLIVER: Could I request that one of our attorneys help Mr. Rhoden find the document?

JUDGE McGUIRE: Yes, that would be fine. Go ahead and approach.

MR. OLIVER: May I approach, Your Honor?

JUDGE McGUIRE: Go ahead.

MR. OLIVER: I apologize, Your Honor, if we could have just a moment to locate that document.

MR. STONE: Your Honor, is it a problem if while this is going on if I just leave and --

JUDGE McGUIRE: Oh, go ahead. Is this a good time to take a 10 or 15-minute break at this time?

MR. OLIVER: That would be fine, Your Honor.

JUDGE McGUIRE: Let's take a break. We will be back here at quarter until 12:00. We are in recess.

(A brief recess was taken.)

JUDGE McGUIRE: This hearing is back in order, and you may continue at this time, Mr. Oliver.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Mr. Rhoden, do you now have in front of you a document marked as JX-0054?

A. Yes, I do.

Q. It should bear a caption EIA Engineering

Publication, Style Manual.

A. Yes.

Q. Do you recognize this document?

A. Yes, I do.

Q. What is this document?

A. This is the style manual for publications created inside of EIA, EIA and also JEDEC, even though at this time EIA/JEDEC -- JEDEC was a part of EIA officially.

Q. How did you become familiar with this document?

A. This document is -- was provided to all the people that were part of any of the JEDEC committees, and I assume also for TIA and EIA, but I have no knowledge about that.

Q. Now, if I could direct your attention, please, to page 9 of JX-54. Towards the bottom of that page, there's a caption that reads 3.4, Patented Items or Processes.

Do you see that?

A. Yes, I do see it.

Q. If I could read a couple of sentences there for you. "Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program standardization shall refer to a patented item or process unless all of the technical information

covered by the patent is known to the formulating committee or working group."

Do you see that?

A. Yes, I do.

Q. Between late 1991 and mid-1996, did you have an understanding of that passage?

A. Yes, I did.

Q. What did you understand the term "no program standardization shall refer to a patented item" to mean?

A. As I referred before, the concept is -- of the policy is that once disclosure has been made of any IP, it is a requirement that discussion about that topic cease until the guideline as you see written here is actually met.

In other words, the holder of the IP provided the information, the technical information, and necessarily the letter stating their willingness to comply with the policy.

Q. If I could continue reading that passage, it continues, "and the committee chairman has received a written expression from the patent holder that one of the following conditions prevails: 1, a license shall be made available without charge to applicants desiring to utilize the patent for the purpose of implementing

the standard, or 2, a license shall be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination."

Do you see that?

A. Yes, I do.

Q. Again, between late 1991 and mid-1996, did you have an understanding of that passage?

A. Yes, I did.

Q. What was your understanding at that time of the term "unfair discrimination"?

A. Well, essentially unfair discrimination would refer to -- it -- perhaps it's better if I state it in this way: It is a requirement that all people be able to use the standards as they're created, and so unfair discrimination would be if people were prohibited for whatever reason from actually using or implementing a standard that was created, so that's why this was a requirement at that time.

Q. Between late 1991 and mid-1996, under what circumstances, if any, would JEDEC members have included a technology for standardization if they understood in advance that the technology would not have been offered to everyone on a non-discriminatory basis?

A. There is no case --

MR. PERRY: Excuse me, Your Honor, I would like to object. I think that was calling -- lacks foundation and calls for speculation unless we're talking about his own understanding.

JUDGE McGUIRE: Overruled.

Sir, if you have any answer to that question, you may go ahead and answer.

THE WITNESS: Yes, there is no case where the patent process would have been included in a standardization process if it was known and if the IP holder was not willing to provide it on free or nondiscriminatory terms. That would not happen.

JUDGE McGUIRE: What is JX-28 that we're referring to now?

MR. OLIVER: JX-28 is a set of the minutes from the December 1995 meeting of the JC-42 --

JUDGE McGUIRE: As opposed to what we talked about earlier between the parties as being a joint exhibit, is that -- I just want to be sure there's no confusion here.

MR. OLIVER: This is one of the joint exhibits that we have identified as JX --

JUDGE McGUIRE: Okay, but it hasn't been offered up until this point, is that correct, because I know we had the agreement, and that agreement has been vacated as of this morning, so I just want to be clear so we know where we're headed.

MR. PERRY: This is a separmor)his is a sepoof, You so we21now wheit*(there.) thiltim a ly withgrey o

actually the practical requirements of remarking everything means that we're ever going to have any more JX, just because the courtroom is full of RX and CX.

JUDGE McGUIRE: Okay, I understand.

(Discussion off the record.)

JUDGE McGUIRE: Okay, can we comment on that? Have these been offered and entered through this point either through agreement of the parties that is not included in the April 29th agreement, but was there an earlier agreement through the parties that these should be entered into evidence?

MR. PERRY: There was an earlier agreement that there would be no objection made if they were offered. I don't believe we discussed that they would all come in at once.

JUDGE McGUIRE: Right, and I am not asking they all come in at once, but I guess at some point, then, if you are going to have this offered, then it needs to be offered, right, and then there will be no opposition, I assume.

MR. PERRY: Correct.

JUDGE McGUIRE: Because this is not -- as of this time, it hasn't been offered. You may have an understanding, but it hasn't been offered.

MR. OLIVER: Okay.

JUDGE McGUIRE: Okay?

MR. OLIVER: Yes, thank you, Your Honor.

With that in mind, at this time, we would like to offer JX-54 for admission into evidence, please.

JUDGE McGUIRE: Mr. Perry, any objection?

MR. PERRY: No objection.

JUDGE McGUIRE: If not, so entered.

(JX Exhibit Number 54 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, do you have JX-28 in front of you now?

A. Yes, I do.

Q. Do you recognize this document?

A. Yes, I do.

Q. What is it?

A. This document is JC-42.3 DRAM committee meeting minutes from December 1995.

Q. If I could direct your attention to page 49 of JX-28.

A. Okay.

MR. OLIVER: Excuse me one moment, Your Honor, please.

(Brief pause.)

BY MR. OLIVER:

Q. My apologies, Mr. Rhoden, if I could actually ask you to set that document aside.

A. Okay.

Q. And instead, if you could please locate JX-59.

A. Okay.

Q. This should be a small document bearing a JEDEC caption at the top and seals at the top.

A. JX-59?

Q. Yes.

A. Okay, I have it.

Q. Okay, JX-59 is a document, it says JEDEC Solid State Products Engineering Council at the top with seals on the left and right-hand side.

Do you see that?

A. On the right-hand side? Yes.

Q. The seals on both the left and right-hand side of the caption?

A. Yes, I do.

Q. And then a few line downs, it says, "Committee ballot, JC-42.3-92-85, item number 376.3."

Do you see that?

A. Yes, I see that.

MR. PERRY: Your Honor, I didn't seem to get that, if I could just look at it or get another copy.

MR. STONE: I have it, Mr. Perry.

MR. PERRY: I have got it. Thank you.

JUDGE McGUIRE: Go ahead.

BY MR. OLIVER:

Q. Mr. Rhoden, do you recognize JX-59?

A. Yes, I do.

Q. What is it?

A. This is a committee ballot from the committee.

Q. What was the use of committee ballots?

A. This is -- when we would be heading down the process of making decisions inside of JEDEC, this would be one of the steps that would be involved in that process. We would issue a committee ballot.

Q. If I could direct your attention to page 2, please.

A. Page 2, okay.

Q. And if you see, starting about a quarter way down the page, there are some blank lines to the left-hand side with writing to the right. Do you see that?

A. Yes, I do.

Q. And about five lines down, there's a blank line, and next to that it reads, "If anyone receiving this ballot is aware of patents involving this ballot, please alert the Committee accordingly during your voting response."

Do you see that?

A. Yes, I do.

Q. Do you recall seeing language of that sort on ballots between late 1991 and mid-1996?

A. To my knowledge, I think I've seen this on every ballot that I've ever looked at.

Q. Between 1991 and 1996, did you have an understanding of the language that I just read?

A. Yes, I do.

Q. And again, based on your understanding between 1991 and 1996, what was your understanding of the language that I just read?

A. This is the reiteration of the JEDEC patent policy requiring disclosure of any IP relating to work going on in reference to this particular matter.

Q. Between 1991 and 1996, was it your understanding that this marked the point in time at which an IP holder was required to disclose?

A. No, it was not. My understanding always was as early as possible. That's the way it has always been stated and the way we have always used it. You are required as soon as -- as soon as you have knowledge of a discussion taking place, a presentation, discussion, ballot, whatever, as soon as you become aware that a topic is being discussed for which you know that there

is IP, you are obligated to disclose.

JUDGE McGUIRE: Can we ask -- let me interject just for my edification here. When you're talking about any IP, just for the context of your testimony, what are you talking about?

THE WITNESS: When I'm talking about IP, Your Honor, I'm talking about anything for which a patent could be applied, is applied, is granted, anything within the realm of the patent process as we've referred to it many times. Our process has always used the term "patent" to apply to the patent process, if you will.

JUDGE McGUIRE: Okay.

MR. OLIVER: Your Honor, at this time I would like to offer into evidence JX-59.

MR. PERRY: No objection.

JUDGE McGUIRE: So entered.

(JX Exhibit Number 59 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, I'd like to shift gears somewhat now and focus on the work of the JC-42.3 subcommittee during the early 1990s.

Could you explain in very general terms what standardization work the JC-42.3 subcommittee was doing

in the early 1990s?

A. Well, a number of things, but perhaps one of the most significant things that we were involved in at the time was the development of the standard for what is now known in the industry as Synchronous DRAM.

Q. Why was the JC-42.3 subcommittee working on a standard for Synchronous DRAM?

A. Well, as I stated before, the user community

A. Well, yes. Perhaps it would be helpful if we used -- I think there are some demonstratives that also reference this, basically the inside cells of the memories themselves.

Q. Okay.

MR. PERRY: Your Honor, I am going to let Mr. Detre sit in my spot while we deal with this, pursuant to what Mr. Stone was talking about the other day.

JUDGE McGUIRE: That's fine.

MR. DETRE: Thank you.

BY MR. OLIVER:

Q. Mr. Rhoden, what does this first demonstrative show?

A. I'll try my best not to put anybody to sleep. I know engineers have a tendency to do that.

The -- this is the fundamental cell, and by cell, it's sort of the lowest level piece of a DRAM, a

transfers that voltage that is on that capacitor, either high or low, to the vertical line that you see, which is called the bit line, sometimes called column, sometimes called bit line, and that is the fundamental operation of a memory cell.

Now, if you go to the next demonstrative, not to give you a headache, but what you see is this is -- it's an X/Y array. By X/Y, I mean it's a two-dimensional array, where the horizontal lines are those same row lines that you saw in the previous demonstrative, and the vertical lines are the column lines or the bit lines that you saw in the previous, and in every location.

Now, you can think about this in terms of a device that has a million storage elements, there would be a million of these cells. Obviously we don't have room for a million on the display.

Q. Focusing on the time period of the early 1990s just very, very roughly now, what magnitude of the number of cells would have been contained in memory at that time?

A. Along back in the 1990s, we were working on -- in and about that time, relative, about 16 million -- 16 megabits, which is -- a megabit is a -- it's a power of two, so it's not quite a thousand. It's 1024. So,

it's a little bit more than 16 million bits of information would be the level that we would be working at at that time.

Q. Would that mean roughly 16 million cells in a -- in memory?

A. Yes, it would.

Q. Mr. Rhoden, how does -- how does a system get information into and out of the memory cells?

A. Well, the -- you have the cell array here, and then this must be connected to the outside world in some way, and if you go to the next demonstrative, we can show a little bit about -- this is a representation of that same array. The X/Y dimension's still the same, the same row lines and the same bit lines or column lines, as they're called in the array.

Now, connected to that, we have to apply some address, and there's two types of address. Since we have a two-dimensional array, we have something that we need to apply that would be the row address and something that we apply that would be the column address, and you can see that connected to the outside world that we saw before, we have the address lines, and those address lines inside the device are translated into a row address location and also a column address location, and each of those is

independently captured, if you will, by a strobe line.

So, there would be a strobe line, we refer to it as, row address, strobe, clock, whatever you like, that would capture the row address, at which time the address information could change to a different address, and then there would be another line that would be a column address strobe or column clock as is often the case, and that would be used then to capture the information into the column address.

So, the row line would then highlight something -- and I can show you the operation here. What has to happen is when the row address comes in, it will highlight a row line or word line, and remember, this is going parallel across that array, so you have a parallel array of all of these transistor cells, if you remember the first cell that we looked at. Those are then -- information is placed out on the bit lines, column lines, and those are captured in the sense amplifier.

Now, the sense amplifier, the name that you see there, the terminology, is sensing the voltage. So, you're trying to sense whether there was a high voltage or a low voltage for each of those column locations.

And then finally, if you are trying to access this information, you provide the row address, as you

see highlighted there. Then the column address will transfer everything in that row down to the sense amplifiers. The next operation would be the column address that would come in and pinpoint a particular location in the sense amplifiers, and you would enable that, and that would become the definition of the X/Y physical location for a given location in memory.

And then on a read, this would then be broadcast out the device in the sense of data out. So, what I've just walked you through here is a simplified description of the read operation of a memory array.

You have the array, the row address, column address, sense amplifiers and then data that goes out.

Q. Okay, thank you.

A. I hope I didn't put anybody to sleep.

MR. OLIVER: Your Honor, at any point during this discussion, I invite you to ask any questions that you --

JUDGE McGUIRE: Sure, I won't hesitate. I will do that.

THE WITNESS: Okay.

BY MR. OLIVER:

Q. Is it possible to back up the slides and run through that one more time, please? We are going to try to go through this one step at a time, if you could

bring up the next slide. Then I believe the next slide after this, there's a horizontal red line that appeared.

Again, what does that red line refer to?

A. The red line would refer to -- the row address would have been captured at that point in time, and the row address, once it is captured, it would apply an enable voltage, if you will, on the row line that we saw for the cells that connected horizontally across there, and that would enable all of the transistors that would transfer the bit information in the cell out to the bit line or column line.

Q. Okay. Then the next demonstrative, I believe, showed some green lines that were between the horizontal red line and the sense amplifier.

A. Yes.

Q. Could you please explain what's represented by those green lines?

A. Yes, this would be the transfer of this information. Once a row line has been enabled, then the transferred information would occur onto the bit lines, and those bit lines then would be transferred into the sense amplifiers, and it would sense the voltage and make the decision whether to capture a zero or one, because high voltage and low voltage, you

designate a one or a zero.

Q. By the way, are you familiar with the term "RAS," R-A-S?

A. Yes, I am.

Q. What is RAS?

A. RAS is the row address strobe. It would be -- it's often been referred to as the row clock. It would be the signal that would actually capture the row address into this row address element that you see at the side of the array, the left-hand side of the array.

Q. Okay. Now, once the data is on the sense amplifiers, what happens next?

A. Well, once you have data on the sense amplifiers, it's necessary to select which of this parallel large block of data that you're trying to capture, either to write it or to read it, either one, and you highlight that by applying a column address, and a column address then highlights, as you see in the demonstrative here, the particular locations -- the particular sense amplifier, that's what they're called, that would pick a particular bit.

We have an X/Y array, and we pick a row of them, which is a horizontal series of them, and from that we pick a particular one. That's the basic operation.

Q. It's a bit difficult to see from here, but it looks as though there's a red line between the column address block and the sense amplifier block?

A. Yes.

Q. What does that red line depict?

A. The column address would be a column address decoder, if you will. It would be an address that would be applied that would select a particular line.

Q. And I also see a red circle on the sense amplifier. What does that represent?

A. That means that that particular sense amplifier has been enabled to connect that sense amplifier to the data output lines of the device.

Q. Okay. What is the next step in a read operation?

A. In the read operation that's shown here, the next step would be that data is connected to the data output lines, and the data then goes out of the device. The only difference between a read and a write is exactly the same operation, except the data goes in the opposite direction.

Q. I'll follow up on that in just a moment.

A. Okay.

Q. First, you say the data goes out. Where does the data go to?

A. The data would go then out onto the memory bus, the interconnection, if you will, between the device itself and the memory controller.

Q. Can you explain in a little bit more general term what a write operation is?

A. A write operation -- remember, I explained DRAM itself is just a scratchpad. It's a place where you are going to store information, and then you are going to later go back and retrieve it, and the write operation is the operation that actually takes information from within usually the CPU, but it could originate anywhere, it could be -- it's information that's in the computer that you wish to store for later use.

So, you take that operation, you do -- follow much the same process that we just described, and the data comes into the DRAM device and is stored in a memory cell.

Q. And in general terms, what is a read operation?

A. And a read operation is the reverse of that, which would be the retrieval of that same information that you previously stored.

Q. Mr. Rhoden, are you familiar with the concept of asynchronous memory?

A. Yes, I'm familiar with the term.

Q. What is your understanding of asynchronous memory?

A. Well, asynchronous memory is a term that has been used to describe memory organized much the same that you see right here where the information about row address, column address, they're actually clocked in with a row clock and a column clock that we call RAS and CAS, but those blocks are not continuous free running. By that I mean they do not continue in a periodic fashion. These would be applied only when necessary or when required.

Q. Mr. Rhoden, you actually referred to the term "CAS." What does that mean?

A. CAS is the partner, if you will, to what we previously described as RAS, and that would be the column address strobe, also known as column clock sometimes. The column address strobe is that control information that provides the captured -- the request to capture the column address into the column address location that you see on the drawing here.

Q. Just to further clarify RAS and CAS, when, if at all, in this diagram would the row access strobe be involved?

A. The row access strobe would be involved in the row address.

Q. In other words, at the time the row address is sent to the memory?

A. That is correct.

Q. And when, if at all, would the column access strobe be involved?

A. It would be involved at the column address, which would be the column address strobe, the column address at the bottom of the page there.

Q. By the way, these demonstratives have depicted identification of a row address followed by identification of a column address. Did it ever happen the other way around? Did it ever start with the column?

A. Well, I'm sure it has happened for some engineers, but that's not the normal operation of the device. That would be a mistake, I'm afraid. You have to enable the row before you can actually access the column address itself.

Q. Could one assume from that that the row access strobe would fire before the column access strobe?

A. Yes, in normal operation of the device, that's correct.

Q. Mr. Rhoden, you've described asynchronous memory. Are you familiar with the concept of Synchronous DRAM?

A. Yes, I am.

Q. What does Synchronous DRAM mean to you?

A. Synchronous DRAM actually brings an additional signal onto the device to actually gate information. It is merely a clock to break up the access into periodic time elements. By that I mean small sections of time. I think we may have a demonstrative even of that.

MR. DETRE: Your Honor, for clarification, perhaps when we're talking about Synchronous DRAM we could just clarify whether we're talking about Synchronous DRAM as developed at JEDEC or the general category of Synchronous DRAM.

JUDGE McGUIRE: Can you answer that, Mr. Rhoden?

THE WITNESS: Well, as I explained, the term that's used in the industry that we call asynchronous just applies to this block that you see here. The row and the column are both clock, and so in a sense, they are -- by technical definition, they are synchronous devices.

However, we have used the term when you apply a continuous free running clock into a device, that also in the terms of the JEDEC definition is when we have called it synchronous, SDRAM.

JUDGE McGUIRE: Does that clarify it for you, Mr. Detre?

MR. DETRE: Partially, Your Honor. I mean, I think as you heard yesterday, there is something that was developed in JEDEC called an SDRAM, which stands for Synchronous DRAM and refers to a specific device, and then there's the general concept of synchronicity of DRAMs.

JUDGE McGUIRE: So, what's your question now? Are you asking him if he's talking about only that that applied to the JEDEC, or in general?

MR. DETRE: That's the question, and I'm not sure that Mr. Rhoden made that clear.

JUDGE McGUIRE: Can you answer that in a very cogent style?

THE WITNESS: Well, I'll try.

As I said, in textbook definition, all of these memories that we're talking about are synchronous; however, when we talk about applying a single continuous free running clock, we are talking about the JEDEC definition of an SDRAM, okay?

JUDGE McGUIRE: That's fine.

Go ahead, Mr. Oliver.

BY MR. OLIVER:

Q. Mr. Rhoden, you referred to a clock. Are you

familiar with the term "system clock"?

A. Yes, I am.

Q. What does a system clock refer to?

A. A system clock is typically the clock found on the motherboard that all elements of the computer would operate within. So, they would be timed from the system clock, whether it be the DRAM, the micro -- the memory controller, the CPU, they all have some basis in the fundamental system clock.

Q. Do all operations occur at the same time?

A. Certainly not. There is a -- in the DRAM, we just talked about a sequence, and so there are a sequence of operations that occur at -- in periods of time, sequentially, some things in parallel, but most operations occur in some sense of sequential operation.

Q. Can you explain how a write operation transpires in connection with a system clock?

A. Yes, I -- that's the -- the write operation -- perhaps there's a demonstrative that might help us here.

We have in this particular picture, kind of to refresh what we had before -- in a way we're all like DRAMs, because we all need to be refreshed a little bit -- so the refresh is the same clock lines, control lines, address lines and a representation of some data

lines here between a memory controller and a single device, and we use this for demonstrative.

This is the same memory bus that we showed before connecting the memory controller and that memory module that we used earlier, okay? And under the pin names and definitions, you see exactly what we're -- the clock and CAS -- excuse me, chip select, RAS, CAS and finally write enable.

Q. Mr. Rhoden, would it be fair to say that this document is somewhat simplified for the audience?

A. This diagram has been extremely simplified to try to make it easily understandable for an audience such as this.

Q. Do you think the demonstrative is helpful to explain the basic concepts?

A. I think it is, yes.

Q. Could you use this demonstrative to explain how the write operation occurs with a system clock?

A. Yes, the write operation would -- let me first give you an explanation, and then I think we have some animation that will show it.

First what would happen is we get the row address, followed by a column address with data, and that's how the write operation would occur. Would you like to see a demonstration of that or is that -- is

that sufficient?

Q. One second, please.

A. Okay.

Q. I'm sorry, Mr. Rhoden, could you please explain how the write operation works?

A. Okay, the write operation itself would be -- some information would go across for the RAS line -- okay, here's a demonstration of exactly how a write operation would occur in the industry standard SDRAM.

Coincident with the clock, you see signals that are the chip select and the RAS line from the control signals on the left, in the BL. In addition to that you see in the red, which are the address lines remember, the address, which it would be -- say that that is the row address. So, row address corresponds to the chip select and RAS, and if we -- I think this will animate so we can show that we are first sending this across, and you will see that we have a burst length of four.

And followed by the RAS -- so, now the SDRAM has captured information from the row address, and a couple of clock periods later or so, we would get information that would come coincident with the column address, and if you could stop that for a moment, as soon as it gets here -- right there.

Now you see that the control lines are slightly different than before. You see, once again, the chip select, and this time it's not the RAS line, but it is the CAS line that's asserted, and also the write enable, to say that this is the column address, and it's also a write. So, the column address along with the write. I have the column information that's accompanied with this. I have -- also, in this case I have the data that's coming across on the data line. Since it is a write, I'm sending data to the SDRAM rather than retrieving it from.

And you can continue this, and you'll see what happens, it goes ahead, and now this is data that goes into the SDRAM that would subsequently be stored into the cell.

Now, because this is a burst length of four -- if you will stop it for a moment -- this also indicates a burst. You will see this is SDR write, burst length of four underneath the subheading underneath Synchronous DRAM. SDR write, burst length of four, also has a continuous burst of data that's followed, which would be four groups or four columns of data that would come coincident with a single address.

And so if you run that, you can see, you had the first one that has already gone, you have the

second one, and each one of these would correspond to a clock edge that comes into the device, and you see now the third, and ultimately you'll see the fourth as well.

And this has been slowed down by about a billion to one, so you get some concept of how fast this is happening.

JUDGE McGUIRE: Thank you for that, how fast it happens.

THE WITNESS: Okay.

BY MR. OLIVER:

Q. Mr. Rhoden, you just covered an awful lot in that description.

A. I'm sorry.

Q. It's very helpful, but you did cover an awful lot. Could you perhaps break it down piece by piece?

First, once again, the blue line that we see at the top is the clock line. Is that right?

A. That is the clock line, yes.

Q. Okay. Now, we've seen a square figure moving from left to right across that blue line.

A. Yes.

Q. What does that refer to?

A. The square figure moving from left to right is just a -- it's a pictorial representation that the

clock is actually traveling in that direction.

Q. Are you familiar with the term "edge" of a clock?

A. Yes, and this is -- as you see here, this is an edge. As a matter of fact, this is what we call the rising edge. The rising edge would be the one where it transitions up, versus the falling edge where it transitions down.

Q. When you say transitions up, transitions from what up to what?

A. Oh, okay. In all of the signals that operate within the computer, the typical interface is between voltages, and so in the clock line here, this would be from a low level voltage to a higher level voltage, perhaps near zero, perhaps near three volts. The actual voltage is not important. It's from a low level voltage to a higher level voltage is how we describe the transition. So, if I'm transitioning from a low voltage to a high voltage on a particular signal, that's how I determine the rising edge, and the edge is when that condition occurs, but once it's high, it's stable, and once it's low, it's also stable, but at the transition, the transitions are the ones that are important to us.

Q. Now, you also referred to an SDR. What does

that mean?

A. SDR is just an industry acronym that we use for single data rate. So, the clock is actually going to have a piece of data for every clock period. So, it's a single rate as it refers to the clock period itself.

Q. Now, I believe you said that all operations take place in time with an edge of the clock. Is that correct?

A. That is correct.

Q. Now, in SDR, do operations take place in conjunction with the rising edge or the falling edge or both?

A. In SDR, the operations take place in terms of the rising edge of the clock.

MR. OLIVER: I propose to run the demonstrative one more time. Do you have any other questions you'd like to ask before we do that?

JUDGE McGUIRE: No, you're doing fine on that point, so no, but go ahead and run it again.

BY MR. OLIVER:

Q. Okay, if we could perhaps run the demonstrative one more time, and again, if you could explain what is happening as we see it.

A. Okay, you can see the row address along with the rising edge of the clock and the row address

strobe. There's a time period later, some time period that you will apply the column address, and the time period later in this particular representation appears two clock cycles later.

And along with that, you see the rising edge and the column address, and the column address comes coincident with the data also for the first piece of data. And then on every subsequent rising edge for a burst length of four, you see data that continues across the device, from the controller into the DRAM itself.

Q. And that's what we see here as the rising edge?

A. And that's what you see. You're seeing write data transition from the memory controller into the SDRAM itself.

Q. And that was just defined by --

A. And I think you will have one more. So, this should be the fourth piece of data in burst that goes across. Now, in a real time system -- viewing this, you have to, in order to be able to see it, you have to capture it such that you can view it after the fact, because this is happening literally billions of times, very quickly.

Q. Now, you've also referred to burst length.

A. Yes.

Q. Could you explain again, please, what that means?

A. Yes. Actually, the burst length itself -- you 4ctua

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the read operation is the same in terms of the address and control, with the single difference being that we're performing a read instead of a write, and so we won't indicate that by the write line, and that's appropriate.

Would you like to play it so you can see it at this time?

Q. Yes, please.

A. Okay, you see here the read is the same -- the row address part is exactly the same, followed by some period of time later, and I'll ask you to stop it when the column address shows up here in a moment. And in the read operation, what's different is the control information -- if you'll stop that for a moment. You see here that we have that same chip select, we have that same CAS, the same column select line, the same rising clock and the same column address.

There's two things that are different here compared to the read -- excuse me, compared to the write. The read is different. And first of all, you'll see the final control signal that's listed here, which is the write enable signal, is not asserted, and since it's not asserted -- if it's asserted one way, it's a write. If it's asserted the other way, it's a read. So, in some senses, people call this the

read/write line. We just call it the write enable line, but there's a long history for why you select particular signals.

But what's different in addition to that, there's also no data, because remember, we're trying to read data, so the memory controller does not have knowledge of what data it wants. It is making a request now of the SDRAM. So, if you'll continue this, you can see -- but before you continue it, let me draw your attention, up underneath Synchronous DRAM, you see an SDR - read, burst length of four, same as before, and you see the terminology that says CAS latency of two, and CAS latency of two is an indication of when the data will become available at the output end.

So, CAS latency of two will say how long do we wait after we send the command before we can expect to start seeing data on the bus, okay? So, if you continue it, you will be able to see that. So, now, the request has gone into the SDRAM, and so I'm going to wait a couple of clocks later before I can expect that I will see data coming back to the memory controller, and you'll see, as this edge arrives, you see data coming back, and if you stop it there, you will see that the data is back right as the clock is arriving, the point being that's your two clock

periods.

Now, if you continue, you'll see the same thing you saw before, except the data now is going in the opposite direction. For the write, it goes from the

perhaps you could just identify for us the beginning of the first, the second, the third clock cycles, et cetera.

A. Okay. So, you see here, this is the first clock cycle, and we now have a clock that's low, and so we're now in the middle of the cycle as the clock is transitioning to low, and now we will have the beginning of the next clock period, so we have a full clock period that's transitioned at this time. And we are going to see one more clock period where transition is low and then back to high --

Q. And then we have number three here?

A. Only two, two so far.

Q. Would this be the third -- the beginning of the third clock cycle?

A. This would be the beginning of the third clock cycle, that's correct. And then this would be the beginning of the fourth that you're seeing here in a moment. And at the beginning of the fifth is when you would expect to see information out on the bus that comes back. So, that's at the beginning of the fifth is when it is broadcast on.

Now, obviously these lines are moving in real time, and the illustration is set up so you can see the direction of flow. You cannot see this operation with

the naked eye. You need some kind of demonstrative or some kind of tool to help you see this, but this is exactly what's happening inside all of these computers right now.

Q. Now, could you please explain CAS latency one more time in the context of this moving animation?

A. Yes, and CAS latency is that period of time from when the column address arrives at the SDRAM and when the data shows up. It's a relative number that says if it's two, then there's basically two periods of clock before the data becomes available. If it's three, then there would be three periods of clock. And period, remember, is a rising and a falling, so you get both. So, CAS latency two or CAS latency three would appear -- would represent full clock cycle differences, okay?

Q. In other words, an example such as this with CAS latency two --

A. Yes.

Q. -- if the column address information was sent at the beginning of the third clock cycle, then the data would arrive back at the beginning of the fifth clock cycle. Is that right?

A. That's the general way to look at it, yes.

Q. Perhaps we could run this one more time, and

then if you could perhaps explain that latency period as it transpires.

A. Okay, so we see the row address, followed -- now, this one also shows, it's a couple of clock cycles later, where it went between the row address and the column address, but that has no relationship to CAS latency. CAS latency is strictly the relationship between the column address and the data, not the relationship between the row and column address.

So, from this period of time, you can count two clock cycles until you can expect to see data back at the controller itself. And so you see a full period go to the device, and in the -- toward the middle of the cycle is where the data comes out and actually arrives at the controller at the time that you see the information being -- the clock transition there. So, that is a two clock period transition.

And after that, the data arrives every clock cycle, once per clock cycle for a single data rate. That's a term I'm sure you'll use a lot.

Q. I believe that we also have a demonstrative that would show a CAS latency three.

A. Okay. Now, this is the same type of thing, and you'll notice that the first part of this is going to be exactly the same. So, if we run this demonstrative,

you will see that row address goes in the same time frame that it went before, and then column address is going to go in the same time frame that you saw before. Okay, go ahead and run it.

So, row address transitions on a clock edge, and in our representation, a couple of clock cycles later is when the column address -- this is pretty typical for a system. Now, the column address does not have to be two cycles later, it could be more or in some cases even less, but after I arrive with the column address, then we will have CAS latency of three. We'll predict how long it is between the arrival -- now, stop it for a moment.

Now, this edge is going to initiate something inside the SDRAM, and inside the SDRAM, what you're going to see is the initiation for how long it takes now for the data to come back out. What we saw before was two, so this time you can count to three, and if you get longer than -- the CAS latency would just get longer, longer or shorter. So, go ahead and continue.

You see latched here, and if you count clock periods, so we now have for midway through, and all the way through one period, and we will go through a second period. This is a CAS latency two.

Q. Ah, okay.

A. Okay? Sorry, there is a mistake in the demonstrative. I'm sorry about that. So --

Q. So, if that were truly a CAS latency three, there would have been one additional clock period --

A. That's right, there would be an additional clock cycle before you saw information. I --

Q. Okay. Now, do we have a demonstrative that would explain a burst length of eight?

A. Yes, burst length of eight would be the same kind of thing, except you're going to have eight pieces of data, and I think you also have that if you'd like to see it.

JUDGE McGUIRE: I'm not sure we have to go through that at this point.

THE WITNESS: Okay.

MR. OLIVER: Okay.

THE WITNESS: You have -- oh, sorry. Any questions, I'd be glad to go through them.

JUDGE McGUIRE: I don't have any at this point.

THE WITNESS: Okay.

BY MR. OLIVER:

Q. Okay, Mr. Rhoden, are you familiar with the concept of a dual edge clock?

A. Yes, I am.

Q. What does that refer to?

A. Well, the concept of dual edge clock is, as we described, the clock itself has two edges, the rising edge and it also has a falling edge, and there's a concept associated -- a dual edge clock, all clocks are dual edge clocks. Now, if you take dual edge clock and add something else to it, then it may mean something.

Q. Are you familiar with the concept of DDR SDRAM?

A. Yes, and in DDR SDRAM, the dual edge clock -- the difference between the single data rate and the double data rate is strictly at the data level. Data actually transitions on both the rising edge and on the falling edge of the clock itself, and that is representative. So, you have a dual edge clock.

So, instead of transitioning -- data transitioning once per clock period, as we talked about before, you now get data twice per clock period. You get it on the rising edge and on the falling edge. So, you get two data phases or two pieces of data for every clock you go through.

Q. And do you have a demonstrative that shows that?

A. Yes, I believe we do have a demonstrative of that. Back up, you had it right. One more time. No? There.

You see here that the Synchronous DRAM's double

data rate, everything about it is essentially the same. In fact, all of the control is the same, because the same -- the control itself operates in the same way. You'll notice on the left there is an additional signal, and that's the DQS. The DQS is actually going to tell us the timing of what's going on on the data line itself. It's a strobe to indicate the -- when data is actually -- it travels with data, so it's a clock, if you will, of the data itself.

Okay, I think you can run this. What you will see is -- except I think -- can you halt this for a moment? I think you need to advance the slide one more time so you can see the relationship of DQS. So, go back -- oh, go ahead and cancel the animation, if you will and advance one foil until we have -- no? Okay,

MR. OLIVER: Your Honor, any questions about dual edge clock for --

JUDGE McGUIRE: No.

THE WITNESS: I'm sorry if I put anybody to sleep.

JUDGE McGUIRE: I'm sure there are questions, but I'm not prepared to ask them.

THE WITNESS: Okay, I'm sorry.

BY MR. OLIVER:

Q. Mr. Rhoden, are you familiar with the concept of programmable burst length?

A. Yes, I am.

Q. What does programmable burst length mean?

A. Programmable burst length would indicate that you could selectively change the length of the burst inside a device through a number of ways, perhaps using a register inside the device.

Q. Do you have any demonstratives that would help illustrate that?

A. I believe there are some demonstratives here that have -- that can show us where the register might be. If we look here at burst length, you see the same basic operation, that the DRAM itself hasn't changed in a lot of years, and if you go with the programmable burst length -- perhaps go to the next one.

Yes, what you can see here is that there is a mode register in the upper left-hand corner, and the mode register itself would contain information, and that information would indicate what the value -- what the length of the burst would be.

There's some circuitry that's also referenced there, probably a little difficult to see in the blue, as to how the burst might actually function, but the key thing is that you would be able to change the length from two to four to eight merely by changing the data in the register device itself.

Q. In a typical system using an SDRAM, how frequently would that system change the burst length?

A. Probably never. Most I would say typical systems never change it.

Q. Mr. Rhoden, are you familiar with the concept of programmable CAS latency?

A. Yes, I am.

Q. Can you please explain what that means?

A. I think we also have a demonstrative to show the same thing. It's going to look very much the same as the other, because it's in effect in the SDRAM exactly the same register. It's merely different bit locations within that same register, and the programmable CAS latency changes the amount of time

between when data is requested and data is applied at the output or received at the controller, and the same kind of thing operates here.

We have programming and changing. You can go from -- the typical SDRAM is a CAS latency of two or three. Other values have existed.

MR. OLIVER: Could you give me one moment, please, Your Honor?

JUDGE McGUIRE: Sure.

(Brief pause.)

BY MR. OLIVER:

Q. Mr. Rhoden, I believe that you said earlier that the various diagrams that we've been looking at are somewhat simplified, shall we say?

A. Oh, overly simplified in some respects, but the point being that they're very simple, to where you can actually understand the operation. That's the main point.

Q. There's another demonstrative that's on the screen now. Can you please explain what this demonstrative shows?

A. Yes, this demonstrative is an indication of a little higher level, a little more complex drawing, although still very simple, where you have those same control, clock, address lines connected to memory

modules now, because in a real system, you would be using modules rather than individual devices in a typical case, and you would see a wide range of data bits, because then data bits, since I'm communicating with multiple DRAMs at the same time, I will have, by definition, multiple data bits coming back at the same time in parallel.

And so in this particular picture, you see four devices, and each one of these devices could correspond to 16 bits. That's been our example that we've been using, we've been using 16-bit data devices, and so it would take four of those devices operating together to produce 64 bits of data information. And so they work much the same way, except now they're communicating with four devices and they operate at the same time and produce the information.

And likewise, you can see the module D1 and module D2, I can communicate with either module. So, I can request or store information to either location, to or from either location.

Q. Could you summarize for us very briefly what the different color lines are on here?

A. Yes, the different color lines are the same colors we've been using this morning. The blue again is the clock. The yellow is the control lines, that's

the ones where we're making the decision about what type of operation. The red itself is the address lines, where we're deciding which addresses we're trying to access either for read or write. And the green that you see here are -- the green lines are representing the actual data lines in the system itself.

Q. Mr. Rhoden, let's shift gears a little bit here and turn to the Rambus system. Let me ask you first, when did you first hear of Rambus?

A. It would have been in probably about 1990 or so.

Q. I'm sorry, can you repeat that?

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Rambus architecture based upon your level of knowledge at that time gained in part through that meeting, if you could answer my following questions on that basis?

A. I will try, yes.

MR. PERRY: Your Honor, I don't know your preference. I was just wondering if this might be a good time for a lunch break. We're switching into a different --

JUDGE McGUIRE: That thought had entered my mind. Do you have some idea as to how soon you want to break? When is a good time? This might be a good time to break if we're getting off on a whole new area, but it's up to you, Mr. Oliver. It's your case.

MR. OLIVER: This would be a fine time, Your Honor.

JUDGE McGUIRE: Yeah, I think it would be, and I appreciate that, Mr. Perry.

Then why don't we break until I think 2:30, and at that time we'll have court reconvene. We are now in recess.

(Whereupon, at 1:00 p.m., a lunch recess was taken.)

AFTERNOON SESSION

(2:30 p.m.)

JUDGE McGUIRE: This hearing is now in order and reconvened at 2:30 p.m.

At this time, you may proceed, Mr. Oliver.

MR. OLIVER: Thank you, Your Honor.

BY MR. OLIVER:

Q. Before the lunch break, we had been looking at SDRAM memory modules and had begun to talk about RDRAM. Do you recall that, Mr. Rhoden?

A. Yes, I do recall.

Q. Perhaps to refresh our recollection, could we bring back up the demonstrative we had on the SDRAM module?

A. Okay.

Q. Mr. Rhoden, could you explain once again what these lines demonstrate?

A. Yes, this is a memory subsystem, memory controller and memory modules with the bus that interconnects them with the clock line in blue, the control lines in yellow, the address lines in red and the data lines in green.

Q. And Mr. Rhoden, I believe that before the lunch break you had testified that while you were at Hewlett Packard, you had heard a presentation by Rambus of

their technology. Is that right?

A. Yes, I did.

Q. And roughly what time period was that again, please?

A. This would have been about 1990, in that time frame.

Q. If you could answer the following questions based on your understanding of the Rambus technology in the early to mid-1990s, please.

A. Certainly.

Q. During the early to mid-1990s, were you familiar with Rambus' memory architecture?

A. During the 1990s?

Q. Yes.

A. Yes, as a result of a visit, yes, I was.

MR. DETRE: I'll object, Your Honor, on the basis of foundation. We have only heard about one presentation that he saw in 1990, nothing about the mid-1990s.

JUDGE McGUIRE: Could you clarify that question? Otherwise, that is sustained.

BY MR. OLIVER:

Q. Between the presentation you've spoken about and mid-1996, did you have occasion to learn more about the Rambus architecture?

A. Not a great deal, no, sir.
Q. Between the time period of 1991 and 1996, did you have an understanding of the Rambus architecture?
A. Yes, I did.
Q. Are you familiar with the term RDRAM?
A. Yes, I am.
Q. What does RDRAM mean?
A. RDRAM was the term coined by Rambus, Rambus DRAM, for their particular flavor of DRAM that they were designing.
Q. How, if at all, does RDRAM differ from the memory module that we've been looking at?
A. Actually, in quite a number of ways. I think we do have a demonstrative that will show some of that, and the most obvious difference, as you can see, that the signals that we've been treating as address, data and control are now all shared across the same narrow bus, and the clock is now a loop clock that goes out and back. So, it's physically different from the one in its implementation of how information is actually propagated in the system.
Q. You referred to a narrow bus. What did you mean by that?
A. Oh, the width of the bus is eight bits, eight lines in this particular case, and the original

approach was to use only eight bits to do all functions, address, data and control across the same function -- across the same lines.

Q. How would that compare with the typical number of bits in a typical SDRAM system?

A. Well, a typical SDRAM has dedicated address lines, dedicated data lines and dedicated control lines to do those functions in a parallel way, and the bus typically is wider in terms of the pin count, the number of bits that are involved in the communication.

Q. How much wider would a typical SDRAM bus be?

A. A typical SDRAM bus would be over 100 pins, 100 to 120 pins, something like that.

Q. Now, I notice that the bus lines on this demonstrative have multiple colors. Can you explain, please, what that represents?

A. The demonstrative is actually attempting to illustrate that address, data and command all share the same lines, such that there's no longer a red line dedicated to address, there is no longer a yellow line dedicated to control and no longer a green line dedicated to data. They all share the same exact lines, and they -- the term that we use in the industry is multiplex. They interleaved, if you will, all of the different functions onto the same lines.

Q. Did you understand the RDRAM architecture to be a multiplexed architecture?

A. Yes, I did, called multiplexed bus and packet protocol is the two terms that were very common in use at that time.

Q. I'm sorry, could you repeat that, please?

A. Multiplexed in terms of the signals themselves and packet based in that all of the information was accumulated into something that is referred to as a packet. It's just a terminology that's used in the industry to describe an architecture like this.

Q. Could you please explain in a bit more detail how the Rambus packet-based system worked?

A. Yeah, I think there's also some more demonstratives to give you some information. This would show on successive clock cycles, you can see that the address and control or a read operation would go into the RDRAM from the memory controller, all shared on the same lines, at different intervals of time. Sometimes it would be address, sometimes it would be command. This is just a simplified approach showing it.

Q. What do the red and yellow boxes indicate?

A. The red and yellow boxes, those that are red indicate address information, those that are yellow

indicate control information, and the vertical lines that actually separate the boxes would indicate different intervals of time. So, in other words, the first interval would have some red and some yellow. The second interval might have all yellow. The third interval may also have all yellow. This would be the type that we would call a packet of information. So, on successive clock cycles, we would see different pieces of information.

Q. What would happen with the data in a read operation?

A. Well, this is a read request, and so the read request would then go into the RDRAM, and the read data would come back at a later time. I think there's the -- yeah, at some later time than the read, which would be also a packet of data, would then be returned back to the memory controller across those same exact lines. So, the sharing of the lines means sometimes the lines are being used for address, sometimes they're being used for control, sometimes they're being used for data.

Q. And how would a write operation work on the RDRAM architecture?

A. How would a write operation?

Q. A write operation.

A. I think the next demonstrative will actually show that, where the packet itself would just be larger and the address, control and data would be handled on successive clocks, if you will, within the system.

Q. Now, you also mentioned the Rambus clocking system. Could you explain that in a bit more detail, please?

A. Yes, this clock that you see here is a -- you see there is what they call an early clock and a late clock, which is a round trip. Some people refer to it as a loop clock, and I think there's a demonstrative that actually will show how that works. It goes from a -- you see the term bus master. It's also a memory controller, if you want, but it's basically information -- you see the outbound clock comes out the top, and it loops around and travels back, and necessarily the little clocks that you see would indicate that the data arrived at each of the locations, each of the DRAM devices at a different time, and then internally the RDRAM would use the relationship between both the inbound and the outbound clock to determine what function they would do or how they would synchronize.

Q. Now, did the Rambus architecture use modules of any form?

A. They have had modules, yes, later, and I think we have an example of the modules themselves.

Q. Can you explain what the multi-colored lines depict here?

A. Sure. This is the same thing that you've seen before, CPU, memory controller, along with the chipset and the other functions, and from the memory controller into the RDRAM modules is a bus that goes up into the module, through the module itself, exits the module, goes to the next module, and continues in a more or less serial fashion. And the Rambus DRAMs themselves attach directly to the connections on these modules, and they communicate with one device at a time.

Q. We had earlier looked at a demonstrative that showed eight bus lines. Would there be more bus lines in the case of a Rambus module?

A. There would be less.

Q. Excuse me?

A. Would there be more? Please restate your question.

Q. Yes. Earlier we saw a demonstrative showing eight bus lines. In the case of a Rambus module, would there be more bus lines?

A. Not necessarily. It would be eight, and all of the information would be contained in that packet of

generally created either after the discussion, during the discussion, sometimes before the discussion takes place. When someone has an idea that they'd like to bring into the committee, they will bring in a presentation, and then we will make presentations, and based on the presentations -- and the committee may generate other discussions and may also generate the development of other presentations for that matter.

Our procedure that we follow inside of the JC-42 committee is we typically have a first presentation, then followed by -- after some review, follow that by a second presentation, at which time we would decide if we want to have a ballot or not have a ballot, a ballot to decide additional information or what level of support.

And from that, if the ballot were to pass, then we would move that ballot perhaps on to the final review process, which would be a procedural review to make sure that due process was followed at -- at that time it was the JEDEC Council, now it's the JEDEC board of directors.

Q. Mr. Rhoden, if I could ask you to find CX-302 in front of you. It's a document we looked at this morning.

A. Yes. Yes, I have it.

Q. And if I could ask you to turn to page 23.

A. Okay.

Q. Can you please explain what this page depicts?

A. Yes, this was an indication actually of some of the work that took place around -- in the development of DDR memory.

Q. I see at the top Development Name DDR II. What does that refer to?

A. DDR II was the second generation of DDR memory, and DDR was just a second generation of SDR memory, that these are based -- within JEDEC, we follow the process of evolutionary progress. So, there's some thousand things that go into the making of a particular DRAM, and we tend to change just a few, maybe a handful, maybe -- sometimes two or three, sometimes four or five, but that's the typical process, is we just evolve one to the next, to the next, with as little changes as possible, because it's much easier to bring the whole industry along when you make minor changes.

Q. Would it be fair to say, then, that DDR II was a -- was intended to be a standard that would come after the DDR SDRAM standard?

A. By definition, I mean, what DDR was originally called by a lot of the people that worked on it, we

called it SDRAM II, and it wasn't until Fujitsu actually coined the term DDR that we came up with a different name, called it DDR as opposed to SDR II or something like that.

Currently, DDR II, the next revision, if you will, is called DDR II for lack of a better name. If somebody comes up with a better name, I'm sure we'll name it again.

Q. By the way, does your diagram here indicate that the standard-setting work for the DDR II standard started in late 1999?

A. Oh, actually, not at all. The -- we had a -- there's always future work that goes on inside of JEDEC, and through that future work, especially even -- it was very formalized even in the DDR II time frame. We had a future DRAM task group, and the task group itself was tasked with the idea of coming up with the next generation of memory.

As always, you start out with a bunch of ideas, a slate, and what you're going to do with it, and that took place much before 1999. What happened in 1999 was, as a result of all of the work that was taking place in the JEDEC task group, the decision was made that indeed the industry, the users, the suppliers all wanted to base the next generation memory off of the

current generation memory, because as I explained, it's extremely painful to try to come in and change too many things at one time.

And so, the decision was made that we would use DDR as the baseline, and so all of the work that had taken place for the couple of years prior to that would then wind up starting with this as a baseline, if you will, starting point, and then we would take the rest of the work that took place in that task group and feed it into other areas, if you will.

Q. If I could direct your attention to the box appearing between the first presentations and second presentations, it reads, "Simulate & Revise."

Do you see that?

A. Yes, I do.

Q. What did that refer to?

A. Actually, if you see the legend down in the lower left, you'll see that this box is highlighted such that this is actually engineering work. The white boxes are work that takes place inside JEDEC, and simulate and revise is something that engineers would

There are a lot of software programs that allow us to experiment, and experimentation would have been done through software programs to see if the proposals had merit or needed further modification. So, that would be simulate and revise those first presentations, and then we would go to the second.

Q. If I can ask you to go to the box after second presentations, it reads, "Simulate & Validate," and what did that refer to?

A. By the time you're getting to second presentations, things should be in a little bit more firm order, and so the revisions would only be if you found it necessary to fix something, because you've made some basic decisions by that time, and so you would simulate and validate. What you would take is the second presentations and continue simulations, through software again, and through a level of software further down that would actually validate that these, indeed, were reasonable decisions to be taken -- to be making, and proceed then to the ballot process.

Q. Now, when you prepared this document, you indicated that you expected the standard to be published in 2002. Is that right?

A. Yes, I did.

Q. And was the DDR II standard, in fact, published

activity of the task group that actually was charged with creating a next generation for this started a couple of years before that.

Q. Now, is that time frame unusual for JEDEC standards?

A. No, it's not, not for a complete revision like this.

Q. Why does it take so long to develop a JEDEC standard?

A. Well, the JEDEC process doesn't take very long. The -- I mean, part of what this slide is telling you is that the JEDEC steps themselves are pretty simple and straightforward. It is the actual engineering effort that takes place in the shaded boxes, that's where the real work is. That's what takes the most amount of time, and that takes months and often times years.

The ones where you see proto test and build, you are actually physically building systems to try this out, and it takes a good deal of time to do that.

JUDGE McGUIRE: Sir, let me interject and ask a question. You testified earlier that in this process, there's a lot of competition to get out these things on time, because everything is happening so quickly.

THE WITNESS: That's right.

JUDGE McGUIRE: How does that comport with what you just said about at times this takes years for these to evolve into a standard?

THE WITNESS: It's a very good question, Your Honor. The -- the -- we always are faced with a trade-off, and the objective is to get things out as soon as possible, and the "as possible" usually has more to do with the engineering than it does the actual process.

The JEDEC process itself -- many years ago, perhaps the process itself took as long as a couple of years. Now the process itself is very short, I mean a matter of a few months now. And so, what we've done is we've removed the process itself from the bottleneck, and now the bottleneck is actually the engineering itself.

I mean, that was when I indicated -- I said now, if we could just speed up the technology. The technology development itself -- some things we can propose, we can conceive, but until it's actually available for us to build, until fabs are actually built and constructed, and these things take years to build, we cannot complete the process.

BY MR. OLIVER:

Q. Mr. Rhoden, with respect to the JEDEC

standard-setting process, do most members have similar ideas as to what features they would like to see in standards or is there sometimes difference of opinions?

A. Oh, it's almost always a difference of opinion.

Q. Can you explain what factors might lead to differences of opinion?

A. Well, differences -- when we're working on a particular device or whatever, there will be proposals that are made that come from usually a number of different companies. Sometimes multiple proposals or multiple ideas, if you will, come from a particular company, but more often than not, it comes from a variety of companies.

So, you will have several different proposals that will be made inside JEDEC as to what path we should take for the next improvement cycle, if you y?r sals

path they're going to take.

Q. Mr. Rhoden, if I could ask you to find JX-10 in front of you. That should be a set of meeting minutes from the December 1991 meeting. It will be in the large stack in front of you.

A. Okay, I have it. It was easy, it was on top.

Q. Mr. Rhoden, do you recognize JX-10?

A. Yes, I do.

Q. What is this document?

A. This is a meeting minutes for the JC-42 DRAM committee from December 1991.

Q. Were you present at this meeting?

A. Yes, I was.

Q. Is there a way to tell from the document that you were present?

A. Yes, actually, the -- as we talked about the sign-up sheet, we take the names from the sign-up sheets, and they are translated to the names that you see at the front, by members, by others present, and it goes across a couple of different pages that you see here. The first two pages are primarily people that attended the meeting.

Q. Now, as of December 1991, was the JC-42.3 subcommittee working at that time on developing a standard for SDRAM?

A. Yes, they were. They had been working for some time on it.

Q. Do you recall what methods were being proposed at that time to determine CAS latency and burst length?

A. Well, actually, there were a number of methods that were under discussion at that time, and the -- as proposed by a variety of companies, and in this time frame, there would have been several different proposals, probably contained in these minutes I'm sure.

Q. Could I direct your attention to page 4, please, and specifically to item 4.8, which reads, "TI Sync DRAM."

Do you see that?

A. Yes, sir, I do.

Q. And underneath that, it says, "TI showed a revised presentation (See Attachment I)."

A. That's correct.

Q. Do you recall what this presentation was about?

A. Yes, this would have been TI's opinion about what we should be doing for the next generation memory device, and it would be contained in these meetings in Attachment I.

Q. Could I ask you to turn to Attachment I, please. I believe it's at page 56.

A. Yes, page 56, yes.
Q. Is that, in fact, the Texas Instruments presentation that was referenced in point 4.8?
A. Yes, it is. This would be the referenced item from the minutes.
Q. Now, in this Texas Instruments presentation, how was Texas Instruments proposing to determine the CAS latency value and burst length value?
A. Well --
MR. DETRE: Objection, Your Honor. There has been no foundation laid that this witness knows what TI was proposing.
JUDGE McGUIRE: I think that's sustained. Could you requestion --
MR. OLIVER: Yes, Your Honor.
BY MR. OLIVER:
Q. Mr. Rhoden, were you present at the December 1991 JC-42.3 meeting?
A. Yes, I was.
Q. Were you present when Texas Instruments presented their proposal?
A. Yes, I was.
Q. Did you observe that presentation at the time?
A. Yes, I did.
Q. How was Texas Instruments proposing to

determine the CAS latency and the burst length in their presentation?

A. The -- as you can see from their presentation, under the second main bullet item, they say, "Features to be programmed in the WCBR cycle." WCBR, it was an earlier definition of what we later changed to be the mode register set cycle. And underneath that you will see several bullets, the last of the four bullets up there says, "Data clock latency," and data clock latency was a term that was used at that time that we later changed to be CAS latency. It's just a choice of terms that everybody has a -- at first has perhaps many different ideas of what name to call it, and Texas Instruments called it data clock latency, and ultimately we decided that the standard terminology would be CAS latency.

Q. So, does that indicate, then, that Texas Instruments was proposing a programmable CAS latency?

A. That is correct, they were proposing to use a register to program the value for CAS latency.

Q. Now, with respect to burst length, how was Texas Instruments proposing to determine the burst length?

A. In the same fashion. You can see they say, "Features to be programmed into the WCBR cycle." In

the second bullet item, you see wrap length, and wrap length is actually the term that Texas Instruments used at the time. Later that was changed to be burst length, and it's strictly a terminology. Wrap is one term that was used at the time. It's the same thing. They were proposing that we program this in with a particular register through the WCBR cycle.

Q. Now, Mr. Rhoden, I would like to reference 9.3.1 of the -- I'm sorry, strike that, please.

Mr. Rhoden, based on your understanding of the JEDEC disclosure policy at that time, was this presentation work the type that would trigger a disclosure obligation?

A. Certainly it would.

Q. If I could ask you to turn back to the minutes at page 4. If I could direct your attention to item 4.9.

A. Okay, I see that.

Q. It reads, "Toshiba Sync DRAM."

Do you see that?

A. Yes, I do.

Q. What does that reference refer to?

A. That refers to another Synchronous DRAM presentation, this time made by Toshiba, and it would be contained in item J of the appendix or attachments,

excuse me.

Q. Now, were you present at the JC-42.3 subcommittee meeting when Toshiba made its presentation?

A. Yes, I was.

Q. And did you observe that presentation?

A. Yes, I did.

Q. Do you recall what that presentation was about?

A. Yes, I do.

Q. What was the presentation about?

A. It was about Toshiba's proposal for the feature set and methodologies to be used for the next generation Synchronous DRAM.

Q. If I could ask you to turn, please, to page 66.

A. Sixty-six?

Q. Yes.

A. Yes, I see it. I have it.

methodology. Again, they're saying synchronous mode set proposal, so mode set cycle later became known as mode register set. The timing diagram that you see there is actually the same as the one that TI had proposed, which was the -- TI called WCBR, but it is the same function.

And then Toshiba actually proposed a register description that's right below that. You see the mode field description, and then all of the list. Once again, they were proposing that it be done by a programmable register.

Q. When you were referring to the timing diagram, were you referring to the lines underneath number 1, mode set cycle?

A. Yes, I'm sorry. The timing diagram is the normal engineering term, and you'll see the period of clock that -- the clock goes up and down, basically the series of squares indicates time periods that we saw in operation before, and you see the signals, the RE, CE and W, which were -- the ones that we saw before would be RAS, CAS and write enable. This is RE, CE and W, just again, a different terminology being proposed at this time until it was finally selected.

Q. So, the timing diagram would be those five or so next to the CLK, RE, et cetera?

A. That is correct.

Q. And you also referred to a mode field definition. Were you referring to the series of boxes that are in a line below caption number 2?

A. Yes, I was.

Q. If I could direct your attention, underneath the heading Field, there's a term that I believe reads "module length."

A. Yes.

Q. Do you see that?

A. Yes, I do.

Q. What does that refer to?

A. Modulo length is -- a modulo is another word that is used in the industry for wrap or also later burst. They were talking about sequentially accessing data, and modulo was the methodology that -- it's a term that -- there's so many terms in engineering that have very similar meaning, and this is one of those that -- whether you call it wrap or whether you call it

A. Yes, I do.

Q. What does that indicate?

A. From what we've seen this morning, that would be a burst length of one, a burst length of two, a burst length of four and a burst length of eight. Two, four and eight are the ones ultimately adopted.

Q. And how did Toshiba propose to differentiate between the one, two, four and eight?

A. By programming values into the mode register fields listed as the M. You see the last four bits, A0, A1, A2, A3, would be listed in Ms, and by changing those four bits, you would be able to program what they called modulo, which is ultimately burst length.

Q. If I could direct your attention three lines further down in the Field column, it reads "latency."

Do you see that?

A. Yes, I do.

Q. Mr. Rhoden, if I could ask you to turn back to page 5 of JX-10.

A. Okay.

Q. And if I could direct your attention to 4.10 at the top of that page.

A. I see it.

Q. It's difficult to read, but I believe it reads, "Samsung 16M Sync DRAM."

Do you see that?

A. Yes, I do.

Q. What did that refer to?

A. This was a presentation that Samsung made at the meeting for their proposal as opposed to Toshiba and TI about how we would implement the next generation Synchronous DRAM.

Q. Were you present at the JC-42.3 subcommittee meeting when Samsung made this presentation?

A. Yes, I was.

Q. Did you observe that presentation?

A. I did.

Q. Do you have an understanding as to what that presentation was about?

A. Yes, it is Samsung's proposal about implementation of Synchronous DRAM.

Q. If I could ask you to turn, please, to page 70

of the minutes.

A. Okay.

Q. Is that, in fact, Samsung's proposal?

A. Yes, it is.

Q. How was Samsung proposing to determine the burst length and latency value?

A. Well, actually, as you can see here, Samsung was in favor at this time of a very simple operational device, and they were proposing -- on the first half of the slide, you'll see the first bullet, second bullet, third bullet and fourth bullet, they were proposing that we create a device that would exist common on the same die. The last two bullet items, fast page and static column mode or fast page mode and static column mode would have been at that time the existing memories common in the industry, and they were proposing that on that same die that they could add additional feature sets.

One would be a synchronous eight-bit wrap mode with a clock pin, and the other would be a synchronous burst mode with a clock pin, and they were proposing to select between these as a manufacturing option, metal mask or whatever you like. So, while these would exist on the same die, they would select it at manufacturing, which function they would actually ship.

the -- which one is which, just that they were two different modes of operation of the device, and they were proposing for selecting between those two different burst options. They were proposing using a fuse to do that.

Q. How would a manufacturer use a fuse to select between those options?

A. Well, a fuse is a pretty common --

MR. DETRE: Objection, Your Honor. We have had no foundation that the witness is expert in any kind of manufacturing. It's not clear to me whether he's still recalling now or --

JUDGE McGUIRE: Overruled. I'll entertain the answer if you have one.

THE WITNESS: Thank you.

The -- fuses are very common in DRAM, and fuses are common in perhaps many devices, but certainly in DRAM. Fuses are a common element that's used to select particular functions. Inside DRAMs that are shipped today, they use fuses to select bad bits or good bits. When they're testing a device, if they find a block that's bad, they would use a fuse to actually block that bad one out, and they always build the devices with some extra hanging around, and they will then program it such that they can replace the bad one for

the good one.

So, fuses were pretty common at this time, still are very common, and they were proposing using a fuse similar to the ones that were in common use at the time and still today to actually select this option.

BY MR. OLIVER:

Q. In late 1991 and early 1992, did you have an understanding as to whether it would have been possible to use fuses to determine the CAS latency and the burst length?

A. I --

MR. DETRE: Objection, Your Honor. I think that Mr. Oliver is now getting into expert testimony from the witness and his opinion on what might have been possible, and Mr. Rhoden hasn't been designated as an expert.

JUDGE McGUIRE: Overruled.

THE WITNESS: As I said, fuses were a very common function that existed in all the memory at that time, so fuses would have been an easy selection, and Samsung was very much in favor of it, because it would be -- it would provide a simple device.

BY MR. OLIVER:

Q. Do you recall whether any JC-42.3 subcommittee members proposed to use fuses to determine either CAS

latency or burst length?

A. The discussion certainly took place. I was the discussion leader for most of the SDRAM throughout its development, and a fuse was one of the options that was considered for a very long time, until we finally settled on the register. So, yes, indeed, many people did.

Q. By the way, would -- in terms of how use of fuses was being discussed within 42.3 at the time, was that being discussed as an alternative to programming CAS latency or burst length through the mode register?

A. Certainly it would be, yes.

Q. If I could ask you to turn back to page 5 of the minutes, please, and if I could direct your attention to the second item, the 4.11, beginning with Mitsubishi.

Do you see that?

A. Yes, I see it.

Q. What did this item refer to?

A. This item referred to the Mitsubishi proposal for Synchronous DRAM, and their proposal would be contained in the attachments, item L it looks like.

Q. Were you present at the 42.3 subcommittee meeting when Mitsubishi gave this proposal?

A. Yes, I was.

Q. Did you observe the Mitsubishi presentation?

A. Yes, I did.

Q. Now, what did the Mitsubishi presentation involve?

A. Mitsubishi -- I can actually turn to it if you like, but Mitsubishi actually made a proposal slightly different. Mitsubishi was in favor of using pins to select the options as opposed to fusible links or programmable registry.

Q. Okay, let's go ahead and turn to that proposal. I believe it appears on page 74.

Can you explain what in the Mitsubishi presentation would set forth their proposal for using pins?

A. Excuse me?

Q. Could you please point out which portion of the written Mitsubishi presentation explains their proposed use of pins?

A. Okay, sure. The -- if you look at the table at the top of their page here, it lists at the top of the first column, it says Pin, and at the top of the second column it says Function, and you'll notice that there's a clock pin, there's something they call a BT pin, which they label outside as a burst mode. There's a WP for wrap mode, and there's a WT for wrap type, and each

one of them are defined.

What they were proposing was the use of these pins, in other words, adding additional pins to the device itself to actually control the functions of the burst length, the burst type and the -- the -- as you can see over here, it says the burst mode -- that all of them are shown in the function itself, what type -- and they call it -- once again, I'm using the term burst, and I apologize, because burst and wrap -- since they mean the same to me, I apologize.

They're using the term selects wrap mode, but wrap and burst are synonymous terms in the discussion of SDRAM.

Q. Can you explain in a bit more detail how Mitsubishi was proposing to use pins to set the burst length, for example, or the wrap length?

A. Certainly. They were proposing just taking pins, available pins that were on the device, and using those pins to generate the type of function and the type of operation for the devices themselves. These would be external pins to the device.

Q. Mr. Rhoden, if I could direct your attention to the box in the lower left-hand corner of the page, page 74.

A. Yeah, I just managed to mess it up. Sorry.

Okay, the box at the lower left hand, yes.

Q. Do you see there's a heading BT, a heading WP, and a heading Mode?

A. Yes.

Q. Do you see that?

Then underneath BT, for example, there's Hs and Ls.

A. Yes.

Q. What does that refer to?

A. The -- since these are external pins to the device, this table refers to, if you connected these, the H would represent a high voltage level, the L would represent a low voltage level. So, I have external pins with a device, and if I connect, for instance, both of the pins to a high voltage level, then I would be in the mode of normal operation. If I connected the two pins both to low, then you could look at the bottom and you could see that I would be in a four-bit wrap operation. And the one above that, if you want to see it, says with BT, the first signal of H, and WP, the second signal low, you would be in an eight-bit burst operation -- wrap, sorry.

Q. Based on what you testified earlier, would it be fair to say, then, that the L-L would refer to a burst length of four?

A. That is correct.

Q. And H-L would refer to burst length of eight?

A. That is correct.

Q. Okay, we've discussed now use of programmable features in mode register to set CAS latency and burst length, use of fuses to separate -- to determine the burst type as well as discussions of fuses involving CAS latency and burst length.

A. Right.

Q. And use of pins to set CAS latency and burst length. Is that right?

A. That is correct.

Q. Were there any other methods of determining CAS latency or burst length that were being proposed at any time period during late 1991 or early 1992?

A. Yes, during committee discussions, there's -- as is often the case, if you give ten engineers a problem, you'll probably get 12 or 14 solutions, and the same is true inside the discussions inside the committee. People were proposing a number of other approaches to the same type of thing. All we're trying to do is set a mode of operation for the device, and since most of them would operate in that particular mode constantly in any given system, the actual methodology had a lot more flexibility about what you

could select and how you could use it, because it was just a static condition that you would put the part in, and so -- I'm not sure I can remember all of them, but there were certainly a wide variety of them.

Q. If I could direct your attention now to page 5, item 4.12.

A. Okay.

Q. This reads, "IBM Synchronous DRAM versus HST Toggle."

Do you see that?

A. Yes, I do.

Q. What does this refer to?

A. This would be a presentation made by IBM and contained in Attachment M, that's a presentation they would have made before the committee.

Q. By the way, it refers to Mark Kellogg. Who is Mark Kellogg?

A. Mark Kellogg is a long-time member, a very active member, within JEDEC that works for IBM.

Q. Now, were you present at the 42.3 subcommittee meeting at the time of Mr. Kellogg's presentation?

A. Yes, I was.

Q. Did you observe that presentation?

A. Yes, I did.

Q. What did it involve?

A. Mr. Kellogg was actually proposing a functionality that IBM had utilized in some of their own devices as a proposal for controlling data and data flow, and high-speed toggle is the terminology that was used, which says -- it says HST toggle, but if you actually unfold the acronym, it would read "high-speed toggle toggle" here, so sorry for the confusion, but HST mode is what it is.

Q. Okay, if I could ask you to turn to Attachment M, which is at page 84, please.

A. Okay.

Q. Is that the presentation that Mr. Kellogg made?

A. Yes, it is.

Q. Can you explain, please, what Mr. Kellogg was proposing by high-speed toggle?

A. High-speed toggle was the use of a signal on the DRAM to control data on both edges of the clock. They were using the CAS clock to actually cycle data on both edges of the clock, and they did this in devices that they shipped in earlier machines, and they were proposing that we include that for use in our future DRAM as a method for achieving higher performance, which was one of the things that we were working toward at the time.

Q. When you refer to both edges, are you referring

to a rising edge and a falling edge?

A. Yes, I am. I'm sorry.

Q. Now, was IBM proposing a synchronous device or asynchronous device or was it something different?

A. Well, in terms of data, it was a synchronous device because of the nature of how -- remember I said, I said it's a CAS clock. It's a function that's fundamentally synchronous. So, as we would toggle the CAS signal, column, clock, whatever -- whichever name you want to call it, you would get data out on -- from the rising edge and from the falling edge in a synchronous fashion.

Q. So, just to be clear, the data is coming out of the rising edge and falling edge of what?

A. Rising edge and falling edge of the signal. Some people would call it the HST signal, some call it the CAS signal, some call it the CE signal or the CAS clock.

Q. Now, was the CAS signal in constant operation?

A. In this case, no, it was not.

Q. In a Synchronous DRAM that has a system clock, is the clock in constant operation?

A. The system clock is in constant operation, that is correct.

Q. Would it be fair to say that that is a

distinction between the IBM high-speed toggle mode and the dual edge clock?

A. Well, sort of, except in -- actually, in DDR, the data clocking signal is actually the data strobe signal, which is not continuous free running. It operates much the same as high-speed toggle does. It's a temporary signal, but in terms of having -- are the -- does the high-speed toggle chip that IBM produced have a free running clock, no, it did not, and did it have a CAS clock, yes, it did.

Q. If you could characterize whether high-speed toggle mode was fairly similar, fairly different or somewhere in between with respect to dual edge clock. How would you characterize it?

MR. DETRE: Objection, Your Honor, vague and calls for opinion testimony.

JUDGE McGUIRE: Overruled. I think he's qualified to answer the question.

MR. STONE: Your Honor, can I ask you to clarify, are we going to have opinion testimony from people who are not designated as experts? That's not something we contemplated, and I guess in taking discovery, it's not something we expected we would confront. We expected opinions would be proffered from those designated as experts, and if all of the

witnesses can give their opinions because they have the expertise but weren't so designated, it does a little bit change the nature of what we had expected, and I just wanted to see if I could clarify that scope --

JUDGE McGUIRE: Well, I'm a little confused here as to whether he's giving opinion evidence or it's based on his perception at the time. Now, if we can state the question again, then I will at that point reconsider.

MR. OLIVER: Yes, thank you, Your Honor. I should be more precise with my question. Thank you.

BY MR. OLIVER:

Q. Based on your observations of the IBM presentation of high-speed toggle at that time, characterizing your understanding, did you understand the high-speed toggle proposed by IBM to be similar to a dual edge clock, different from a dual edge clock or somewhere in between?

A. It's actually almost identical.

MR. DETRE: Objection, Your Honor. The dual edge clock that Mr. Rhoden testified about in DDR was much, much later, so this question really could not be based on his observations at the time that he was observing the high-speed toggle. Unless later he somehow did this comparison, this is pure opinion

testimony he's being asked for now.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Rhoden, could you find document CX-34, please. I'm sorry, Mr. Rhoden, it's a set of meeting minutes from the May 1992 meeting. It would be in the large stack of documents.

A. CX-34, okay, I have it.

Q. Do you recognize CX-34?

A. Yes, I do.

Q. What is it?

A. This would be meeting minutes, and it's meeting minutes from the JC-42.3 DRAM committee from May 1992.

Q. Did you attend that meeting?

A. Yes, I did.

Q. If I could direct your attention, please, to page 30 of these minutes.

A. Page 30?

Q. Yes.

A. Okay.

Q. It states in the upper right-hand corner, "Attachment E."

A. Attachment E?

Q. Attachment E as in Edward?

A. Yes, I do have Attachment E, yes.

think this would have been a proposal that he would have made at the special meeting.

Q. All right. Were you present at the special meeting when he made the proposal?

A. Yes, I was.

Q. And did you observe the proposal?

A. Yes, I did.

Q. If I could direct your attention to the first star underneath Asynchronous RAS/CAS, underneath that it reads, "Dual edge clock."

Do you see that?

A. Yes, I do.

Q. What was Mr. Hardell proposing regarding dual edge clock?

A. He was proposing using both edges of the clock for the transition of data and information inside the Synchronous DRAM.

Q. How, if at all, did this presentation from Mr. Hardell differ from the presentation of Mr. Kellogg in December 1991?

A. In a lot of ways, they are very similar, except in Mr. Hardell's case, he wanted to operate the whole device on the dual edge clock, such that it would be a free running clock.

Q. Excuse me, it would be what?

A. It would be a free running clock in Mr. Hardell's case.

Q. What differences, if any, existed between the dual edge clock proposed by Mr. Hardell and the clocking scheme ultimately adopted within the DDR standard?

MR. DETRE: Objection, calls for opinion testimony.

JUDGE McGUIRE: Sustained.

BY MR. OLIVER:

Q. Mr. Rhoden, were you involved in the JC-42.3 subcommittee at the time that 42.3 subcommittee adopted the DDR SDRAM standard?

A. Adopted -- excuse me?

Q. Were you active in the 42.3 subcommittee at the time that the 42.3 subcommittee voted to adopt the DDR SDRAM standard?

A. Yes, I was.

Q. Did you vote on various proposals with respect to the DDR SDRAM standard?

A. I was involved in all of the activities of the committee at that time, yes.

Q. Did you vote on the proposal to use a dual edge clock in the DDR SDRAM standard?

A. The -- the voting whether to use the DDR or

not, at the time I was coordinating development between multiple companies, and so normally I would lead the discussion, and as leader, I would often choose not to vote such that I did not bias the outcome, but I was the leader of the discussion, so yes, I was involved.

Q. Were you familiar with the ballots proposing to use a dual edge clock in the DDR SDRAM system?

A. Yes, I was.

Q. And did you have an understanding of the dual edge clock being proposed in the DDR SDRAM system?

A. Yes, I did.

Q. Based on your understanding of dual edge clock being proposed for the DDR SDRAM standard at that time and based on your understanding of Mr. Hardell's presentation in April 1992, what differences, if any, do you understand there to be between the dual edge clock being proposed, as you understood it, in the ballot for the DDR SDRAM standard and Mr. Hardell's presentation?

MR. DETRE: Objection, Your Honor, calls for opinion testimony. The witness is being asked to make a comparison today. It is not based on any comparison he made in the past.

JUDGE McGUIRE: That one's overruled. I think the way he asked that is utterly proper.

You can answer.

THE WITNESS: The differences was almost none. What Mr. Hardell was proposing is essentially what we ultimately wound up with in the standard for DDR.

MR. OLIVER: Could I have just a moment, Your Honor, please?

JUDGE McGUIRE: Go ahead.

(Counsel conferring.)

BY MR. OLIVER:

Q. Mr. Rhoden, could you please find JX-59? It's a JEDEC ballot that I believe you looked at this morning.

A. Okay.

MR. PERRY: Did you say 59?

MR. OLIVER: Fifty-nine, yes.

MR. PERRY: Thanks.

THE WITNESS: Okay, I have it.

BY MR. OLIVER:

Q. And you recall that we discussed this ballot this morning?

A. Yes, I do.

Q. Could you please explain what this ballot involved?

A. The subject of this ballot, as you see at the

it would indicate programmability of the device in other modes.

And one of the things that they would -- so, the horizontal is a representation of the register, and the lines that are connected to the boxes that you see here indicate the function represented as programmed by those bits within that register. So, at the top you see wrap length, and remember I said wrap length and burst length are the same thing. The second one, WT, wrap type, burst type, the same thing. And the bottom is latency mode, and latency mode and CAS latency are the same thing.

In fact, in this particular table, it's actually labeled CAS latency above the -- in the table at the bottom right-hand corner of the ballot itself.

Q. Just to be clear, how was the ballot proposing that the latency mode would be set?

A. The latency -- the latency mode in this ballot is proposed to be set by a programmable register, the mode register.

Q. And how is the ballot proposing that the wrap length would be set?

A. The wrap length/burst length would be set by programming a value into the mode register, a programmable register.

Q. Can you please explain briefly the events that led up to the JC-42.3 subcommittee issuing this ballot?

A. Sure. The committee itself actually discusses, as you saw, the many different options that you see, and in the process of standardization, we can't really have a plethora of approaches on how to support -- how to approach something. The concept is to just pick one. And so, the committee picked one to move forward, and this was the item that they picked to move forward.

So, the committee would pick one. Somebody would basically recommend that they send something out for ballot. That's what happened. Somebody recommended that they send this out for ballot, and then someone else would second, we would take a vote, send it out for ballot, and then actually vote on it.

Q. When was this ballot sent out?

A. You can see this ballot would have gone out in June 1992.

Q. Can I ask you to please find JX-13 in front of you, please? It's another set of minutes from July 1992.

A. Okay. Thank you for telling me what type. It helps me find the pile.

MR. OLIVER: Actually, Your Honor, I realize I'm getting a little ahead of myself here, if I could

just take this moment to offer into evidence first JX-10.

JUDGE McGUIRE: Any objection, Mr. Detre?

MR. DETRE: No objection.

JUDGE McGUIRE: If not, it's so entered.

(JX Exhibit Number 10 was admitted into evidence.)

MR. OLIVER: Your Honor, could I also offer into evidence CX-34, the meeting minutes from May 1992?

MR. DETRE: No objection.

JUDGE McGUIRE: Any objection? So entered.

(CX Exhibit Number 34 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, if I could direct your attention back to JX-13.

A. Okay, I have it.

Q. And do you recognize this document?

A. Yes, I do.

Q. What is it?

A. This would be meeting minutes from JC-42.3, DRAM committee, from July 1992.

Q. Were you present at this meeting?

A. Yes, I was.

Q. If I could direct your attention, please, to

page 9, do you see item 16 on that page, DRAM Ballot Counts?

A. Yes, I do.

Q. What does that item refer to?

A. In the minutes, we record -- when we have sent out a ballot and it has been voted on, we try to record the pertinent information about the discussion of that ballot in the minutes, and so this would have -- the ballot count, we would go through the subsequent things under -- the DRAM ballot count would have been ballots that were -- had been issued from either the previous meeting but were issued to be counted at this meeting.

Q. Now, the ballot reflected in JX-59, was that counted at the July 1992 meeting?

A. Let's see, this is the -- it probably would have been. Let me -- I'm looking for -- inside the minutes, we have to look for the JC -- the ballot number. Ballot number 85, and I'm --

Q. If I could direct your attention to paragraph 16.3 on page 10.

A. Okay, thank you. Yes, it is that -- the mode register ballot.

Q. Did the mode register ballot pass?

A. Yes, it did, the -- you see the vote count was 14 yes, five no and seven abstentions, and the voting

requirement inside of JEDEC is two-thirds. That means we have to have twice as many yes as to we do nos, and we do in this case, so the ballot did pass.

Q. So, if there is a vote with more than two-thirds majority, does that mean that the ballot then automatically passes?

A. That -- yes. I mean, the ballot actually passes when the vote count is two-thirds.

Q. Is there any further procedure that's taken?

A. Yes, inside the committee, we take the further procedure to discuss and resolve the -- or at least -- I think perhaps the best term instead of resolve, we discuss and address all of the comments that had been made. Whether the comments were made in respect to a yes vote or a no vote or an abstain vote, anybody can make a comment on a ballot if they want to, and we make certain that we address the comments before proceeding further with the ballot.

Q. Why is JC-42.3 certain to address the comments before proceeding?

A. We did address the comments, yes.

Q. Why does the JC-42.3 subcommittee address the comments before proceeding?

A. Oh, I understand. Addressing the comments is part of the due process. In the standardization

procedure, we want to make certain that we give everybody the opportunity to speak and participate in the standardization process itself.

Q. If I could direct your attention back to page 10, under item 16.3, it reads, "The vote was: 14 yes, 5 no, 7 abstentions. The no votes were from Compaq, Hitachi, IBM, Rambus and TI."

Do you see that?

A. Yes, I do.

Q. Now, do you recall whether there was any discussion of the -- of any comments from Rambus?

A. Yes, there was.

Q. What do you recall about those discussions?

A. Well, the discussions actually would have been listed in here. You see they -- the companies, Compaq, IBM and Rambus, made the same comments to a previous ballot that had already been discussed and counted, and since they made the same comments, then we would verify in the meeting that the same comments and the same resolutions for those comments still applied, both with the committee and with the people who had made the comments.

Q. If I could direct your attention to page 9.

A. Okay.

Q. Underneath the heading 16.1.

A. Okay.

Q. About the fifth paragraph down beginning "Rambus," do you see that?

A. Yes, yes, I do.

Q. Does that reflect the Rambus comments?

A. Yes, it does.

Q. And those are the Rambus comments that you were

have been sent at this time, because it has passed the committee, but in this particular case, I think what we did is we decided to hold it and send it with a group of other ballots that were pending, that some had passed, and we sent the rest of them on in March 1993. That's when we sent the group of 15 that were the early fundamental definition of SDRAM.

Q. And that group was sent in March of '93, did you say?

A. Yes, it would have been. It did happen at that time.

Q. If I could direct your attention, please, to JX-56.

A. What --

Q. This is a JEDEC standard, a fairly thick document.

A. Okay, 56, okay. I have it.

MR. OLIVER: Your Honor, I realize I'm getting ahead of myself again. Could I at this time offer into evidence JX-13, please?

JUDGE McGUIRE: Any opposition, Mr. Detre?

MR. DETRE: No objection.

JUDGE McGUIRE: If not, so entered.

(JX Exhibit Number 13 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, do you recognize JX-56?

A. Yes, I do.

Q. What is it?

A. JX-56 is actually the JEDEC standard for memory and memory-related modules, devices, that sort of thing. It's a -- we refer to it as 21-C.

Q. If I could direct your attention to the middle

Q. Where would we find those features in Release 4?

A. It would be under subsection 3.11, I think -- I'm sorry, I don't have the page number for you.

Q. Mr. Rhoden, if I could direct your attention, please, to page 114.

A. 114, okay. I have 114.

Q. What is set forth on page 114 of JX-56?

A. Yes, this is actually the definition of the SDRAM mode register, and we see the similarity to the ballot that was previously discussed.

Q. Does this include programmable burst length?

A. It does.

Q. And where do you see that?

A. It's -- the programmable burst length is listed here under Burst Length in the top table, if you will, about the middle of the page there, you will see burst length in the left column and then bits identifying and then what BT-0 and -- the burst type is listed as.

Q. Does this also reflect programmable CAS latency?

A. It does that as well, and that's the bottom table on the bottom right-hand side. You can see that again it's a table that says latency mode at the right, CL identifying the bit definitions, and then the CE

latency that's listed in the column of 1, 2, 3 and 4, which is -- since it's in parentheses, the 4 item is optional.

MR. OLIVER: Your Honor, at this time I would like to offer JX-56 into evidence.

JUDGE McGUIRE: Any opposition?

MR. DETRE: No objection, Your Honor.

JUDGE McGUIRE: So entered.

(JX Exhibit Number 56 was admitted into evidence.)

MR. OLIVER: Your Honor, if I could interrupt just for a moment just to ask your preferences with respect to timing. We had hoped to try to finish with Mr. Rhoden today and tomorrow. We had hoped to finish our direct today or at the latest fairly early tomorrow morning to permit them to try to finish their cross tomorrow.

I do still have a moderate amount of material to cover. I don't know what your preference --

JUDGE McGUIRE: How much time do you think that will take, to conclude your direct?

MR. OLIVER: I'm guessing two to two and a half hours, Your Honor.

JUDGE McGUIRE: That's going to push us to about 6:30. To me, it doesn't matter. It may be a

good point to go ahead and take the next couple hours and try to get this portion of his testimony I think concluded, but if we could go another hour, then maybe start off again in the morning with another hour or hour and a half, then -- any comment by respondent?

MR. PERRY: I think that we would prefer the latter proposal, but if Your Honor prefers --

JUDGE McGUIRE: Okay, I think that makes sense at this point. Is there some area that you could go for perhaps another half hour or hour and then take a break, or is this a time that you would like to do that?

MR. OLIVER: Your Honor, if I could suggest perhaps if I could take five minutes to try to focus on what I could then do today --

JUDGE McGUIRE: Okay, let's take a five-minute break.

MR. OLIVER: Great. Thank you, Your Honor.

(A brief recess was taken.)

JUDGE McGUIRE: Okay, on the record.

BY MR. OLIVER:

Q. Mr. Rhoden, we left off after having discussed the JEDEC SDRAM standard. Do you recall that?

A. Yes, I do.

Q. And I believe you testified that the final set

of ballots on that was passed at the subcommittee level in March of 1993. Is that --

A. That is correct.

Q. Now, what standard-setting work, if any, did the JC-42.3 subcommittee do between May of 1993 and June of 1996?

A. Oh, a tremendous amount. The work -- inside JEDEC, there is a continuous time line of activity. Work -- it's -- while there are snapshots and we do collect groups of ballots at times, the work is continuous. We're always working on the improvements to what we have, improvements to what we've seen before and future generation of devices. So, that's three things we're always working on.

Q. Now, with respect to the SDRAM standard, what would future generation devices refer to?

A. Well, we call them future generation DRAM -- SDRAM, we call them -- well, as you've seen, the future DRAM task group was one of the terms that we used for a group of activity that we used. Sometimes it was referred to as SDRAM II, sometimes it was just future DRAM.

Q. Did that eventually lead to a standard?

A. Eventually, all of the activity that's inside JEDEC will typically lead to a standard, all the

presentations and all of the activity. It usually has more to do with the timing and availability of process technology than with the actual information flow that takes place in JEDEC.

Q. Let me be more specific. You had described some of the standard-setting work that was being done in the JC-42.3 subcommittee between May of 1993 and June of 1996. Now, did the work that you are referring to eventually lead to a standard?

A. Yes, it did.

Q. What standard did it lead to?

A. Well, the next generation standard would have been the DDR standard that actually came out later. The name DDR was not coined until late 19 -- I forget, 1996? Late 1996 is when the DDR standard came out.

Q. Now, after the SDRAM standard was adopted, did the JC-42.3 subcommittee begin to consider any other features for the next generation standard?

A. Well, certainly. Actually, in the committee, what usually happens is we take -- any time we've completed a particular snapshot, if you will -- remember, this is an evolutionary time line, and we are continually changing and continually improving, if you will, the devices, the modules, all of the things that we're working with, and so through this continuous

evolutionary process, at points in time, we will ship out things that are -- this seem significant at least to the outside world but perhaps are not necessarily to the members, and we will take groups of ideas or groups of ballots, if you will, or groups of presentations and coagulate those into a release like you saw here, Release 4, and the things that we've been considering we continue to consider, and then we add new things to that. So, it is a -- do you understand what I mean by the process is a continuing one in terms of development?

Q. Thank you.

With respect to new features, if any, that were being considered by the JC-42.3 subcommittee for inclusion in the next standard, do you recall discussion of any new features to be added?

A. Sure, the presentation by Mr. Hardell from IBM had generated quite a bit of interest in the beginning, and actually we came very close to including it in the original SDRAM standard, and that's the one where we talked about the dual edge clocking, and at the time, for a number of different reasons, a lot of them had to do with process technology, we decided to actually postpone implementation of that until a later date. So, that continued as part of the discussion.

There were also improvements to the latency, write latency. Discussions took place of additions of PLLs into the devices themselves. Many topics like that were under discussion and discussed during that time frame, and many of those wound up in DDR ultimately.

Q. By the way, just to follow up on one thing you said, you referred to the decision not to include dual edge clocking in the SDRAM standard. Could you give a brief explanation based on your recollection as to why it was decided not to include dual edge clocking in the SDRAM standard?

A. Yes, the dual edge clocking was a technology that would have allowed us to use both edges of the clock, and certainly IBM was already doing that with devices that they were shipping at the time, and the discussion inside the committee essentially centered around, well, in the first place, we didn't need it, because the performance of the memory was substantial enough from a system perspective to be greater than the need of the system, and so we said, well, since we don't need it at this time, perhaps we don't need to expend the effort.

There were also some suppliers that -- their process technology -- and this is actually the process

technology in their fabs themselves -- that would have had a greater degree of difficulty implementing it in that time frame. They still needed to advance their process. Obviously, IBM's process was more advanced because they were already shipping that type of device, and some of the others were as well, but to allow a little bit of time, and for whatever reason, inside JEDEC, we basically pick a path, and we try to pick a path to get to a common agreement, a common standard, and anything that's a good idea sticks around, and we ultimately come back to it as well, and that's exactly what happened with dual edge clock.

Q. Mr. Rhoden, if I could ask you to locate JX-21 in the documents in front of you. This is another set of meeting minutes from September of 1994.

A. Twenty?

Q. JX-21.

A. Twenty-one, okay, I have it.

Q. Mr. Rhoden, do you recognize JX-21?

A. Yes, I do.

Q. What is this document?

A. This is a JC-42.3 DRAM committee meeting in Albuquerque, New Mexico in September 1994.

Q. Were you present at this meeting?

A. Yes, I was.

Q. If I could direct your attention, please, to page 11 of JX-21 and specifically to item 11.3. It reads, "NEC SDRAM Mode Register Item 639."

Do you see that?

A. Yes, I see it.

Q. What does that refer to?

A. That refers to a presentation that NEC made about SDRAM mode register. It was a first showing, and it's in Attachment AA.

Q. Were you present when NEC made this proposal?

A. Yes, I was.

Q. Did you observe the NEC presentation?

A. Yes, I did.

Q. If I could ask you to turn, please, to Attachment AA. It should beon, pldthat r t,f JXtr4f6r

it

Q. Was this presentation one that you would characterize as a proposed improvement on the previous standard or a proposal for a future generation standard or something else?

A. Well, the answer in a sense is yes and yes, because when a proposal is made, it's up to the committee to decide where to put it, obviously, but a proposal like this, when NEC made this proposal, their intent was to actually implement this functionality in whatever device, an existing device or a future device. They were making the proposal as an improvement to what we had today. So, it would be an improvement over a given device, and you can call that a new device if you like.

Q. If I could direct your attention to page 91, please.

A. Okay.

Q. Based on your observation of the NEC proposal at the time, what was your understanding of what NEC was proposing with respect to PLL enable mode?

A. NEC was proposing including a PLL on board the chip to actually synchronize the phased relationship of the internal clock to the external clock. You can see the two boxes on the page there. The left-hand side says without PLL and the right-hand side says with PLL.

Q. At the time you observed this proposal, did you have an understanding of the term "PLL"?

A. Yes, I did.

Q. What was your understanding?

A. The classic terminology for PLL is phased lock loop, and in this case it was used to synchronize the clocks.

Q. In September 1994 when you observed this proposal, did -- were you familiar with the term "delayed lock loop"?

A. Yes, I was.

Q. And based on your understanding in September 1994, what, if any, was the difference between a phased lock loop and a delayed lock loop?

A. Well, in the implementation that NEC was proposing, there was essentially no difference. They were proposing something to allow the synchronization of clock, so delayed lock loop and phased lock loop, we have used both terms interchangeably inside JEDEC.

Q. Based on your understanding of the --

MR. DETRE: Objection, Your Honor, I would like to move to strike that last answer as speculation unless it was based on something that NEC actually said. It wasn't clear to me whether that was the witness' opinion or whether this was actually based on

his observation of the presentation.

JUDGE McGUIRE: Well, let's clarify. Was that based on your observation or as an opinion, because I can't hear your opinion.

THE WITNESS: Well, actually, it's not my opinion. I myself have made presentations about the PLL/DLL being the same inside JEDEC, and the discussion that took place about this at the time that NEC made it used both terms, because that's all -- that's kind of an ongoing discussion that's taken place inside JEDEC for a long time.

JUDGE McGUIRE: Okay, so noted. You may proceed.

BY MR. OLIVER:

Q. Mr. Rhoden, based on your understanding of the JEDEC disclosure policy as of September 1994, did the NEC presentation trigger any disclosure obligation?

A. Certainly, it was a presentation inside of JEDEC, so yes, the requirement to disclose was certainly there.

Q. Mr. Rhoden, if I could ask you next to turn to Exhibit JX-26. It's another set of meeting minutes from the May 1995 meeting.

A. Okay. Twenty-six, JX-26 you said?

Q. Yes.

A. Okay.

MR. OLIVER: Actually, before I ask any questions about that, Your Honor, at this time could I offer into evidence JX-21?

JUDGE McGUIRE: Mr. Detre?

MR. DETRE: No objection, Your Honor.

JUDGE McGUIRE: So admitted.

(JX Exhibit Number 21 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, directing your attention now to JX-26, do you recognize this document?

A. Yes, I do.

Q. What is it?

A. This is meeting minutes from JC-42.3 DRAM committee in May of 1995.

Q. Were you present at this meeting?

A. Yes, I was.

Q. Could I ask you to turn, please, to page 10 of JX-26.

A. Okay.

Q. If I could direct your attention down to 13.7, it reads, "Hyundai SyncLink no item."

Do you see that?

A. The Hyundai SyncLink? Yes, I do.

Q. As of May 1995, did you have an understanding of what SyncLink was?

A. Yes, I did.

Q. What was SyncLink?

A. SyncLink was a consortium of people involved in the memory industry, and they were working to develop a proposal for a future type of DRAM.

Q. If you see the paragraph that follows that, it begins, "A presentation was made by Hyundai (see Attachment Y)."

Do you see that?

A. Yes, I do.

Q. Were you present at the time that Hyundai made a presentation on SyncLink?

A. Yes, I was.

Q. And did you observe that presentation?

A. Yes, I did.

Q. Mr. Rhoden, what do you recall about the SyncLink presentation at the May 1995 JEDEC meeting?

A. Primarily that it was a high-level presentation by Mr. Tabrizi. It was an overview of the proposals for what came to be known as SLDRAM, they called it, SyncLink DRAM at that time.

(Counsel conferring.)

Q. Mr. Rhoden, if I could ask you to turn to page 111, please.

A. Okay.

Q. This bears a caption at the top that reads, "Mitsubishi Electric," and then under that it also says, "64Mbit SyncLink SDRAM."

Do you see that?

A. Yes.

Q. Mr. Rhoden, if I could ask you to turn to page 112, please.

A. Okay.

Q. And particularly I'd like to direct your attention to the language underneath Signal Name - Definition. It reads, "Strobe-in, reference clock, both edge for input, positive edge for output."

Do you see that?

A. Yes, I do.

Q. What was -- again, based on your observation at the time, what was Mitsubishi proposing?

A. Mitsubishi was proposing here a reference clock. Both edge for input is basically, if you want to think about it, it's a dual edge input. Both edge for input and positive edge for output, they were using a combination, if you would.

MR. STONE: Your Honor, if you would ask the witness to speak a little closer to the mike.

JUDGE McGUIRE: Mr. Rhoden, if you could speak up, he can't hear you. I know it's getting towards the end of the day, you're probably getting tired, but we'd appreciate it.

THE WITNESS: I'm slouching back in my chair, so --

JUDGE McGUIRE: I think we all are at this

point.

BY MR. OLIVER:

Q. Mr. Rhoden, if I could direct your attention back to page 10, please.

A. Okay, all right.

Q. Looking again at item 13.7 under Hyundai SyncLink.

A. Okay.

Q. Looking now three lines down, part way through that line, it begins, "The patent issues were a concern in this proposal. It was stated that no known patents exist on this proposal. It was intended to be an open system."

Do you see that?

A. Yes, I do.

Q. Do you recall any discussion of that item at the meeting?

A. There were -- there was a discussion that people, since it was a new proposal that came in that was fundamentally different in a lot of ways from the kind of work that we had been doing inside JEDEC, people were concerned that perhaps there might be patent issue, and the discussion ensued about -- I believe Mr. Tabrizi at this time, it is my recollection, is that he was trying to inform the

committee that he was not aware of anyone else that had any patents that might apply to this.

Q. Do you recall any discussion of Rambus in connection with that patent discussion?

A. I do not.

Q. Did Mr. -- did Mr. Tabrizi give any explanation as to why he thought that SyncLink would be an open standard?

A. Well, part of the proposal when they brought it into the JEDEC body was to make certain that everyone understood and knew that the participants inside SyncLink intended to follow the JEDEC patent policy and develop an open standard. That was their stated objective for a long time, and they made that perfectly clear to all the people involved.

MR. OLIVER: I'm sorry, Your Honor, one minute, please?

JUDGE McGUIRE: Go ahead.

(Counsel conferring.)

BY MR. OLIVER:

Q. Mr. Rhoden, if I could ask you to find JX-28, please. This would be in the pile of meeting minutes. This would be the December 1995 meeting.

A. Are we complete with 26 here?

Q. Excuse me, JX-28.

A. Oh, JX-28, okay. Okay, I have JX-28.

MR. OLIVER: Actually, before I ask you any questions, Your Honor, at this point, I would like to offer into evidence JX-26, please.

JUDGE McGUIRE: Any opposition?

MR. DETRE: No opposition, Your Honor.

JUDGE McGUIRE: So entered.

(JX Exhibit Number 26 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, do you recognize JX-28?

A. Yes, I do.

Q. Were you present at this meeting?

A. Yes, I was.

Q. If I could direct your attention, please, to page 6.

A. Okay.

Q. If I could direct your attention to the top of the page, 8.6, SDRAM-Lite Survey Results.

Do you see that?

A. Yes, I do.

Q. As of December 1995, did you have an understanding of what SDRAM-Lite referred to?

A. Yes, actually, SDRAM-Lite was a series of proposals for modification to the existing SDRAM

standard for creation of a subset device, if you will, to create a "lite," in the same way of light beer, but in any event a lighter proposal.

Q. What do you mean by a lighter proposal?

A. Well, with fewer -- a reduced feature set. By reducing the feature set in some way, they would save manufacturing costs through testing and through capabilities.

Q. Would the proposal have affected in any way either the programmable CAS latency or programmable burst length features of the SDRAM standard?

A. Yes, sir, they were proposing that would be fixed. That was one of the proposals that was under consideration for SDRAM-Lite, was that they be fixed.

Q. As of December 1995, did you have an understanding why it was proposed to make those fixes?

A. Some of the suppliers were expressing an interest that they wanted to pursue this avenue as a way to reduce the cost of the device, because the programmable nature added additional test costs, because they had to test both features or three -- however many features there were, they had to test all

A. Yes, I did.

Q. If I could direct your attention, please, to page 34.

A. Okay, I have it.

Q. This is a page with the title Future SDRAM Features Survey Ballot.

Do you see that?

A. Yes see it.

Q. If I could direct your attention to the third bullet point, "Take the Time to Do It Right." Based on MOSAID's presentation of the discussion that you observed at the time, did you have an understanding of what was meant by "take the time to do it right"?

A. MOSAID was proposing that in creation of a next generation device that we take our time, we use special task group meetings and put a number of people together to develop the next generation of device, and so take your time to do it right was Mr. Allen's approach to having the information -- having the feature set and functionality of the next generation device go under a lot of scrutiny for as long as it took to get it right, so to speak.

Q. Can I direct your attention to the last bullet point on that page, please, "Create another Standard that will Stand the Test of Time."

Do you see that?

A. The last bullet item?

Q. Yes.

A. Yeah, "Create another Standard that will Stand the Test of Time"?

Q. Yes.

A. Yes, I see it.

Q. Based on your observation of the presentation of the MOSAID survey ballot and other discussions, did you have an understanding of what was meant by "create another standard that will stand the test of time"?

A. Yes, the intent of saying what was said here was that it's essentially based on taking the time to do it right. If you invest the proper amount of time and the proper amount of resources, then you will create something that is serviceable in the industry for a long period of time, and so in that sense, stand the test of time. Time in the electronics industry is a relative term.

Q. If I could direct your attention to the next page, page 35. Under heading 4, Conclusions, 4.1, Issues with Strong Support (>2/3)," do you see that?

A. Issues -- yes.

Q. If I could direct your attention down about nine bullet points down, it reads, "On chip PLL/DLLs to

reduce clock access time."

Do you see that?

A. Yes, I do.

Q. I think before I ask the next question, before this meeting, did you actually receive a copy of the survey ballot?

A. Yes. Before the meeting? Yeah, the way survey ballots actually work is the survey ballots were sent out along -- some period of time in advance. People had the opportunity to look over them and make comments, and survey ballots were intended to gather information so we could gauge a sense of the direction that we should take.

Q. Did you review this survey ballot when you received it?

A. Yes, I did.

Q. Based on your review of the survey ballot and the presentation by MOSAID on the results of the survey ballot, as of December 1995, did you have an understanding of the reference to on-chip PLL/DLLs to reduce clock access time under 4.1?

A. Yes, I did.

Q. What was your understanding at the time?

A. My understanding was similar, in fact, to the presentation that had been made by NEC in earlier

presentations and discussed inside the committee. The use of the PLL/DLL, and you see it here used as interchangeable terms, because sometimes we would argue about which term was which, and so finally we decided it didn't matter. So, the PLL/DLL, as it's referenced here, actually showed up as a method to allow us to synchronize the internal clock of the device with the external clock.

Q. How did this particular feature get on the survey ballot in the first place?

A. Well, everything that shows up in a survey ballot is either from a presentation or from an earlier discussion that takes place in JEDEC. Usually what happens is feature sets come around, they come up through discussions, and especially when it starts taking an inordinate amount of committee time, we will say, look, let's take some of these items, put them in a survey ballot, and see if we can gauge the level of support, see if we can identify a direction that we might want to go. So, the short answer to your question is this came from earlier discussions that took place inside JEDEC.

Q. If I could direct your attention back to page 6, please.

A. Page 6?

Q. Yes.

A. Okay.

Q. Again, under 8.8, SDRAM Feature Survey Ballot Results, and after Attachment G, it reads, "MOSAID noted that they had a patent pending on DLL and noted that it was a particular implementation and may not be required to use the standard."

Do you see that?

A. Yes, I do.

Q. Do you have an understanding as to how that item came to be raised at a JEDEC meeting?

A. As is typically the case, somebody would stand up and say, hey, look, we have some IP related to this area, as Mr. Allen did in this case, and it would be normally listed to where it can be referenced, and his statement is it may be required -- it may involve the work that's going on. His discussion about it was that it was very specific, so it may only apply to a particular implementation.

Q. If I could direct your attention again back to page 35, please.

A. Okay.

Q. Towards the bottom of the page, on 4.2, Issues with Mixed Support, the fourth bullet point.

A. 4.2, okay.

Q. The fourth bullet point reads, "Using both edges of the clock for sampling inputs."

Do you see that?

A. Yes.

Q. Again, was that an item that you had seen in the survey ballot itself?

A. That is correct.

Q. Based on your review of the survey ballot and the presentation on the results by MOSAID that took place in that meeting, did you have an understanding in December 1995 what was meant by using both edges of the clock for sampling inputs?

A. Yes, I did.

Q. Based on your understanding in December 1995, what, if any, differences were contemplated by the proposal to use both edges of the clock as included in the survey ballot as opposed to the IBM presentation of dual edge clock in April 1992?

A. Well, in operation -- and the utilization of both edges of a clock to do work is -- is and was a common discussion, and on the survey ballot and as presented in Mr. Hardell's position from IBM, it's extremely similar. If not exactly the same, certainly similar.

MR. OLIVER: Your Honor, at this time, I would

like to actually on a timely basis offer JX-28 into evidence, please.

JUDGE McGUIRE: Mr. Detre?

MR. DETRE: No objection.

JUDGE McGUIRE: So admitted.

(JX Exhibit Number 28 was admitted into evidence.)

BY MR. OLIVER:

Q. If I could ask you to find JX-29 in your pile, another set of meeting minutes, this time from a 1996 meeting.

A. Okay.

Q. Do you recognize JX-29?

A. Yes, I do.

Q. What is that document?

A. This is an interim committee meeting for the JC-42.3 in January 1996.

Q. What is an interim meeting?

A. As I explained, we have four regularly scheduled meetings per year, and often times during high levels of activity, we schedule meetings in between those other meetings, and this would have been one of those meetings, sometimes called special meetings, sometimes called interim meetings. They're called interim because they're between two other

meetings, two regular meetings.

Q. Were you present at the January 1996 interim meeting?

A. Yes, I was.

Q. I'd like to direct your attention, please, to page 4 of JX-29.

A. Okay.

Q. Specifically, if I could direct your attention to item 6.2, Micron Future SDRAM Clock Issues.

Do you see that?

A. 6.2, yes, I do.

Q. Now, what did this item refer to?

A. This would have -- this was a presentation made by Micron at the meeting and would be included here in Attachment F.

Q. Were you present at the meeting when Micron made the presentation?

A. Yes, I was.

Q. Did you observe Micron's presentation?

A. Yes, I did.

Q. What was Micron's presentation about?

A. Micron's presentation was about the topic that you see here, the SDRAM clock and issues that they had with the clock itself.

Q. Could I ask you to turn to Attachment F,

please. I believe you'll find it at page 17.

A. I'm in the middle -- okay, 17.

Q. Is this the Micron presentation that was made at the January 1996 meeting?

A. That is correct.

Q. Based on your observation of the presentation and any related discussions, as of January 1996, did you have an understanding of what was referred to by PLL/DLL circuits?

A. Yes.

Q. Could you please explain what your understanding was as of January 1996?

A. That DLL/PLL circuits or that PLL/DLL, as it's listed here, were circuits that were intended to be used to adjust the phased relationship between the outside clock of the device and the inside clock of the device.

Q. Was Micron proposing to place the PLL/DLL circuits on the DRAM chip or outside the DRAM chip or elsewhere?

A. Well, actually, Micron was proposing that -- they were identifying that there's two separate approaches. There's another way to essentially do the same type of thing. So, Micron was proposing an alternative way.

Q. Thank you, it was an imprecise question on my part.

The PLL/DLL circuit that Micron was referring to in its comparison, was it referring to an on-chip PLL/DLL or PLL/DLL located elsewhere?

A. Oh, yes, it was an on-chip PLL/DLL that they were referring to.

Q. What was Micron actually proposing with its presentation?

A. Well, as you can see, the first two page, they say there's two different objectives, the PLL/DLL, and they gave some description, and they show echo clock, which is another methodology to accomplish synchronization of data, which was the ultimate goal of the PLL/DLL.

Q. What is an echo clock?

A. An echo clock is just another methodology of creating some method to determine when data would be arriving and data would be valid.

Q. Was Micron proposing echo clock as an alternative to on-chip PLL/DLL?

A. That was part of the presentation they were making. They were making a proposal so you could see that there are issues with both of them, there's advantages and disadvantages. I'm not sure that they

necessarily said exactly which one they would like to do, but certainly they -- by presenting the differences here, they wanted to bring up the discussion such that we could have it inside the committee.

If you look at their conclusion foil at the end, you can see that they -- they conclude that there is some -- the word that they use is overwhelming. And it's a recommendation, work added they said.

Q. You are referring to on page 22?

A. Yes, I am.

Q. Now, based on your understanding of the JEDEC disclosure policy as of January 1996, was it your understanding that the Micron presentation at Attachment F would have triggered the JEDEC disclosure policy?

A. Certainly, any activity that takes place inside the meeting, and this is a presentation that was made in a meeting, and so certainly it would have triggered.

Q. You referred to any activity. Could you explain that?

A. Oh, discussions, presentations, ballots, anything that's taking place inside the committee is what will trigger -- when we're having a topic discussed, and certainly they would be discussing about presentations, because this would be somebody

physically standing up there and showing their work, and a discussion would be taking place in the committee.

MR. OLIVER: Your Honor, I'd like to offer JX-29 into evidence.

JUDGE McGUIRE: Any objection?

MR. DETRE: No objection, Your Honor.

JUDGE McGUIRE: Entered at this time.

(JX Exhibit Number 29 was admitted into evidence.)

BY MR. OLIVER:

Q. Mr. Rhoden, could I please ask you to find JX-31 in the pile in front of you? It's another set of meeting minutes, this time from March 1996.

A. I have it.

Q. Do you recognize JX-31?

A. Yes, I do.

Q. What is it?

A. This is meeting minutes from JC-42.3 from March 1996.

Q. Were you present at this meeting?

A. Yes, I was.

Q. If I could direct your attention to page 64, please.

A. Okay.

Q. Do you recognize the document appearing at page 64?

A. Yes, I do.

Q. What is it?

A. This is actually a presentation that I made about future DRAM possibilities, proposals, if you will. Feature sets, how's that?

Q. When you made this presentation, were you intending to direct this presentation towards a revision of the past SDRAM standard or towards a future standard?

A. Well, you could consider -- as -- recall, as I said, when a presentation is made, the committee can decide either way, but in terms of this particular presentation, it was intended to be for a future DRAM standard, because what you see here is a change in the interface level. At the very top, under SDRAM Features, it says LVTTL, and the next line over that has the arrow that says SSTL3. That would be a change of interface levels of the device and so necessarily would indicate a new device.

Q. If I could direct your attention to the caption Function on the left-hand side. Do you see that?

A. Yes.

Q. Underneath that it says, "CAS latency."

Do you see that?

A. Yes, I do.

Q. What were you intending to propose with your reference to CAS latency there?

A. It's actually showing CAS latency, we -- that various frequencies of operation, perhaps we needed more than the two values that we were then using, which was two and three. Perhaps we would need to add three and four, four and five, at future frequencies.

Q. Did you propose any particular method of determining the CAS latency?

A. I did not.

Q. Did you have any understanding as to what the method to determine the CAS latency likely would have been?

A. Well, actually, in this case, by this time we were already utilizing and shipping the programmable mode register to determine CAS latency, so I didn't include that here, because it was already assumed that that's where we would handle it. I was merely proposing some additional values that we consider.

Q. Just to be clear, it was assumed that programmable CAS latency would be continued for use in the next standard, is that what you're saying?

A. Oh, yes, certainly.

Q. If I could direct your attention to the last function on the list, the burst length.

A. Yes.

Q. Again, what were you intending to propose with respect to burst length?

A. Actually, it was -- the proposal was that the demand for two, four and eight continues for a long time, and so the proposal was to continue the same programmable nature of two, four and eight throughout the future devices themselves.

Q. If I could direct your attention to the sixth item, it reads, "On Chip PLL/DLL."

Do you see that?

A. Yes.

Q. What were you intending to propose with that reference?

A. My proposal was that as we went to higher frequencies, perhaps we would want to include a PLL/DLL as a method of phase adjusting the clocks inside of the devices.

Q. Did your proposal favor either a PLL or a DLL?

A. No, you can see it says PLL/DLL. I -- remember, I used the term, as did others, interchangeably. I did not distinguish between PLL and DLL.

Q. Based on your understanding of the JEDEC disclosure policy in March of 1996, did your presentation constitute JEDEC work?

A. Yes, it did, certainly.

Q. And would your presentation have triggered any disclosure obligation?

A. Yes, it would have, certainly.

MR. OLIVER: Your Honor, I see it's 5:00. This is probably a good breaking point.

JUDGE McGUIRE: Okay, very good, Counsel. This hearing then is adjourned until 9:30 a.m. on Friday. Thank you very much, everyone. Have a good evening.

(Whereupon, at 5:00 p.m., the hearing was adjourned.)

C E R T I F I C A T I O N O F R E P O R T E R

DOCKET NUMBER: 9302

CASE TITLE: RAMBUS, INC.

DATE: MAY 1, 2003

I HEREBY CERTIFY that the transcript contained herein is a full and accurate transcript of the notes taken by me at the hearing on the above cause before the FEDERAL TRADE COMMISSION to the best of my knowledge and belief.

DATED: 5/2/03

SUSANNE BERGLING, RMR

C E R T I F I C A T I O N O F P R O O F R E A D E R

I HEREBY CERTIFY that I proofread the transcript for accuracy in spelling, hyphenation, punctuation and format.

DIANE QUADE