FEDERAL TRADE COMMISSION

I N D E X

FEDERAL TRADE COMMISSION

I N D E X (cont'd)

UNITED STATES OF AMERICA

FEDERAL TRADE COMMISSION

In the Matter of:	)	
Rambus, Inc.	)	Docket No. 9302
----------	)	

Monday, May 12, 2003

9:30 a.m.

TRIAL VOLUME 8

PART 1

PUBLIC RECORD

BEFORE THE HONORABLE STEPHEN J. McGUIRE

Chief Administrative Law Judge

Federal Trade Commission

600 Pennsylvania Avenue, N.W.

Washington, D.C.

Reported by: Sally Jo Bowling

APPEARANCES:

ON BEHALF OF THE FEDERAL TRADE COMMISSION:

GEOFFREY OLIVER, Attorney
JOHN C. WEBER, Attorney
SUZANNE MICHEL, Attorney
Federal Trade Commission
601 New Jersey Avenue, N.W.
Washington, D.C. 20580-0000
(202) 326-3663

ON BEHALF OF THE RESPONDENT:

GREGORY P. STONE, Attorney
STEVEN M. PERRY, Attorney
PETER A. DETRE, Attorney
SEAN GATES, Attorney
Munger, Tolles & Olson LLP
355 South Grand Avenue, 35th Floor
Los Angeles, California 90071-1560
(213) 683-9255

APPEARANCES:

ON BEHALF OF THE RESPONDENT:

A. DOUGLAS MELAMED, Attorney
Wilmer, Cutler & Pickering
2445 M Street, N.W.
Washington, D.C. 20037-1420
(202) 663-6090

P R O C E E D I N G S

- - - - - -

JUDGE McGUIRE: This hearing is now in order. Before we get started today, are there any housekeeping tasks we need to concern ourselves with or can we proceed?

MR. OLIVER: Not at this time, Your Honor.

JUDGE McGUIRE: Mr. Stone, anything on behalf of respondent?

MR. STONE: None, Your Honor.

JUDGE McGUIRE: Then you may call your next witness.

MR. OLIVER: Your Honor, Ms. Suzanne Michel will handle the next witness on behalf of complaint counsel.

JUDGE McGUIRE: Okay, thank you. All right, Ms. Michel? And then how is that spelled, Ms. Michel?

MS. MICHEL: It's M I C H E L. Your Honor, complaint counsel calls Mr. Mark Nusbaum to the stand.

JUDGE McGUIRE: Mr. Nusbaum, please approach and remain standing while you're sworn by the court reporter.

Whereupon--

MARK E. NUSBAUM

a witness, called for examination, having been first

duly sworn, was examined and testified as follows:

DIRECT EXAMINATION

BY MS. MICHEL:

A. In 1969, I received a Bachelor of Science degree in electrical engineering from the University of Marylandã. In 1974, I received a juris doctorate degree from the American University's Washington College of Law.

Q. Did you graduate with honors from the electrical engineering program at the University of Maryland?

A. Yes, I did.

Q. Were you elected to honor societies there?

A. I was elected to the General Engineering Honor Society and the Electrical Engineering Honor Society.

MR. STONE: Your Honor, in Ms. Michel would like, we would be happy to stipulate the three topics Mr. Nusbaum has identified in his intended testimony

Trademark Office for 17 years in various capacities, and on virtually a daily basis for those 17 years, I was either personally examining or involved in patent examining activities.

Q. And when did you first start with the patent office?

A. I started with the Patent & Trademark Office in July of 1969.

Q. When you did first start at the patent office, were you assigned to examine any particular types of patent applications?

A. Yes, I was assigned to examine patent applications in the so-called art unit and was responsible for examining general purpose digital data processing systems related applications and special purpose digital data processing systems patent applications.

Q. In what years were you assigned to the art unit that examined those types of applications?

A. From 1969 through 1980.

Q. What were your duties during that time?

A. My duties during that time were essentially to examine patent applications. I would estimate that over that time frame I examined somewhere in the neighborhood of between 700 and a thousand patent applications in

this art area. Later on during -- in the latter part of that time frame, I was also involved, to some extent, in supervising junior patent examiners.

Q. You mentioned that you examined patent applications in the general computer art -- of general computer systems. Could you please just briefly explain what you mean by that, what kind of applications were involved?

A. The kind of applications that were involved in terms of general technological subject matter were with respect to the general purpose digital data processing arts. I examined patent applications that related to any particular subsystem of a computer system, such as the central processing unit or the storage subsystem. I examined applications related to multiple computers, so-called multiprocessor systems. In special purpose data processing art, I examined patent applications relating to, for example, display processing systems, printer control systems.

I recall having personally examined the very first entire computer that was fabricated on a single semiconductor chip. I also examined a number of the very first microprocessor related patent applications.

Q. And how does this general technological subject matter that you examined compare with the subject matter

examining requires more than an undergraduate level degree of knowledge to understand, and then secondly, after a grilling by a patent office committee, it has to be determined that the particular candidate has mastered that technology.

Q. Did you receive a master's level rating in the art area which you examined?

A. Yes, I did. That was in early 1975.

Q. Could you please explain what a primary examiner is?

A. A primary examiner is a patent examiner who has been granted the authority by the Patent & Trademark Office to either finally reject a patent application or to allow a patent application to mature into an issued patent over his or her own signature.

Q. Did you become a primary examiner?

A. I did. And that would have been somewhere in the vicinity of mid-1975.

Q. Did you ever receive the senior examiner rating in the computer art system area which you examined?

A. Yes, I did. In 1977.

Q. What does that rating mean?

A. A senior examiner rating is not necessarily a rating which is awarded to a person who is most senior in a particular art area. In essence, it's an

indication that the examiner's supervisor viewed that particular examiner as being the most knowledgeable patent examiner in that examining art area.

Q. Did you at some point become a supervisory patent examiner?

A. I did, in 1980.

Q. What were the responsibilities of a supervisory patent examiner?

A. A supervisory patent examiner is charged with the responsibility of managing an examining art unit which are now referred to as technology centers, but there are a group of 10 to 15 to perhaps as many as 20 patent examiners, and the supervisory patent examiner is responsible for making sure that the quality of examination in the art unit remains as high as possible while the examiners achieve their expected productivity. A supervisory patent examiner's job to a large extent involves training new examiners, evaluating examiner work product and answering legal and technical questions either from the examiners in the art unit or the manager of a group of art units.

Q. What technological areas did you supervise?

A. I supervised the same general purpose and special purpose technological area, that digital data processing art area that I examined in. I also was

responsible for supervising an area that related to a vast array of applications of computers such as patient monitoring, measuring of testing systems, computers used in control systems. I was also responsible to a lesser extent for some multiplex communication technology.

Q. What position did you assume in the patent office after being a supervisory patent examiner?

A. In 19 -- in 1983, I was appointed to the United States Patent & Trademark Office's Board of Patent Appeals and Interferences.

Q. What was your title in that position?

A. My title at that time as a member of the Patent Office Board of Appeals and Interferences was examiner in chief. Today, members of the board are referred to as administrative patent judges.

Q. What is the Board of Patent Appeals and Interferences?

A. The Board of Patent Appeals and Interferences is a quasi judicial body within the Patent & Trademark Office, and the responsibility of the board is to decide appeals by patent applicants who receive two rejections or typically a final rejection from a primary patent examiner.

Q. Did you have to write opinions as a member of the board?

A. Yes, every appeal at the Patent & Trademark Office ends with a written opinion where the board panel either affirms or reverses the examiner's objections.

Q. Did any of the cases in which you heard at the board involve computer-related technology?

A. Yes. The unofficial segment of the Board of Appeals that I worked in was a group of five or six board members who handled appeals emanating from the electrical -- so-called electrical examining groups. The art area where I examined, the examining group where I examined was one of those groups, and as long as I wasn't personally responsible for any application, it was actually highly likely that I would have been assigned on panels that heard computer systems or storage technology related appeals.

Q. What options does a patent applicant have if the board of appeals affirms a patent examiner's final rejection of an application?

A. A patent applicant has the option to appeal directly to the Court of Appeals for the Federal Circuit or alternatively to initiate an action in the Federal

A. I would roughly estimate somewhere between 750 and a thousand appeals that I was involved in.

Q. And how many opinions did you draft?

A. I drafted somewhere on the order of 200 opinions.

Q. Were any of those appealed?

A. To the best of my knowledge, there were five that were appealed.

Q. What was the outcome in those cases?

A. I was fortunate enough to have been affirmed on all five.

Q. Did you receive any awards while you were at the Patent & Trademark Office?

A. Yes, I did. I received awards pretty much every year when I was personally examining patent applications and as supervisor I received quality step increase awards, and I also received the Commerce Department's Silver Medal Award.

Q. What was the basis for that Silver Medal Award?

A. The Silver Medal Award recognized my accomplishments from 1969 to 1979. I was also recognized for my efforts in reclassifying the computer arts, and I believe for training examiners as well.

Q. Did you have any teaching responsibilities within the PTO?

A. Yes, I did.

Q. What were they?

A. I taught on a number of occasions a course in the Patent & Trademark Office that was referred to as the patent examiner initial training course, and what this course was designed to do is to take brand new patent examiners who have had no on-the-job experience whatsoever and attempt to give them a solid ground in fundamental aspects of patent law, and patent examining process -- practice, pardon me. I also taught on a couple of occasions an in-house course relating to microprocessor technology.

Q. Mr. Nusbaum, did you ever serve as the chairman of any U.S. Patent Office committees?

A. Yes. I served as chairman of a patent office committee that was responsible for generating patent examining guidelines for determining the eligibility of patent applications that related to either computer programs or mathematical algorithms for patent protection, and I was the principal author of guidelines that were the result of that committee's work.

Q. Were you ever asked by the patent office to speak to members of the bar regarding patent office policy?

A. Yes, I was. I was asked to give lectures at

other litigations.

Q. Okay, thank you.

Your Honor, at this point I would like to ask the Court to recognize Mr. Nusbaum as an expert in patent office practice and in patent law.

JUDGE McGUIRE: Mr. Stone, any voir dire?

MR. STONE: No, Your Honor. Not as to those two topics.

JUDGE McGUIRE: Okay. So noted.

BY MS. MICHEL:

Q. Mr. Nusbaum, what is a patent?

A. A patent is a government grant in the nature of a contract between the patentee and the United States Government. The United States Government gives to the patentee a right to exclude others from making, using, selling or offering to sell a claimed invention for a limited period of time. In return, the patentee gives to the United States public a disclosure of a claimed invention that satisfies the requirements of the patent laws and adds to the United States technological base.

Q. What are the main parts of a patent?

A. The main parts of a patent include the written description of a claimed invention that's referred to as the patent specification. The patent specification concludes with one or more patent claims and in most

Q. Would you please explain how a patent examiner examines a patent application?

A. A patent examiner reads and studies an original patent application disclosure and -- including the claims, and the patent examiner does that in order to make sure that the disclosure satisfies the disclosure requirements of the patent law and to gain an understanding of the claimed invention.

The patent examiner then does a search of the prior art that he or she has access to within the Patent & Trademark Office. The patent examiner then compiles all the various objections and rejections that he or she may have in a communication, and that communication is referred to as an official action. The examiner then sends that official action to a patent applicant, typically through the patent applicant's patent attorney.

Q. How does the patent applicant typically respond to the office action?

A. Well, what the patent applicant does is to respond to each and every objection and rejection that was raised by the patent examiner, either by telling the examiner that, examiner, you're just wrong, for identified legal and technical reasons. The patent applicant may choose to amend, for example, the patent

application claims, and then this response will be sent in to the Patent & Trademark Office for the examiner's consideration.

Q. And what will an examiner typically do after receiving that response?

A. The examiner may be convinced by the arguments that are presented, and at that point, allow the patent application, if he or she has the requisite authority, or alternatively, the examiner may choose to reject again, which typically is a final rejection, the patent application restating the grounds of rejection.

Q. If the examiner finally rejects the patent applications, what options does the patent applicant have at that point?

A. The patent applicant has an option of filing a continuing application, an applicant has an option of appealing to the Patent & Trademark Office's Board of Patent Appeals and Interferences, the body that I was a member of.

Q. I think we'll talk about continuing applications again a little later. And what is the prosecution history of a patent application?

A. The prosecution history of a patent application is the patent office's file that's maintained during the examination process. It includes the original patent

application and it's a compilation of all the communications that are exchanged between the patent examiner and a patent applicant, either leading to the abandonment of that particular patent application, or to the issuance of that patent application.

Q. Let's talk a little now about the requirements for patentability. What requirements for patentability does an examiner most commonly rely on when he rejects an application?

A. A patent examiner most commonly relies on disclosure, requirements for patentability, adequacy of disclosure, claimed definiteness requirements, requirements for patentability over the prior art, that is to say that patent application claims must be both new and non-obvious variations of the prior art.

Q. You mentioned prior art, what is prior art?

A. That's actually quite a complicated question to answer fully. Prior art is defined by a section of the patent law 35 USC 102 and the various subparagraphs, and prior art most commonly may include properly dated United States patents or publications. Prior art, though, can also include commercial products that have been offered for sale or in public use more than one year prior to filing a patent application. Prior art can include the prior work of another that has not been

abandoned, suppressed or concealed, but at the risk of oversimplification, prior art may be thought of in general as prior technological developments that are public, that are at least prior to a patent application's filing date.

Q. What's the impact on patentability if the prior art subject matter falls within the scope of a patent claim?

A. If the prior art falls within the scope of a patent claim, then that claim is invalid. It's fundamental notion of patent law that you can't patent what's old. You can't get a right to exclude others from subject matter that already belongs or exists in the public domain.

Q. You also mentioned that examiners consider the adequacy of the disclosure. What are the requirements for the adequacy of the disclosure?

A. There are three requirements for adequacy of disclosure. There's a so-called enablement requirement, a written description requirement, and a best mode requirement. With respect to the enablement requirement, it's necessary that a patent application be set forth in such full, clear, concise and exact terminology that a person skilled in the art is enabled to make and use the claimed invention without having to

resort to undue experimentation.

With regard to the written description requirement, it's necessary that an original patent application disclosure provide support for later added claims subject matter, and what's meant by that is that it's necessary that the originally filed disclosure evidence that a patent applicant was in possession of the later claimed invention, as of the original filing date.

With regard to the best mode requirement, if a patent applicant has a contemplated best way of implementing a claimed invention, that must be disclosed in a patent application.

Q. You also mentioned that examiners consider the definiteness of the claims. What are the requirements for the claims to be definite?

A. Claims are required by statute to particularly point out and distinctly claim the invention. And that requirement is satisfied if the words of a claim circumscribe a particular area with a reasonable degree of precision and particularity such that the bounds of the invention are reasonably precise.

Q. Is it common practice for patent examiners to reject patent application claims as being indefinite?

A. Yes, it's extremely common for patent examiners

in an official action to reject claims based on indefiniteness. I hesitate to indicate a particular percentage, but it wouldn't surprise me if as many as 75 to 90 percent of cases where there is a rejection, that there will be an indefiniteness rejection. It's extremely common is the message I'm trying to give.

Q. Well, what in your opinion is the significance of this practice in the patent office?

A. The significance of this practice is that patent examiners are trained that a patent application is much

application claim is fatally flawed in that it violates this statutory requirement that the claims particularly point out and distinctly claim an invention. It's actually relatively rare, although it does happen, that claims are ultimately found to be indefinite, and invalid because of that.

Q. Mr. Nusbaum, do patent examiners operate under any time constraints?

A. Yes. Patent examiners do operate under time constraints. Every examiner in the Patent & Trademark Office is assigned a productivity quota defining the average time they have to spend on an average patent application.

Q. Did you personally have a productivity quota when you were examining applications in the computer system art?

A. Yes, I did.

Q. What was that?

A. When I was a primary patent examiner, my productivity quota was 23.4 hours, and what that means is that I was responsible for reviewing the patent application and claims, searching the prior art, drafting a first office action, reviewing examiners' responses, all the work that needed to be done, this is for an average patent application, was supposed to be

done in that period of time.

Q. We're going to turn now to the Rambus patent tree. We have both a blow-up exhibit to set on an easel, and also smaller copies for everyone to follow. I think we will mark it as a demonstrative. What are we up to?

JUDGE McGUIRE: I believe it will be DX-14 if I'm not mistaken.

MR. STONE: I believe that's right, Your Honor.

MS. MICHEL: Your Honor, may I approach and hand you a copy of the exhibit, also?

JUDGE McGUIRE: Please.

(DX Exhibit Number 14 was marked for identification.)

MS. MICHEL: Your Honor, do you have any preference as to where we place an easel with a blow-up on it? We are going to have several such demonstratives today.

JUDGE McGUIRE: Maybe right over here where I can see it and it can also be seen by opposing counsel.

MS. MICHEL: Thank you. Well, we have to make sure he can see it as well, and the witness.

MS. MICHEL: Yes.

BY MS. MICHEL:

Q. Well, luckily we all have small ones of DX-14.

parties have stipulated to the accuracy of the tree.

JUDGE McGUIRE: Mr. Stone, is that correct?

MR. STONE: Yes, Your Honor.

JUDGE McGUIRE: Okay, so noted.

BY MS. MICHEL:

Q. Mr. Nusbaum, please describe just very generally what the exhibit shows.

A. It may help if I can approach the exhibit.

JUDGE McGUIRE: Yeah, go ahead.

THE WITNESS: What this Rambus tree shows is in the upper left-hand corner of the tree, the very first filed Rambus patent application is designated which is application 07/510,898. This application was filed on April 18th, 1990. Every patent application and issued patent that's represented on this chart flows from this single first filed patent application.

On the right-hand -- along the right-hand margin of the exhibit is the year 1990, which is lined up with the filing -- the year of filing of the originally filed Rambus application, and then down the right-hand margin, the various years are indicated through 2003.

All the patent applications that -- well, first of all, the patent applications are indicated in this chart, if you take a look at the key, in blue. The patents, on the other hand, which matured from patent

applications to which they are linked on this tree are indicated in yellow, by a yellow rectangle, and the patents that have been asserted by Rambus in patent litigation are indicated by yellow rectangles circumscribed by red.

In the middle of this chart is a date indicating June '96 with a red dotted line, and this is the date that the FTC is alleging that Rambus ceased becoming a member of JEDEC.

BY MS. MICHEL:

Q. Mr. Nusbaum, I believe you said the patent applications shown on the chart flow from the '898 application. Can you explain what you meant by that?

A. Yes. Each of these applications is either what's referred to as a continuation application or a divisional application of the originally filed patent application.

Q. Okay, thank you. You can have a seat, please.

You just mentioned continuation application. What is a continuation application?

A. A continuation application is a patent application that names one or more of the inventors of a prior patent application that was filed during the pendency of the prior application. What I mean by pendency is while the prior application was pending

claims subject matter that is present in the current application, and that subject matter is filed with the divisional application.

JUDGE McGUIRE: Now I'm confused, again, just so I'm clear as to these two types of applications, you know, what's the chief distinction between the two that you have just testified on?

THE WITNESS: The chief distinction is that a divisional application will typically arise when a patent examiner looks at a parent application and decides that there's multiple inventions, multiple claimed inventions. And what the examiner does is sends a communication to the patent applicant that's called the restriction requirement, and requires the applicant to elect one of these groups of inventions. The applicant will prosecute in the original parent application the chosen or elected group of inventions. To those groups of inventions that aren't elected, the applicant may choose to file divisional applications which are directed to these different groups of claimed inventions that were not elected, or not chosen.

JUDGE McGUIRE: Is it fair to say that they are in their own right claims that emanate, you know, from a founding application? Are they claims within themselves?

THE WITNESS: Yes. That's correct. For example, an examiner may say that in an original application their claims 1 to 5 define one group of inventions and 6 to 10 define an independent and distinct group of inventions, and the examiner may -- the applicant may choose to prosecute in the original case claims 1 to 5, the applicant would then later file a divisional application that would be restricted to claims 6 to 10.

JUDGE McGUIRE: Okay. All right, go ahead.

BY MS. MICHEL:

Q. Did Rambus receive a restriction requirement during prosecution of the '898 application?

A. Yes. Rambus during the prosecution of the first filed application received an 11-way restriction requirement.

Q. And just very generally, what was Rambus' response to that restriction requirement?

A. Rambus chose to prosecute one of those 11 groups of claims in the originally filed '898 application, and then Rambus on I believe it was March 5th, 1992, filed 10 divisional applications. And if you see the first -- the line of 10 applications that are aligned by 1992, those are the 10 divisional applications that were filed on March 5th, 1992.

Q. In terms of identifying prior art, what's the significance that the applications on the Rambus patent tree are continuations on divisionals?

A. Presuming that the original application satisfies the disclosure requirements that I identified, the three disclosure requirements, and then if, for example, we're dealing with a patent application that unfortunately I can't identify specific applications due to my inability to read this, but let's just presume that a patent application, and there were some here that were filed in 1995. So, the individual filing date for that application, the actual filing date for that application is some time in 1995.

And then let's presume that there was a publication that arose of that exact same claimed invention in 1993. Let's presume it was anthat exact same claimed

Q. Okay, why would an applicant typically file a continuation application?

A. A patent applicant would file a continuing application for a number of different reasons. A patent applicant might receive a final rejection from a patent examiner, and decide that rather than appealing the final rejection to the board of appeals, that they would be better served by submitting further arguments to this same patent examiner. That could be done by filing a continuation application, paying a new government filing fee, and starting a process anew.

Also, continuing applications are filed to permit an original application to issue into a patent, and to seek claims that are of a different scope than the prior application. And in this fashion, build up a patent portfolio.

Q. Can events in the prosecution of a parent patent application impact a continuing application?

A. Yes. They surely can. With respect to commonly disclosed subject matter between a parent application and a continuing application, and in the case of the continuation application, there's an exact correspondence between the two specifications, typically, that the parent application and continuation application prosecution is treated as being a continuous

transaction before the Patent & Trademark Office.

So, the parent application prosecution may well be used, for example, to continue the claims of the continuing application.

Q. I would like to turn now to CX-1451, and it's the '898 patent application. Mr. Nusbaum, do you recognize this exhibit?

A. Yes, I do.

Q. And what is it?

A. This exhibit is the -- is a copy of the originally filed Rambus patent application that I pointed to that was in the upper left-hand corner of the Rambus patent tree, through which all the other patent applications flowed.

MS. MICHEL: Your Honor, we're going to distribute copies. Would you like a full copy of this exhibit?

JUDGE McGUIRE: Is it going to be on the ELMO? When you say copies, of what?

MS. MICHEL: The application itself is about 150 pages. We'll be looking at some specific pages.

JUDGE McGUIRE: No, I do not need a specific set. I can just view it off the ELMO.

MS. MICHEL: I think we will, however, distribute copies to opposing counsel, if they wish.

JUDGE McGUIRE: Yes, they would like that.

BY MS. MICHEL:

Q. Mr. Nusbaum, how many original claims were submitted with this application?

A. There were 150 original claims submitted with this patent.

Q. All right, and where are they located in the document?

A. Patent application claims are always towards the end or at the end of the patent specification, and in this case, if you look at page 63, the typewritten 63, which denotes page 63 of the specification, through page 124, are the original claims, the 150 original claims.

Q. Okay, I would like to start by looking at claim 1. With reference to claim 1, could you just explain to us the different components of a patent application.

A. You mean the different components of a patent application claim?

Q. Oh, I'm sorry, yes, excuse me. Could you just please give us a general explanation of the different components of a patent claim and use claim 1 as an example to illustrate the point.

A. Yes. Claim 1 is an example of a claim, and it begins -- it's a single sentence, it begins with a capital letter and ends with a period. The portions of

A. Claim 1 is an example of an independent claim. It stands on its own, it doesn't refer to any other claim. It's independent. On the other hand, claim 2 is a typical example of a dependent claim. It reads, "The memory subsystem of claim 1," and what that means is that you can treat claim 2 as if all the limitations of claim 1 were physically incorporated into claim 2, but claim 2 is dependent upon claim 1, and therefore it's referred to as a dependent claim.

Q. How are patent examiners trained that claims should be interpreted with respect to the patent application?

A. Patent examiners are trained that claims are not to be read in a vacuum, but rather that they must be interpreted in light of the patent specification. At the same time, patent examiners are also trained that they are not to import limitations from the patent specification into the claim that are not otherwise present in the claim.

Q. Is there a claim interpretation standard that patent examiners are required to use?

A. Yes, there certainly is. The claim interpretation standard that patent examiners are required to use is the broadest reasonable interpretation consistent with the specification.

Q. Could you please explain for us what that means?

A. Yes. The broadest reasonable interpretation standard that examiners are required to employ means that examiners are to view claimed terminology as broadly as they reasonably can view the terminology. For example, if there's a claim limitation that calls for a plurality of devices, and in the patent specification there are ten devices shown, the broadest interpretation of that terminology would be two or more. The examiner is trained not to be focused on the fact that the specification talks about 10. Similarly, with the term "memory device," the specification may describe certain types of memory devices, such as DRAMs or SDRAMs, but an examiner in interpreting memory device would look far more broadly at the term "memory device," and be trained to keep in mind to be looking for any type of memory device.

Q. Why is this claim interpretation approach used in the PTO?

A. This claim interpretation approach is used in the Patent & Trademark Office because it's very important that once a patent issues, and is asserted in a litigation, that a patentee doesn't assert an interpretation of a claim that's actually broader than what the patent examiner was using when he was searching

for the prior art in determining patentability with respect to the prior art.

If this standard were not employed, then, and examiners were viewing claims too narrowly and an applicant or patentee were to follow and interpret the claim broadly, what really may happen is that a patentee may be asserting a claim that an examiner, if he had a broader view, would recognize would be unpatentable over the prior art.

Q. Switching gears, are there any limitations of claim 1 that are essentially repeated in the majority of the 150 claims?

A. Yes, there definitely are.

Q. With reference to claim 1, what are those limitations?

A. In the context of referring to a bus, that carries substantially all address, data and control information, there's a limitation that said bus containing substantially fewer bus lines than the number of bits in a single address, and said bus carrying device-select information, without the need for separate device-select lines, connected directly to individual memory devices.

Q. Which of the 150 claims contain those limitations? Generally.

A. There are 20 independent claims among the 150 claims in this application. Eighteen of those 20 claims include at least one of these two what I'll refer to as multiplex bus limitations. Of those 18 independent claims, 16 of the independent claims include both those limitations.

Q. Do you recall which claims do not contain those limitations?

A. Yes. Claims 73 to 81 do not contain those limitations, and claims 91 to 94. There's two independent claims in those groupings, claim 73 is an independent claim, and claim 91 is an independent claim.

Q. Let's come back to that. First, looking at the limitation of claim 1, which recites, "Said bus containing substantially fewer bus lines than the number of bits in a single address," does the '898 patent specification describe that phrase?

A. Yes, it does.

Q. And do you recall where? Or can you give us an example?

A. Yes. If one turns to the summary of the invention. In the context of describing the present invention as opposed to an exemplary implementation, this is on page 7 of the specification, the summary of the invention.

Q. Okay.

A. It's stated that "The present invention includes a memory subsystem," and there's a discussion of the bus carrying substantially all address, data and control information. And then it's stated in lines 16 and 17, that "the bus has substantially fewer bus lines than the number of bits in a single address." Additionally, with respect to characterizing the buses having very few lines, towards the end of page 7, there's an indication that, "The new bus," going over to the next page, "Includes clock signals, power and multiplexed address, data and control signals." And then it's stated, "In a preferred implementation, 8 bus data lanes and an address valid bus line carry address, data and control information for memory addresses up to 40 bits wide."

So, there is an example there of the bus lines being substantially less than the number of lines in a single address.

Q. Does the detailed description of the invention section of this patent application provide any examples describing the phrase "substantially fewer bus lines than the number of bits in a single address?"

A. Yes. If one turns to the very first sentence of the detailed description of page 11 of the specification.

Q. And I believe that's page 13 in the exhibit.

A. There's an indication that "The present invention is designed to provide a high-speed multiplexed bus for communication." There is an indication in lines 22 to 23 that, "The bus consists of a relatively small number of lines," once again this theme of small number of lines connected in parallel to the bus. And then, at page 14 of the exhibit, at page 12 of the spec, there's a further example where it's indicated that, "Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024 bites) can be sent over a small number of bus lines (8 plus one control line in the preferred implementation.)"

BY MS. MICHEL:

Q. Now turning to the other implementation of claim 1, which you identified, which I believe you said stated the bus carrying device-select information without the need for device-select lines, does the '898 patent specification describe that phrase?

A. Yes, it does. Once again, at page 9 of the exhibit, and the summary of the invention, and once again in the context of describing the present invention as opposed to an exemplary implementation, the present invention is described as including, and this is in line

17 through 19, that, "The bus carries device-select information without the need for separate device-select

indicates more specifically what this system covers in a dependent claim context, and that is claim 78, which indicates that "A semiconductor device has an internal device clock generating means to derive the midpoint time between set early and corresponding late bus clock signals and to generate an internal device clock synchronized to said midpoint in time." So, the result is that there is an average clock signal that is generated.

Q. If you will now please turn to claim 91. You mentioned that this claim also does not contain the two limitations that we discussed. What generally does this claim cover?

A. Claim 91, as indicated, in the claim preamble, is directed to a package, the package contains a semiconductor die, and the next paragraph there's an indication that the package comprises a plurality of bus connecting means for connecting to a plurality of external bus lines. There are some other limitations, but at the end of the claim there's the requirement that "each of the external bus lines can be connected to said corresponding connecting area on the semiconductor die by bus connection means that are positioned along a single side of the package."

MS. MICHEL: Your Honor, I would like to request

complaint counsel's case.

JUDGE McGUIRE: All right, then I'll entertain.

MR. STONE: Your Honor, my point is it's not in dispute.

JUDGE McGUIRE: It's not in dispute, but as an aid to the court, I will entertain the answer. Go ahead.

BY MS. MICHEL:

Q. Thank you.

Mr. Nusbaum, could you explain, please, the basis for your belief that the original 150 claims do not cover JEDEC-compliant SDRAMs?

A. Yes. With respect to the 18 out of the 20 independent claims, that is all claims except for 73 to 81, and 91 to 94, as I testified, there are claim limitations of one out of the two multiplex bus related limitations that I identified. More particularly, there's a limitation in the context of a bus that carries substantially all address data and control information, that that bus contain substantially fewer bus lines than the number of bits in a single address.

Looking at Mr. Rhoden's presentation, one could see a wide bus that did not have substantially fewer bus lines than the number of bits in a single address. Additionally, with respect to the second so-called

multiplex bus limitation, there's a requirement that the bus carrying device-select information, without the need for separate device-select lines that are connected directly to individual memory devices. Well, as we saw in the JEDEC presentations by Mr. Rhoden and also by Mr. Williams, that there's chip select lines that are involved in a JEDEC-compliant SDRAM that are indeed connected directly to individual memory devices.

So, with respect to 18 out of the 20 independent claims, in all claims but 73 to 81 and 91 to 94, those limitations form a basis for why they cannot cover a JEDEC-compliant SDRAM.

what a reasonable patent attorney or engineer would have understood about the original patent application, which was public as of 1993 or earlier. And I believe that testimony from an expert like Mr. Nusbaum about how a reasonable patent attorney would have viewed that patent application is, in fact, relevant to that issue.

MR. STONE: Your Honor, that's not the issue we've put in the case, but even if it were the issue that we put in the case, that doesn't go to the question of whether inventors would confer with their patent attorney, and that's the question pending. And in this

lawyers did or did not carry out what they're required to do by whatever the standard of care is, and in this case, if they did confer or didn't confer, that would be a matter of fact. There's no purpose for having opinion testimony as to whether an attorney should or should not talk to the inventors.

MS. MICHEL: Your Honor, perhaps I can rephrase the question in a way that alleviates the objection.

JUDGE McGUIRE: Okay, go ahead.

BY MS. MICHEL:

Q. Mr. Nusbaum, would a reasonable patent attorney reading the '898 application and the original 150 claims have expected the patent attorney involved in the application to have conferred with the inventors?

MR. STONE: Your Honor, there are two part objections. I mean, first, there's still no reason for whether somebody would assume that you have conferred

ultimately issue.

JUDGE McGUIRE: Well, now he has been qualified as an expert in two areas, patent law practice and patent law. So, I would assume that under either of those criteria, he should be allowed to answer that inquiry.

MR. STONE: No, because this is neither a question of patent law, this is not an issue of patent law, he has talked about the law, this is an issue about what people would do upon seeing an application.

JUDGE McGUIRE: How about patent law in the practice?

MR. STONE: No, this is not the practice of patent law. This is something that most often is done as the facts will bear out by engineers. It's not the practice of patent law. He doesn't as part of his practice conduct investigations where he looks at published patent applications and tries to advise people on the ultimate scope of claims that may issue. And he was asked this at his deposition, he says I can't remember ever having done it. So there's no --

MS. MICHEL: Your Honor --

JUDGE McGUIRE: I'll give you a chance, Ms. Michel, let him finish.

MR. STONE: So, there is no basis in his

expertise or his experience to offer this opinion.

JUDGE McGUIRE: All right, Ms. Michel?

MS. MICHEL: Your Honor, I think Mr. Stone's reading much more into the question than actually exists. I am not asking Mr. Nusbaum to testify to anything about claims that might come out of the specification, and nor will I in the following questions. The question was simply directed towards how a patent attorney seeing the original '898 specification, which was public at one point, would understand about a consultation. I think that the follow-up question will go to that.

JUDGE McGUIRE: I will entertain the objection, I will overrule the objection. You can take it up on cross examination, if you please.

MS. MICHEL: Could I ask the court reporter to read back the question I asked.

(The record was read as follows:)

"QUESTION: Mr. Nusbaum, would a reasonable patent attorney reading the '898 application and the original 150 claims have expected the patent attorney involved in the application to have conferred with the inventors?"

THE WITNESS: Yes. I --

MR. STONE: Your Honor, all he's been asked to

statistical study to determine how many inventors confer with their attorneys before patent applications are filed?

A. No, I have never conducted any such statistical study, nor am I aware that any exists.

Q. Is there any requirement of the patent office that a patent attorney certify amount of time he has spent talking to the inventor before he files an application on his behalf?

A. Of course not.

Q. Can a patent attorney write an application and submit it to the patent office consistent with the rules of conduct, without meeting and conferring with all the inventors?

A. It is possible, yes.

Q. And in your experience, have you ever set up two stacks of patent applications, those that have been written without conferring with the inventors and those that have been written after conferring with the inventors and performed some sort of study that lets you look at those applications and determine from their content whether the attorney did or did not confer with the inventors?

the application whether the inventor had consulted with the lawyer who prepared it or not. He says there's no way of knowing. And I think that establishes that there's no basis for him to express an opinion by looking at the '898 application as to whether you would assume that there had or had not been such consultation.

JUDGE McGUIRE: Again, I am going to let you take that up on any cross examination. I think that's where that ought to lie. Go ahead, Ms. Michel.

FURTHER DIRECT EXAMINATION

he or she can in order to make sure that claims are formulated that give an applicant the protection that the applicant merits when considered in light of the prior art that the patent -- that the inventor is aware of, as well as the patent counsel.

And in light of the massive effort that was undertaken, it's at least my presumption that a reasonable patent practitioner would have conferred with the inventors to get the benefit of the inventors' insight as to what the unique aspects were of the invention, in light of the prior art.

Q. Does the '898 patent application provide any indication to a reasonable patent attorney reading that application that the claims were drafted with prior art in mind?

A. Yes. At page 3 of the specification, that's the typewritten 3, there's a section called Comparison with Prior Art, and there is a discussion of somewhere on the order of 14 patents from pages 3 through the top of page 6 of the specification.

Q. In your view, would a reasonable patent practitioner reviewing the '898 patent application have presumed that the original claims included unnecessary limitations?

MR. STONE: Objection, Your Honor. Again, this

is a topic of which this witness has never expressed any experience or expertise as to whether looking at someone else's application you could draw inferences as to what the lawyer drafting the application had in mind. He never testified that that's something that he's done in his experience, it's outside his area of expertise.

JUDGE McGUIRE: I think that's your same opposition that you just made, Mr. Stone, that was overruled. So, I'm going to overrule this one as well.

BY MS. MICHEL:

Q. Would you like the question read back?

A. I think I have it. In my opinion, a reasonable practitioner would not have presumed in this particular case that there were unnecessary limitations in the original claims. The original claims are permeated, as I previously testified, by two multiplex bus limitations that we went over that appear in 18 out of the 20 independent claims. In wrestling with when those limitations are likely to be unnecessary limitations, in the summary of the invention, those two limitations in the very first paragraph of the summary of the invention are characterized as being the present invention and are identified expressly, those two limitations. They're not characterized as merely being exemplary implementations.

So, they are featured limitations that I don't believe would be regarded or be presumed to be unnecessary that could be eliminated. Additionally, because of the very large number of claims, 150 claims, and the associated massive effort that would have been presumed to have gone into those claims, including the analyzing the prior art, in my view, a reasonable practitioner would not have presumed that there were unnecessary limitations.

Q. Have you formed opinions about certain of those applications that were pending before the patent office prior to June 1996?

A. Yes, I have.

Q. Please just generally state your opinion with regard to those applications.

JUDGE McGUIRE: All right, I'm going to ask you to -- that question is a little too broad. I want you to be more detailed in the question. I don't want a long narrative answer here to such a broad question.

BY MS. MICHEL:

Q. I'll withdraw that question.

Mr. Nusbaum, have you identified any Rambus patent applications that in your opinion contain claims covering the programmable burst length and programmable cast latency features of JEDEC-compliant SDRAMs, and

A. Yes, I do.

Q. Will you please just generally describe what it is?

A. This is the prosecution history of Rambus U.S. serial number 08/910,810, and it includes within it the prosecution history of the applications that I identified, application 847,961, and application 469,490.

Q. When was the '961 application filed?

A. The '961 application was one of the ten divisional applications that I identified, and it was filed on March 5th, 1992.

Q. And what is the relationship between the '961 and the '898 applications?

A. As I indicated, the '961 application is a divisional application of the parent '898 application.

Q. Did the original claims of the '961 application cover SDRAMs that were compliant with JEDEC Release 4 standard?

A. No, they did not.

Q. Could you please explain why they did not.

A. The original claims in the '961 application were claims 95 through 104 of the original claims, and as I previously testified, claim 95, for example, included the two multiplex bus limitations that I identified, and

that is to say that the bus has substantially fewer bus lines than the number of bits in a single address and without the single direct line connected to individual semiconductor devices, and then in addition claim 95 required that there be at least one modifiable identification register that uniquely identifies a that identification register notfies a

meaning when you say a claim has been replaced?

THE WITNESS: Actually the original claims were cancelled and the term of art replaced is used in its ordinary sense, they were replaced with other claims.

JUDGE McGUIRE: All right.

BY MS. MICHEL:

Q. Since filing the '961 application in March 1992, had Rambus made any changes to the application prior to this January 1995 amendment?

A. No, there had been no prior changes to the claims before this January 6, 1995 amendment.

Q. Does the amendment itself give any indication of what prompted Rambus to file it?

A. On the face of the amendment, the first page, there is an indication that this amendment is -- in the very first line -- "In response to the office action," that is an office action from the Patent & Trademark Office, "mailed September 6, 1994."

Q. Was that the first office action issued by the examiner in the '961 application?

A. Yes, it was.

Q. In your opinion, which of the claims added in the January 6, 1995 amendment covered JEDEC-compliant SDRAMs?

A. Claim 160 and claim 164, as well as claims 151,

159, 165 and 168.

Q. Let's start by looking at claim 160. I believe that's at page 221 of the exhibit. How does claim 160 compare to original claim 103?

A. Claim 103, as I just testified to, had the limitation of -- well, I better turn to 103 so I don't misquote the language. Had the limitation of "a bus that has substantially fewer bus lines than the number of bits in a single address."

If one looks through claim 160, there's no such limitation that the claim had been broadened in that regard, and that the limitation with respect to the bus just indicates that it's a memory storage system including a bus, there's no such narrow bus limitation.

In addition, claim 103 referred to an access time register. The claim 160 was broadened so as not to be limited to an access time register, but as one can see, beginning at line 5, "At least one register that's operative to store information, specifying a manner in which the semiconductor device is to respond."

Q. You also mentioned claim 164, what's the relationship between claim 164 and claim 160?

A. Claim 164 is a dependent claim, and it is -- it is dependent upon claim 160, and as I previously testified, it should be treated as if all the

limitations of 160 are incorporated into 164.

Q. Mr. Nusbaum, I would now like to ask you to turn to JEDEC Release 4, it's been previously marked as JX-56. And in particular, if you will turn to the exhibit page 114 that's Bates 7793.

What's your understanding of what is shown here?

A. What's shown on this page, as indicated by the title of the page, is the SDRAM Mode Register aspect/feature of the JEDEC Release 4, and there's a number of characteristics of this mode register that are specifically enumerated. One is that the register is located on the SDRAM chip, and it's indicated -- there is an indication that its purpose is to store mode of operation data, so it determines what mode the SDRAM is operating in. There's an indication that the data is written after power-on and before normal operation, so my understanding is that this register is permitted to be programmed, and that it is written and it's programmed during a configuration time period to determine the mode of operation.

And then more specifically there is an indication of what the data in this mode register relates to, and then it's listed as burst length, burst type, and cast latency. And there is an indication that while operating in one mode, and for example burst of

four in sequential addresses, it can change to burst of eight in interleaved address modes, so that indicates the matters in which the SDRAM may respond to requests.

With respect to the writing of data, there's an indication two pages further in this Release 4 that indicates that data is written via the address bus.

MS. MICHEL: Your Honor, we're going to be using several demonstratives in the coming testimony, and I would like to hand our copies of the demonstratives to both you and opposing counsel.

JUDGE McGUIRE: Go ahead.

MS. MICHEL: Thank you.

BY MS. MICHEL:

Q. Mr. Nusbaum, let's turn to block diagram demonstrative previously been marked as DX-4.

Your Honor, I think it should be the first one in the stack of block diagrams that I gave you.

JUDGE McGUIRE: I'm sorry, it's been marked as what, DX-4?

MS. MICHEL: It had been previously marked during Mr. Williams' testimony as DX-4.

JUDGE McGUIRE: Okay.

BY MS. MICHEL:

Q. Mr. Nusbaum, please explain your understanding of what DX-4 shows.

A. DX-4 is a block diagram that I prepared, and whose accuracy was confirmed by Dr. Jacob, who did make some minor labeling changes with respect to certain of the buses that are shown. And the bottom portion of this figure was extracted from Dr. Jacob's expert report that just shows a JEDEC Release 4 style SDRAM memory

as specifying burst length for read and write requests, specifying burst type for read and write commands, and specifying the timing of DRAM array response to a read command in regard to the latency.

Q. Now, Mr. Nusbaum, I would like you to explain the basis for your opinion that claims 160 and 164 cover SDRAMs compliant with the JEDEC Release 4 standard.

A. I have prepared a claim chart that may be helpful in my demonstrating that.

MS. MICHEL: Your Honor, I will put the chart on the board, but also everyone has a smaller size of it.

JUDGE McGUIRE: Do we have a copy of that up here?

MS. MICHEL: Yes, it should be the top chart.

JUDGE McGUIRE: We will label that as DX-15.

MS. MICHEL: Yes, thank you.

(DX Exhibit Number 15 was marked for

A. May I step down and --

JUDGE McGUIRE: Yeah, go ahead. All right, now, again, I am going to ask you to clarify that I have a question when you say please explain your opinion, what opinion are you asking him to express as to the claims that you have otherwise mentioned, I believe 160 and 164.

BY MS. MICHEL:

Q. At this time, I ask Mr. Nusbaum to only explain his opinion with regard to claims 160 and 164, and in particular, why those claims cover an SDRAM compliant with the JEDEC Release 4 standard.

JUDGE McGUIRE: Okay, Mr. Nusbaum, you may proceed.

THE WITNESS: What this claim chart shows is in left-hand column, the limitations of claim 160 from the patent office amendment that we were just looking at. And 164, that's in the left-hand column.

In the right-hand column, is labeled JEDEC Standard Release 4, which is short for an SDRAM that's compliant with JEDEC Standard Release 4.

One determines or demonstrates that a claim literally covers a product by demonstrating that every limitation in the claim finds a counterpart in some aspect of the product. Now, the product can have a

multitude of other features, but if the claim has this open-ended language comprising it, but there must be each feature that's claimed in the product in question.

Now, I've given this claim language its broadest reasonable interpretation as must be done for application claims in the Patent & Trademark Office. Starting with "in a memory storage system," the JEDEC Release 4 standard talks about, "Configurations for solid-state memories," focusing on SDRAMs, and it may be handy to have the block diagram in front of you as well to reference in this analysis, but it's clear that we're dealing with a plurality of DRAMs, or systems with the plurality of DRAMs.

And so clearly there's a memory storage system. That system includes a bus. If one looks at the JEDEC standard, there is various indications of address, data and control lines in the various DRAM block diagrams. One can look at DX-4, the block diagram, and see a number of different buses all to claim what requires of a bus, we have that.

The next limitation is a semiconductor device. The semiconductor device corresponds as indicated in the chart, to any one of the SDRAMs in a standard, they're semiconductor devices. Also, because each module contains a number of DRAMs which are semiconductor

devices, the modules are semiconductor, or may be viewed as semiconductor devices as well.

The device has to be configurable by a device that's external to the semiconductor device, and the standard provides for changing the modes of operation by virtue of changing a mode of operation, and further in this case by changing the mode of operation before normal operation, the device is being configured.

Then we get to the body of the claim. The body of the claim requires at least one pin for coupling the semiconductor device to the bus. One can look at any of the many DRAM block diagrams that are in the standard and the SDRAMs or DRAMs have pins which makes it possible for them to be connected to the address, data and control bus.

Now we come to at least one register. That at least one register, giving that claim language its broadest reasonable interpretation, that one means at least one or more. That's met by one. If you've got one register that satisfies these limitations, you've got this one-to-one mapping that's required. And for the counterpart to this, at least one register, I have identified the SDRAM mode register.

Now, the SD -- the limitation of at least one register, what it has to do by virtue of this claim is

to be received by the semiconductor device from the bus when the semiconductor device is configured. That information by virtue of the standard is indicated as being the latency mode burst type, burst length information is transmitted over the address bus, so it's received from the bus and it's received, and this is a quote from JX-56-114, the mode register page we looked at, that "Data is written after power-on, but before normal operation." So, it was during the configuration time period.

The semiconductor device stores the information received from the bus lines in the register during configuration. We know that's the case, that's the purpose of the information being written, so that it may be stored in the mode register.

And then, finally, the semiconductor device has to respond to transaction requests in the manner specified by the information stored in the register. Again, during the animation, and we saw that depending upon how the cast latency bits were set, there would be a number of clock cycles that one would wait before information was transmitted, but beyond that, in the -- in Release 4 itself there is an indication that depending upon the setting of bits in the register that the burst of four, or in sequential addresses a burst of

8, in an interleaved mode are examples of responses that follow.

Now, claim 164 is dependent upon claim 160, so it includes all these limitations, but what it adds, it gets more specific. And it says, now, the register doesn't merely specify a manner in which the semiconductor device is to respond, it gets more specific, and identifies what that manner is. It expressly says that the register is an access-time register and the information is a value indicative of the access time for the semiconductor device, where the access time -- where the semiconductor device being operative to wait for the access time before using the bus in response to a transaction request specifying the semiconductor device.

So, this now more particularly just zones in on the cast latency field where the field of -- the latency field of the SDRAM mode register defines values which are indicative of the programmable access time and, as we saw in the animation, causes the SDRAM to wait for the access time before using the bus in response to a read request.

BY MS. MICHEL:

Q. Okay, thank you. If you would like to take a seat, unless Your Honor has any questions.

JUDGE McGUIRE: No, I do not have any questions.

BY MS. MICHEL:

Q. If you would like to take your seat, Mr. Nusbaum, also, as you walk back there, if you could please take a pen and indicate the location of the '961 application on the patent tree in back of you.

A. I have no pen.

Q. I'm sorry, there are markers right in back of your seat.

A. (Witness complied.)

Q. That's fine, thank you. And Mr. Nusbaum, could you please tell us which application you've just circled.

Q. Mr. Nusbaum, referring to claim 160, that claim contains the phrase "a semiconductor device having that is," do you see that phrase?

A. Yes, I do.

Q. What approach did you take in interpreting that phrase?

A. In my view, the language "having" is a result of a typographical or word processing error where the drafter did not delete that terminology, that the -- in my opinion, this phrase should be read as if the claim were amended to connect that typographical/word processing type error, so that the language reads, "A semiconductor device that is configurable by a device that is external to the semiconductor device," and there is precedent to support interpreting the claim as if it were amended to correct such a typographical -- such an apparent typographical word processing type error.

"comprising," as I testified, is open-ended terminology, which means that if an accused product has all the features required by the claim, it could have a multitude of other features, and it matters not.

Q. You said there was precedent, could you explain what you meant by that?

A. There is a court of customs and patent appeals case in re: Herman, in which the court followed the board of appeals lead and treated certain language in a claim that was believed to be an obvious typographical error as if it were amended to correct that. There is also a District Court case out of Kentucky that I'm aware of, the name escapes me, but it is a case in which a claim included by what was believed to be an obvious typographical error the word "into," and the court chose to interpret that language as "to," instead of "into."

Q. In interpreting claim 160, how did you interpret the terminology "transaction request?"

A. I/TT2 1 Tfm.009tR9n(e terminology "1c(12)6(logy 0 Tcrq In i 0 9.96

it's consistent with the interpretation -- the interpretation that I've used -- is consistent with the interpretation that the court of appeals used in its Rambus appeal.

Q. If we could look at the interpretation from the

A. Again, I interpreted "transaction request specifying the semiconductor device" giving that language its broadest reasonable interpretation. At the end of the day, we know that a semiconductor device is specified somehow, because it would be impossible to read from or write to a DRAM unless it was specified. I have interpreted transaction request specifying the semiconductor device as being broad enough to cover the JEDEC-compliant SDRAM Release 4 whether a transaction request is interpreted so as to include within the request itself a chip select signal that in the JEDEC memory system identifies a semiconductor device such as a module with the DRAMs in there, or alternatively, even if one were not to interpret transaction request as including the chip select line, but alternatively interpreted the chip select line as being something

semiconductor device by virtue of the time of appearance of the transaction request, which coincides with the chip select line being in a state enabling a particular module.

Q. I would like to refer again to claim 160, it might be easiest to look at the claim chart. Does that claim require a device identifier?

A. No, it does not. There is nothing in claim 160 whatsoever that either calls -- that calls for any kind of device identifier. There is a limitation that at least one register is operative to store information specifying a matter in which the semiconductor device is to respond.

Q. Are you aware that the Federal Circuit has stated that claims in the '961 application were limited to device identifier features?

A. Yes.

Q. Do you believe that the court would have based 0160 least one registe

Q. Does claim 164 require a device identifier feature?

A. No, it does not.

Q. Do any of the claims added in the January 1995 amendment recite device identifier features?

A. Yes, they do, there are claims that recite device identifier features. In, for example, claim 161. This is a claim that's dependent upon claim 160, which requires that the register is an identification register, and the information is an identification number that uniquely identifies the semiconductor device. So, that's an example of a claim that claims an identification feature.

Q. Does the fact that the claim 161 contained this feature suggest anything about the interpretation of claim 160?

A. Yes. It suggests that claim 160 should not be interpreted to include a limitation that is included independently. It should not be interpreted to cover or be directed to what is set forth in claim 161.

Q. Mr. Nusbaum, I believe you also stated that claims -- that claim 151 would cover an SDRAM used in compliance with JEDEC SDRAM -- JEDEC Release Standard 4. Is that right?

A. That's correct.

Q. And could you please explain your basis for that opinion that claim 151 would cover SDRAM compliant with Release 4? I believe we have a demonstrative to use with this explanation, which we don't have the blow-up, but I think we're going to get it on the screen. The demonstrative claim for claim chart 161.

JUDGE McGUIRE: Do you have that as well for hard copy purposes?

MS. MICHEL: Yes, I believe that should be on the second page of the hand-out I handed out.

JUDGE McGUIRE: Has that already been marked, the one you're talking about?

this whole thing as DX-15 instead of every page. I mean, that's going to get out of bounds by the time we conclude this trial.

MS. MICHEL: Yes, Your Honor, that would be fine. We also have blow-ups of some of the charts, and as long as that doesn't cause --

JUDGE McGUIRE: Well, that's fine. It seems to me it's part of this overall package. Do you have any comment on this, Mr. Stone?

MR. STONE: No, Your Honor, I have four pages, five pages, I'm sorry, of claim charts, and if we mark the five pages of claim charts as DX-15, I think that's fine.

JUDGE McGUIRE: Right.

MR. STONE: And then the block diagrams, the first one was marked as DX-4, but I believe there's going to be three more block diagrams.

JUDGE McGUIRE: Three pages of DX-4.

MR. STONE: This we could possibly mark as DX-16.

JUDGE McGUIRE: It's already been marked as DX-15, and now you are referring to page 2 of DX-15, correct, for claim 151?

MS. MICHEL: That's right, Your Honor, I believe it may be page 3 on my copy.

JUDGE McGUIRE: Page 3, okay. All right, page 3.

MS. MICHEL: Your Honor, may I approach the witness and hand him more water?

JUDGE McGUIRE: Yes, please.

THE WITNESS: Thank you.

JUDGE McGUIRE: I hope that's only water you're giving him.

BY MS. MICHEL:

Q. All right, Mr. Nusbaum, if you could please explain for us with reference to the claim chart previously marked DX-15, your opinion that claim 151 of the '961 application would cover an SDRAM compliant with the JEDEC Release 4.

A. Yes. Once again, what we have in this claim chart is in the left-hand column, claim 151 of application 847,961, and it's important to get the right application, because there are a lot of claim 151s in these various applications.

In the right-hand column of this chart is JEDEC Standard Release 4, which relates to SDRAMs that are compliant with JEDEC's Standard Release 4. And in order to demonstrate that this claim covers the JEDEC-compliant SDRAM or SDRAM system, it's necessary to show that each and every limitation in the claim on the

left-hand side finds a counterpart in such a system on the right-hand part of the chart.

And for this purpose, it is helpful to have a visual aid of the block diagram DX-4 in front of you, because it does show a system that it's important to focus on.

With regard to the computer system that is recited in claim 151, this system is formed by the combination of JEDEC-compliant DRAM modules such as module 1 and module 2 that's shown in the block diagram, together with the memory controller that's shown in the block diagram, or alternatively, you could take the system in the block diagram and put it into its typical PC context, where the memory controller would be coupled to the central processing unit of a personal computer. Either way, you have a computer system.

What follows from that is a limitation that the bus includes bus lines for carrying data. It's clear that this feature is met, we have address data control lines, certainly there is data lines that carry data in the JEDEC counterpart.

We have then a bus master that's coupled to the bus. Well, if one looks at the block diagram, as was explained in or by Mr. Rhoden, we've got a memory controller that is the sole interface between let's say

a central processor and a PC, and these DRAM modules. The memory controller is that which controls the bus between the memory controller and the DRAMs, and it is a bus master, it seizes control of this bus.

Then what's required are plurality of semiconductor devices that are coupled to the bus, and in this instance, any one of -- any of the SDRAMs in the [illegible] device. Such DRAMs are typically used in a module, and each of these modules, as I testified before, may also be viewed as a semiconductor device. So, we clearly have a plurality of semiconductor devices.

Then we have each semiconductor devices comprising, and then what follows are limitations with

t's 90 412.8 Tm.001 Tc(Theatil.dmT8o rf9t,ycscally u.96 Tm9.96 0 0

are defined by the SDRAM mode register, the time at which information is transmitted over the bus changes. So, as we saw in the animation, depending upon how the cast latency field is set, the timing of information being transmitted over the bus changes.

And so the communication protocol for the bus is changed or configured. And other than that characterization, the limitations are very similar, and for the reasons that I explained with respect to claim 60, these limitations are satisfied as well.

There's a counterpart to each and every limitation in this claim, in the system that I've described.

Q. I believe you also mentioned claim 159. Is that right?

A. Yes.

Q. And if we could look at claim 159, which is at CX-1504 at page 221.

MR. STONE: Your Honor, I believe claims 159 and 168 that were mentioned by the witness as claims that he has opinions on today were not discussed in either his report or his rebuttal report. I think we can probably deal with them here today, but it's possible if he raises things that we couldn't have anticipated, we may find a need for either a further deposition of the

talked about in claim 164, except now we're talking about in the context of the computer system of 151. So, this is a dependent claim on 151, and what's added is the register is an access time register operative to store value indicative of an access time for the semiconductor device. The semiconductor device being operative to wait for the access time before using the bus. This is precisely what I already went over with respect to claim 164, and it clearly finds a counterpart in the JEDEC system relying on the latency mode field of the mode register, as I have in the past.

Q. Do claims 151 and 159 cover SDRAMs themselves?

A. Claims 151 and 159 are -- actually they cover a range of devices, including SDRAMs in a computer system context.

Q. I believe you also mentioned claim 165, if we could see that, please. Could you please briefly explain what this claim covers and how it relates to JEDEC-compliant SDRAM.

A. Claim 161 defines a method for configuring operation of a semiconductor device in a computer system, and what it is is it defines the inherent method of operating the system that I described in great detail with respect to claim 151, that is the computer system.

required, outputting the value through the bus by a bus master that is coupled with a bus, where the value specifies the manner in which the semiconductor device is to respond to transaction requests, after the semiconductor device is configured.

I have explained how there's a -- in accordance with the JEDEC standard, there is a value that's placed on the address bus that -- which is ultimately stored in the mode register, and there are multiple manners in which the semiconductor device, that is in this case the SDRAM, is to respond. Those values, as per the second step, are written to the SDRAM mode register, thereby conforming with the step of writing the value to a register in a semiconductor device.

Q. And if we could please look at claim 168. Mr. Nusbaum, could you please explain your opinion regarding the relationship of claim 168 with JEDEC-compliant SDRAM.

A. Yes, claim 168 is dependent upon the method of claim 165, and it is, again, analogous, although not identical, to the claim 164 that we looked at, but this time in method format. Claim 168 requires that the value specifies an access time for the semiconductor device, the method comprising the further step of the semiconductor device waiting for the access time before

waiting to respond to the access bus that requires the semiconductor device.

So, this step will inherently flow from the result of loading the cast latency field, and we saw on the animation the waiting of the access time before using the bus.

Q. Okay, Mr. Nusbaum, have you identified any other Rambus patent applications pending prior to June 1996 that in your opinion contain claims covering the programmable cast latency feature of JEDEC-compliant SDRAMs?

A. Yes. Application serial number 469,490.

Q. When was the '490 application filed?

A. The '490 application was filed on June 6th, 1995.

Q. What's the relationship between the '490 application and the '961 application that we just talked about?

A. The '490 application is a continuation application of the '961 application.

Q. Did Rambus file claims in the '490 application which are similar to claims in the '961 application?

A. Yes, Rambus did.

Q. And which claims were those?

A. Those claims are claims 183 to 185.

Q. And did Rambus file those claims in the June 23rd, 1995 amendment?

A. Yes, Rambus did.

Q. Is the amendment -- is the document on the screen the amendment to which you just referred?

A. Yes, it is. I referred to the date of the amendment by virtue of the certificate of mailing date that's June 23rd, 1995.

Q. In your opinion, do claims 183 to 185 that you mentioned also cover the use of a SDRAM compliant with JEDEC Release 4?

A. Yes, I believe they do.

Q. Could you please explain the basis for your opinion with regard to how claim 184 of those three covers a JEDEC-compliant SDRAM.

A. Yes, I would be glad to do that. I've prepared a blow-up exhibit, which will aid in that demonstration.

Q. All right, we will be using a claim chart in the demonstrative previously marked DX-15. I believe it's at page 4 in my package.

Mr. Nusbaum, Your Honor, may Mr. Nusbaum step down and approach the board?

JUDGE McGUIRE: Yes, go ahead, Mr. Nusbaum.

BY MS. MICHEL:

Q. Thank you.

A. Once again, in order to demonstrate that a claim covers a JEDEC-compliant SDRAM or any other product that's necessary to -- after giving claim in this case its broadest reasonable interpretation, find that there is a counterpart in the product you're comparing for each and every limitation in the claim. In order to demonstrate that the claim literally covers the product.

With respect to a semiconductor device having an access time that's programmable, the SDRAMs in the Release 4 are semiconductor devices, and the programmable cast latency field provides that they have an access time that's programmable.

Then what is required is at least one pin for coupling the semiconductor device to a bus, that must be present, it can be seen from many of the DRAM block diagrams in Release 4, I've identified one in this chart, and there are various DRAM pins that are coupled to address, data and control bus lines.

Then what we have is in the final claim paragraph, at least one access time register was operative to store a value indicative of the access time for the semiconductor device. And this language, in this paragraph, is very reminiscent of what we looked at before, and this access time register finds correspondence in the SDRAM mode register, particularly

noting the information that's stored there defining latency.

The value has to be received by the memory device from the bus. This chart reads form the bus, but I believe that to be a typographical error that probably occurred on my end. The semiconductor device storing the value and in the access time register, the semiconductor device thereafter being operative to wait for the access time before using the bus in response to a request, specifying the semiconductor device. And once again, the values are stored in this cast latency field indicative of programmable access time that causes the SDRAM to wait for the access time before using the bus in response to a request, as we saw in the animation during Mr. Rhoden's testimony.

Q. Thank you. You can have a seat.

Will you please circle the '490 application on the Rambus patent tree.

A. (Witness complied.)

Q. If we could please show on the screen claim 183 from CX-1504. I believe it's approximately page 264 of the exhibit. Mr. Nusbaum, will you please just briefly explain your understanding -- your opinion regarding the relationship between claim 183 here and a JEDEC-compliant SDRAM.

A. Yes. Claim 183, as opposed to being directed to a semiconductor device, puts that semiconductor device into a system context, and what's claimed is a computer system that comprises a bus, a semiconductor device that includes an access time register, that stores a value indicative of an access time for the semiconductor device, and then a bus master that stores the value, again, of the access time ratio.

Q. And if we could turn next to claim 185. If you could please briefly explain your opinion regarding the relationship of claim 185 to JEDEC-compliant SDRAM.

A. Claim 185 defines a method for programming an access time of a semiconductor device, and claim 185 would define the inherent method of operating such a JEDEC-compliant device. For very much the same reasons that I've testified about previously, there's in the JEDEC-compliant operation, there's a value that is put on a bus, as I indicated, the address bus, by a bus master, which is the memory controller, and the value

semiconductor device, which in this case is the JEDEC-compliant Release 4 SDRAM, responds to requests that specify the semiconductor device by waiting the particular number of clock cycles before using the bus.

Q. And how did you interpret the phrase "a request specifying the semiconductor device" that appears in claim 184?.96 0 0 9.96 67.02 586.6801 Tm0 Tcieaw vice" that appears in

semiconductor device coupled to the bus. A new claim 184 claims a semiconductor device having the programmable access time and new claim 185 claims a method whereby a bus master programs the access time of a semiconductor device coupled to the bus."

Q. All right, and is the portion on the screen in front of you now the portion that you just read?

A. That's correct.

Q. What was the examiner's response to the June '95 amendment that contained claims 183 to 185?

A. The examiner issued on November 27th, 1995, a restriction requirement, and what the examiner did in the restriction requirement is that he identified claims 169 to 175 as being drawn to a system and method of configuring devices by identification, and identified a group 3 which were claims 183 to 185 that were drawn to a system and method of configuring devices by access time.

Q. Is the page of CX-1504 on the screen the first page of the office action issued by the examiner that you just referred to?

A. Yes, it is.

MS. MICHEL: Your Honor, we request that CX-1504, which is the prosecution history that we've just been discussing, be entered into evidence.

JUDGE McGUIRE: Any objection?

MR. STONE: No objection.

JUDGE McGUIRE: So entered.

(CX Exhibit Number 1504 was admitted into evidence.)

MS. MICHEL: Your Honor, we are about to admit to a new topic, we have approximately 45 minutes left at this point.

JUDGE McGUIRE: Would you like to take a break now or just go ahead and conclude with this witness on direct? I have no preference.

MS. MICHEL: Mr. Nusbaum would like to take a break, Your Honor.

JUDGE McGUIRE: Okay, well then he controls. Then let's say 12:30, why don't we break until 1:45, and then we'll be back in at that time and you can continue inquiring. Hearing adjourned.

(Whereupon, at 12:30 p.m., a lunch recess was taken.)

AFTERNOON SESSION

(1:50 p.m.)

JUDGE McGUIRE: This hearing is now in order. At this time complaint counsel may proceed with its questioning of the witness, and there he is, okay. All right, Mr. Nusbaum, you're still under oath, so would you have a seat, please.

BY MS. MICHEL:

Q. Your Honor, I would like to clean up one point from this morning. In particular, I would like to ask the witness to refer to Exhibit 183 of the '490 application, which is currently on the screen.

Mr. Nusbaum, could you please explain why it is your opinion that this claim covers a JEDEC-compliant SDRAM?

JUDGE McGUIRE: All right, now before you go into that, I'm not sure what you mean when you say a 183, is that in CX-183 or it's claim 183, right?

MS. MICHEL: Your Honor, what is shown on the screen is claim 183 of the '490 patent application, which is CX -- which can be found in CX-1504.

JUDGE McGUIRE: Okay.

BY MS. MICHEL:

Q. Mr. Nusbaum, if you could please explain your opinion regarding the relationship of this claim to a

JEDEC-compliant SDRAM.

A. Claim number 183, for reasons that I went into in great detail this morning, covers a JEDEC Release 4 compliant SDRAM for a system for which it was designed to operate as -- and I'll just explain very briefly, as per the block diagram that I was using, DX-4, the computer system would indeed include a bus. The semiconductor device is the -- would correspond to the SDRAM. The semiconductor device comprising an access time register, for the reasons I went into in great detail this morning, there's a mode register which includes a latency field that corresponds to the access time register operative to store a value, and the bus master would correspond to the memory controller. The other limitations that are in the claim closely parallel limitations that I have testified about previously. There is a one-to-one correspondence between elements in this claim and a computer system using a JEDEC-compliant SDRAM.

Q. And one other clean-up point, Your Honor, I would like to enter into evidence Exhibit CX-1877, that is the Markman brief by Rambus in the Rambus versus Infineon litigation to which Mr. Nusbaum relied on the definition of transaction request in that exhibit.

JUDGE McGUIRE: Objection?

MR. STONE: Your Honor, yes, I don't believe briefs properly should be admitted into evidence in that fashion. The court should take judicial notice of filings that are made in other proceedings, but I don't think there's any basis for introducing briefs into evidence as such.

JUDGE McGUIRE: I agree, sustained. I'll take any notice of it, but I'm not going to enter it into evidence.

BY MS. MICHEL:

Q. Mr. Nusbaum, have you identified any Rambus patent application pending before June 1996 which contains claims that in your opinion cover a phase locked loop related JEDEC proposal for SDRAM?

A. Yes, I have.

Q. Which patent application was that?

A. It's patent application serial number 847,692.

Q. What's the relationship between the '692 application and the original '898 application?

A. The '692 application is a divisional application of the original '898 application.

Q. When was the '692 application filed?

A. I believe it was filed March 5th, 1992, although I can't read on my copy of the first page of the prosecution history.

signals, and this is the loop clock system that I've testified that it is not utilized in a JEDEC-compliant system.

Q. Did Rambus at some point cancel the original claims and replace them?

A. Yes.

Q. And do you recall approximately when that was?

A. That occurred on June 28th, 1993.

Q. And did that occur in a preliminary amendment which I believe is at page 208 of the Exhibit 1502?

A. Yes, it did. On page 4 of the preliminary amendment, to be specific.

Q. In your opinion, do any of these claims in this preliminary amendment cover a PLL proposal for SDRAMs?

A. Yes.

Q. And which claim, in your opinion, meets that criteria?

A. Claims 151 and 152, 166 and 167.

Q. Is the claim 151 to which you just referred the claim now shown on the screen?

A. That is correct. Actually, I better back up a . Yes.

has been deleted.

Q. And is the version of claim 151 now on the screen the amended version to which you just referred?

A. Yes.

Q. How does it differ from the earlier version of claim 151?

A. Well, it differs in a number of respects. The terminology at the very end of the claim, wherein the memory array, the clock signal receiving circuit, and the PLL, all reside on a single semiconductor chip has been added, and there have been other changes that have been made as well, such as the language performing has been -- performing memory operations has been changed to controlling memory operations.

Q. Mr. Nusbaum, I would now like to ask you to refer to exhibit previously marked JX-21, it is a set of JEDEC minutes. Do you recognize that exhibit, JX-21?

A. I can't say that I can read what's on the screen, but --

Q. There you go.

A. Yes, these are JEDEC minutes of meeting number 72, the meeting took place on September 13th, 1994, and this exhibit includes an attachment that's designated attachment AA that includes a phase locked loop related presentation by NEC.

Q. Did you review that proposal relating to phase locked loop?

A. Yes, I did.

Q. In particular, with regards to the page of the proposal now shown on the screen, what's your understanding of what's shown here?

A. The proposal that's shown here, just to put it in context, two pages earlier in the proposal, at least I believe it's two pages earlier, there is a -- there is a mode register shown for an SDRAM, so that we know that the proposal relates to SDRAM. This particular mode register has got a bit in position 11 that is a PLL enabler. And going back to the page that you directed my attention to, this page shows the details of the operation of the PLL enabled mode. There is an indication that this PLL is on-chip, because it says, "on-chip-PLL." There is a block diagram that shows SDRAM operation without PLL and then with PLL. And with respect to the operation with PLL, what's shown is an external clock signal that's coming in on the left-hand side, and there is an internal clock that's generated that's labeled ICLK. That's output from the PLL, as shown, and the PLL, phase locked loop, operates, as you can see, in the timing diagram, to synchronize in time the external clock signal that's shown with the internal

clock, and it does that by variably delaying the internal clock, and you can see the delay in the internal clock by comparing the two timing diagrams.

Q. All right, and now I would like to ask you to turn to a demonstrative, which we've previously marked DX-16, and it has the -- it is the first page of DX-16, and it has the title Phase Locked Loop Proposal for JEDEC-Style SDRAM Memory System. Mr. Nusbaum, could you please explain your understanding of this exhibit?

A. Yes. I generated this block diagram exhibit and had its accuracy confirmed by Dr. Jacob, the FTC's technical expert. The bottom of the block diagram is essentially the same as the block diagram in DX-4, I believe it was, that we talked about with respect to cast latency and the mode register.

And as I explained previously, this -- the bottom of the block diagram which shows the memory controller and the DRAM modules was taken from Dr. Jacob's expert report for showing a typical JEDEC-style SDRAM memory system. The blow-up of the DRAM that's shown on the top portion of the diagram, if one looks at both the mode register page that we talked about earlier, there is an indication of that mode register from the NEC proposal at the very top of the block diagram, and then the PLL proposal that's shown on the

at every word in the claim and this is to see whether it literally covers and see if there is a counterpart in the product that you're comparing it with.

With respect to a memory device, the first three words of the claim, there's no question about it, but the proposal relates to a memory device, the page we looked at with respect to the mode register identifies it as an SDRAM mode register, and SDRAM contains a memory bus.

Then moving to the next limitation, a memory array that stores data at addresses, if one looks at the NEC proposal, there is a block that's labeled memory array. And it does store data at addresses.

A clock signal receiving circuit is the next limitation, that's got to be coupled to receive an external clock signal. The clock signal receiving circuit generating a local clock signal for controlling memory operations with respect to the memory array. The PLL proposal from NEC has a triangular block that's shown, and it's labeled receiver in the NEC proposal. It is coupled to receive an external clock signal, CLK, and it generates or passes on the internal clock signal, ICLK, as its output.

The next limitation that's required is a phase locked loop, and that phase locked loop is shown in the

NEC proposal. According to the claim, that a phase locked loop has got to be coupled to the clock receiving circuit, which we can see in the NEC proposal, if one looks at the proposal, the PLL there is coupled to the component labeled receiver, and in terms of being coupled, giving this terminology its broadest reasonable interpretation, in terms of being coupled could be either actually physically coupled or operatively coupled.

With respect to the phase locked loop in the NEC proposal, the PLL is coupled to this -- to the output buffer of the memory array that's represented by a little triangle in the PLL proposal. This controls the reading of data from the memory array to the data bus that's indicated by the DQ. The PLL is required to provide a variable delay to the local plot system such that the delay clock signal is synchronized with the external clock signal, the signal received by the clock signal receiving circuit.

The PLL will provide a variable delay, that can be -- the delay can be seen, as I mentioned, by comparing the timing diagram with PLL and without PLL, and the external clock signal is synchronized with the internal clock, you can see the two timing diagrams lining up precisely in phase.

Lastly, the memory, the memory array, the clock signal receiving circuit and the PLL all reside on a single semiconductor substrate. The PLL in the proposal is identified as on-chip. The receiver and the memory array are on-chip as well, they all reside on a single substrate.

With respect to the claim 152, this is a dependent claim, it incorporates all of the limitations of claim 151, what it adds is that the memory array is a DRAM, we know that in the JEDEC proposal, that what we're dealing with is an SDRAM, which is a type of DRAM.

Q. Okay, thank you. Mr. Nusbaum, could I ask you to circle, please, the '692 application on the Rambus patent tree.

A. (Witness complied.)

Q. I would like to look for a moment at JX-21, that is the NEC proposal, and particularly exhibit page 91. Mr. Nusbaum, you mentioned that claim 151 has a limitation, the delay local clock system is synchronized with the external clock signal. Could you point out on Exhibit JX-21, page 91, where you believe that limitation is indicated.

A. The external clock signal, CLK, there's a timing diagram that's shown in the very bottom of the with PLL. The internal clock signal that's shown at the output of

the PLL is designated by ICLK, and you can see how these -- the clock signal and the external clock and the internal clock are lined up together, they're synchronized.

Q. Now, Mr. Nusbaum, when you analyzed claim 151 from October of '95, in your opinion, was there an earlier version of claim 151 that was introduced in the language that was also covered under the NEC claims?

A. Yes, it does.

Q. Can you explain briefly why?

A. Yes, the earlier version of claim 151 did not include the limitations wherein the receiver circuit and the PLL and the memory array were together under a single semiconductor substrate. I can't see the exact language, but that -- so, claim 151 was just a broader version, had less limitations than the October '95 version of the same claim. There were some other relatively minor changes that were made, but there's correspondence with those as well.

Q. Turning back to CX-1502, which is the prosecution hear, have you reviewed claims 166 and 167 which were also submitted in the October 1995 amendment?

A. Yes, I have.

Q. Do you have any opinion as to whether these claims cover a computer system using an

SDRAM-incorporated PLL proposal that we just looked at?

A. Yes, these claims do.

Q. Could you please explain the basis for that opinion?

A. Yes, if you take the entirety of claim 151, and I can't see too well from here, but I've seen it many times before, and you look at paragraph (C) of claim 166. Claim 151, as I previously explained the correspondence, is embodied in the memory device of paragraph (C) with respect to the limitations that are set forth, including the memory array, the clock signal receiving circuit and the phased lock loop. So, for all the reasons that I just went through in detail, those features are present that are in claim 166.

The two features that are added, or the features that are added, this claim is in a computer system context, if one looks at the demonstrative I was just utilizing with the PLL, for the reasons that I stated before, the combination of a memory controller and the DRAM modules can be viewed as being a computer system as well as a memory controller and the modules when used in its typical PC context, is a computer system.

Then the only other two limitations are a bus, which we clearly have, and the bus master would correspond to the memory controller. So, there's a

counterpart for each and every element in claim 166 as well.

Q. And do you have an opinion with regard to claim 167 and its relationship to an SDRAM incorporated in the PLL proposal?

A. Yes, I do.

Q. And what is that opinion?

A. Claim 167 just merely adds that the memory array is a DRAM, and it clearly is, I've demonstrated that.

MS. MICHEL: Your Honor, at this time we request that CX-1502, which is the prosecution history that we have just been discussing, be entered into evidence.

MR. STONE: No objection.

JUDGE McGUIRE: So entered.

(CX Exhibit Number 1502 was admitted into evidence.)

BY MS. MICHEL:

Q. Turning now to another topic, Mr. Nusbaum, have you identified any Rambus patent application that in your opinion contains claims covering a dual edge clock proposal for JEDEC SDRAMs?

A. Yes, I have.

clock proposal for SDRAM?

A. What I mean is by dual edge clock proposal, it is a proposal for controlling memory operations in an SDRAM -- read and write operations in response to both the rising edge and falling edge of the clock server.

Q. I would like to ask you to refer to CX-1493, which is the prosecution history of the '327 patent. Mr. Nusbaum, have you reviewed this exhibit?

A. Yes, I have.

Q. And what is it?

A. This is the prosecution history of the '327 patent, and actually U.S. patent 5,513,327, which contains the prosecution history of the application that I just identified 222,646.

Q. When was the '646 application filed?

A. The '646 application was filed on March 31st, 1994.

Q. What's the relationship between the '646 application and the original '898 application?

A. The '646 application is a continuation of an application 954,945, which in turn is a continuation of the very first originally filed patent application 510,898.

Q. Did any of the original claims in the '646 application cover a dual edge clock related JEDEC

proposal for SDRAMs?

A. No, they did not.

Q. Will you please explain your opinion on that.

A. The original claims in application 222,646 were the same 150 original claims that we have seen before, you know, there was just no claim in there that covered a dual edge clock proposal.

Q. In your opinion, when was the claim first filed in the patent office in the '646 application which covered an SDRAM having a dual edge clocking feature?

signal.

Q. Mr. Nusbaum, are you aware of any JEDEC proposals relating to dual edge clocking for SDRAMs made prior to June 1996?

A. Yes, I'm aware of a March 1996 JEDEC proposal. I'm aware of surveys prior to June of '96, and I'm aware of a May 1992 dual edge clock proposal.

Q. Let's look at JX-31, please, which should be JEDEC minutes from March of '96. Mr. Nusbaum, have you reviewed any portion of this exhibit?

A. Yes.

Q. And which portions have you reviewed?

A. I have reviewed the portion of this exhibit that is identified by attachment U and is a proposal for future SDRAM by Samsung.

JUDGE McGUIRE: Let's go off the record for a moment.

(Whereupon, there was a brief pause in the proceedings.)

BY MS. MICHEL:

Q. Mr. Nusbaum, what's your understanding of the proposal shown on the screen?

A. The proposal shown on the screen, as it indicates, is for a future SDRAM proposal, more specifically to a proposed clocking scheme, and there's

an indication in the proposed clocking scheme on -- I'm not sure if we can accurately call this a bullet point, but the fourth point is, "Data in sampled at both edge of clock into memory." So, that's a dual edge clock proposal.

Q. Okay, next I would like to direct your attention to a demonstrative previously marked DX-16, and it's the second page of DX-16.

JUDGE McGUIRE: I'm sorry, is it DX-15 or 16?

MS. MICHEL: Sixteen, Your Honor.

JUDGE McGUIRE: Okay, right, got you. No, wait a minute, I'm still confused, I had DX-4, and then the previous was DX -- I'm not sure what you're talking about when you say DX-16.

MS. MICHEL: Yes.

JUDGE McGUIRE: I don't recall that being marked.

MS. MICHEL: All right, what happened, Your

JUDGE McGUIRE: I don't think we did that.

MR. STONE: We talked about doing it, Your Honor.

JUDGE McGUIRE: Okay, then so marked at this time, DX-16, I just want to keep it straight for the record.

(DX Exhibit Number 16 was marked for identification.)

JUDGE McGUIRE: All right, go ahead.

BY MS. MICHEL:

Q. Mr. Nusbaum, I would like to direct your attention to the second block diagram of DX-16, which bears the title Dual Edge Clock Proposal for JEDEC-Style SDRAM Memory System. Do you have that?

A. Yes, I do.

Q. What's your understanding of what's shown in this block diagram?

A. This is a block diagram that I prepared in concert with Dr. Jacob. The bottom portion of the block diagram I extracted from Dr. Jacob's expert report that shows a typical JEDEC-style SDRAM memory system. With respect to the exploded view of a DRAM, this exploded view was generated by Dr. Jacob and what it shows are the structural components that are inherent in data that's in sample -- of data in that's sampled at both

edges of the clock into memory, where the data is coming in at the right through this data pin, as represented by the data pin DQ, the memory of the data is being stored in the memory array that we've seen before. The clock signal is coming in through this pin CLK, and there's a quote, "Data in sampled at both edges of clock into memory" from the Samsung proposal, and what's shown as a

standard of Samsung. In order to demonstrate that this claim literally covers this proposal, it's necessary to show at each level what's set forth in the claim and a counterpart in the proposal. The claim calls for a dynamic random access memory or DRAM that's capable of being coupled to a bus. The proposal is for an SDRAM, which is a type of DRAM, we know it's coupled through a bus.

A first circuit for providing a clock signal, and an SDRAM inherently will receive an external clock signal and it will do that through a circuit that will provide an internal clock, so the internal clock representation of the external clock that corresponds to the first circuit that provides a clock signal, and is indicated by a receiver triangular block of the nature that we saw in the NEC proposal, even without PLL.

The next limitation is that there's a conductor for coupling the DRAM to the bus. An SDRAM will have pins that couple to the bus. The Samsung and other dual edge clock proposals will inherently require connection of the SDRAM to various different buses.

Then the final limitation is that the receiver circuit is coupled to the conductor and the first circuit, and the receiver op circuit operates the latching information received from the conductor in

JUDGE McGUIRE: Would you like to take a short break, Mr. Stone?

MR. STONE: No, I'm fine.

JUDGE McGUIRE: Then proceed with cross examination.

CROSS EXAMINATION

BY MR. STONE:

Q. Good afternoon, Mr. Nusbaum.

A. Good afternoon, sir.

Q. Could we bring up the stipulations? Paragraphs 9 and 10. I would like you to take a look, if you would, at the stipulations that are on the screen in front of you, Mr. Nusbaum. And take a look first at paragraph 9. It talks about prior to the adoption of the JEDEC SDRAM standard in 1993. You're familiar with rev 4, correct, of that standard? That's been your testimony today?

A. Release 4, yes.

Q. And when was Release 4 published?

A. It's my understanding that it was published in November of 1993.

Q. So, prior to November of 1993, do you agree that Rambus had no claims in any pending patent application that if issued would have necessarily been infringed by the manufacture or use of any device manufactured in

accordance with the 1993 JEDEC SDRAM standard?

A. I can't testify as to any pending patent application, I am not familiar with the entirety of Rambus's patent applications. I can say that of the patent applications that I've looked at, I'm not aware of any pending application that had claims that would have necessarily been infringed.

Q. Okay. And you looked only at patent applications that were shown to you by complaint counsel?

A. That's correct. I had no knowledge of those applications prior to this case.

Q. And so, someone else made the selection of what you should or should not look at? Is that fair?

A. Employees of the FTC did, indeed, forward me certain patent applications.

Q. Okay. And then if you would look at paragraph 10 of the stipulations. Do you agree that based at least on the extent of things you have looked at, that as of January of 1996, Rambus had no issued U.S. patents that were essential to the manufacture or use of any device manufactured in compliance with any JEDEC standard?

A. I am not aware of any issued patents that I have knowledge of that were essential to the manufacture or

use of any device. I've testified about these four patent applications, and that's the extent of my knowledge.

Q. Are there any patents that issued to Rambus prior to June of 1996 that would be essential to the manufacture or use of any device manufactured in compliance with any JEDEC standard as of that date?

A. My focus has been on these four patent applications. If you could present me with a patent that I could analyze, if given enough time, I would be happy to express my opinion appli02 66Tm0 g.001 Tc0TT4 1 Tf9.96 0 0 9.96 62.0

Q. And you've checked this chart?

A. I have.

Q. Okay. As to any of those six patents that had issued to Rambus prior to June of 1996, are any of those patents necessarily infringed by the manufacture of a JEDEC-compliant SDRAM part?

A. Are you talking about with respect to Release 4?

Q. Let me ask you first about Release 4, yes.

A. I'm not aware of any patent that falls within your question, but please keep in mind that I have looked at four patent applications, I have not studied the claims in any of these patents, but I'm not aware of any patent that falls within your question.

Q. And have you looked at other versions of any SDRAM standards other than Release 4?

A. I have not.

Q. Now, you've testified earlier today about a standard that you applied from time to time which was interpreting the claims as broadly as their terms reasonably allow. Is that a fair paraphrasing of your testimony?

A. The claim interpretations standard that I was referring to is the broadest reasonable interpretation standard, that's what I was referring to.

Q. And was that the standard that you understand

that is applied by patent examiners during the prosecution?

A. That is correct, as a matter of law.

Q. And is it -- am I not correct that the patent examiners are trained and told that they should "apply the following standard: During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning, unless applicant has provided a clear definition in the specification." And I'm quoting from the manual, which I know you're way more familiar with than I am. Is that a correct statement of the standard?

A. I believe it is, yes.

Q. Okay. And is it also correct that the meaning of claims of issued patents are to be interpreted in light of the specification prosecution history, prior art and other claims, and that is different than the mode of claim interpretation to be applied during prosecution?

A. There are -- they are two different claim interpretations standards.

Q. So, when I asked you earlier about whether something necessarily infringes, you would apply the claim interpretation that you would apply to an issued

patent in responding to that question, correct?

referring to?

Q. Those 11 inventions.

A. One file is patent applications, one includes claims -- a claimed invention in patent applications, I'm not quite sure if I appreciate your question.

Q. Sure. The original '898 application was subject to a restriction that required it to be ultimately divided into 11 separate applications, correct?

A. That is correct.

Q. And the reason for the restriction was that the examiner thought there were at least 11 separate inventions?

A. The examiner did indicate that in his view there were 11 independent distinct inventions.

Q. Now, and an attorney had filed that application, correct?

A. That is correct.

Q. And you talked earlier about a reasonably prudent patent attorney, do I have the language right that you used?

A. I'm not sure if those were my exact words.

JUDGE McGUIRE: Close enough, Mr. Stone.

BY MR. STONE:

Q. Okay. Would a reasonably prudent patent attorney aware of the existence of 11 separate

inventions decide to include them all on a single application, in your opinion?

A. It's not at all unusual for a prudent patent attorney to file a single comprehensive patent application that includes a lot of identifiably different kind of inventions.

Q. Knowing that there's going to be a restriction imposed?

A. Suspecting strongly. There are certainly those instances where clients prefer not to have to pay for a number of different -- many different divisional applications.

Q. And when you do that, when you file them all as part of a single application, then as they are subsequently subject to restriction, and divisions result, each of those divisions is going to be based on the same written description as the original application. Is that also correct?

A. That is correct.

Q. Okay. And when there's a continuation of a patent, that continuation application also is based on the specification and written description of the original application?

A. It is not allowed to contain any new matter.

Q. Okay. And so, the patent tree that you have

behind you, it has on it -- do you know how many issued patents?

A. I do not.

Q. In the neighborhood of 43, would that be an approximation?

A. It wouldn't surprise me.

Q. Okay. Each of the claims, in each of those issued patents, is based on the original written description and specification filed on April 18th of 1990 in the '898 application, correct?

A. When you say it is based, are you -- I presume that you're just saying did the -- were those claims filed in an application that had the same disclosure.

Q. No, that's okay, let me lay a little more foundation here. It's a requirement, is it not, of the patent laws that the written description must describe the invention in full, clear, concise and exact terms?

A. That is part of 35 USC 112.

Q. And 35 USC 112 then goes on to say, "It must describe the invention in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains to make and use the invention," correct?

A. It does say that, and that is the enablement requirement that I testified to.

Q. And a person skilled in the art is whom?

A. A person skilled in the art is a hypothetical

it's clear from reviewing the original specification that the inventors were in possession of that later claimed subject matter.

Q. So, the fundamental factual inquiry is for the examiner to determine that the specification conveys with reasonable clarity to those skilled in the art that as of the filing date sought, the applicant was in possession of the invention that is now described in a claim, correct?

A. That is part of what needs to be considered, it's certainly what a patent examiner would consider.

Q. And it's a necessary element, I mean, they have to have that, as well as other things?

A. Correct.

Q. So, in each of the claims, in each of the patents that has issued from the original '898 application, was determined by a patent examiner to claim an invention that was described with reasonable clarity to those skilled in the art in the written description that was filed in April of 1990, correct?

A. That's correct, but it should be borne in mind that over time the legal standard changed and a determination that may have been made by a patent examiner let's say in 1997 may not have been in accord with the legal standard that prevails today.

Q. And some of the things you've described to us today, some of the claims that you said were later amended or added, sometimes your description of those claims was that they broadened the claim coverage from what had been in the application earlier. Is that fair?

A. Yes, I did indeed state that.

Q. Now, can we just go back to the last one that you told us about, that was the '646 application, and I just want to make sure that we have some basic facts in the record as to this particular application. The claim that you said related to a DDR presentation, that's a dual edge clock presentation, that claim was first added to the application when? 3

Q. And this ultimately issued as what?
A. The '327 patent.
Q. And did the '327 patent have that claim in it?
A. It did not.
Q. Okay. Now, does the SDRAM standard that you've looked at, that's Revision 4? It's Release 4, I keep saying that, which one is it?
A. I believe it's Release 4.
Q. Okay, Release 4. Does Release 4 of the SDRAM standard have in it any features that would necessarily infringe claim 151 of the '646 application?
A. Not that I'm aware of.
Q. Okay. Can we fairly write that dual edge clocking is not in release 4 of SDRAM standard?
A. Yes.
Q. Okay. And so what you showed us a relationship between was not the SDRAM standard, you showed us the relationship with a particular presentation, correct, on your claim chart?
A. I showed a relationship with a particular Samsung presentation and indicated other presentations, some of which were dated -- one of which identified as being dated May of '92.
Q. Right. And let me just focus on your claim chart for the moment. In your claim chart, you were

using a Samsung proposal.

A. Yes, sir.

Q. Or presentation.

A. Yes, sir.

Q. Was there ever a second showing of that presentation?

A. I have no idea.

Q. Was it ever valid?

A. I do not know.

Q. That was the March 1996 meeting of JEDEC that you pulled that proposal from, was it not?

A. That is correct.

Q. And was anybody from Rambus in attendance at that meeting?

A. I have no knowledge of that.

Q. Why don't you look at the first page of the exhibit that you showed us.

A. Maybe use your set, I'm not quite sure where I put it.

JUDGE McGUIRE: Take your time.

BY MR. STONE:

Q. We can bring it up, it's JX-31.

A. I've got it.

Q. You've got it?

A. Yes, sir.

Q. And just take a look at the cover page, you'll see how the companies are listed in alphabetical order. And you'll note, won't you, that there's no entry for anybody from Rambus being in attendance on the first page.

A. I don't see Rambus identified on this page.

Q. And then if you go to the second page where it shows others present, you will note that there's also again no entry for Rambus, correct?

A. That's correct.

Q. Now, you have not as part of the work that you've performed, you have not done an analysis with

identification.)

BY MR. STONE:

A. I did at one time.

Q. And did you make a determination as to whether in your opinion there was a relationship between those allowed claims and the PLL presentation by NEC that I think you used in your claim chart?

A. I don't recall reviewing those claims with that in mind, seeing that there was an amendment after July of 1996, and my analysis stopped at the June '96 point in time where the FTC is alleging that Rambus was no longer a JEDEC committee member.

Q. Okay. So, you don't know, I guess, whether from this '692 application, claims ultimately issued which would still have had a particular relationship to the PLL presentation that you referred to earlier?

A. I do not know one way or the other.

Q. Now, this particular application, the '692 application, this was argued by Infineon in the Infineon case to have been something that Rambus should have disclosed to JEDEC, correct?

A. I can't say that sitting here today I'm entirely familiar with the arguments that Infineon made.

Q. Did the Federal Circuit consider an argument in its opinion as to whether the '692 application should have been disclosed by Rambus to JEDEC?

A. I don't recall whether the '692 application was

specifically identified by the Federal Circuit.

Q. Okay, but I guess we can go back and look at that opinion and see one way or the other?

A. We could.

Q. And the PLL presentation that you used in your claim chart was a presentation by NEC in September of 1994?

A. That's correct.

Q. And was PLL -- is PLL required by the 1993 Release 4 JEDEC SDRAM standard?

A. I do not believe that it is required.

Q. Okay. So, would it be correct to say Release 4 of SDRAM standard does not require use of PLL?

A. That's my understanding.

Q. Okay. So, with respect to the two that we've just done, and let me ask you a question, a background question about infringement. Standards themselves don't infringe patents, do they?

infringe, that's one scenario, correct? That's a background question.

A. The product --

Q. Let me back up. I'm trying to ask a background question, let me make it simpler.

A. It is possible to manufacture a product in compliance with a standard, and then add some other features that the standard doesn't prohibit. Correct?

MS. MICHEL: Objection, outside the scope of direct. Mr. Nusbaum --

JUDGE McGUIRE: How is that outside the scope of direct?

MS. MICHEL: Mr. Nusbaum has not talked about what's possible to or what kind of products could possibly be built and still comply with the standard.

MR. STONE: Let me go at it another way, Your Honor, I'm not trying to turn him into an expert in this field.

JUDGE McGUIRE: Sustained.

BY MR. STONE:

Q. Earlier when I asked you about a patent that might necessarily be infringed by the manufacturer of a product in compliance with a standard, did you understand that if the standard required you to include certain features and if those features that you were

required to include would infringe, then the product would necessarily infringe as a result of its compliance? Is that worse?

A. It doesn't glimmer with clarity to me. I think I know what you mean.

Q. Then let me just violate that number one rule of cross examination, okay? Just explain to me what it is that a -- what the criteria are for a product manufactured in compliance with a standard to necessarily infringe a patent because of compliance with that standard.

A. As I went through with my claim charts many times, if one looks at each and every element of a claim, and there is a counterpart in a product that is built in compliance with a standard with each and every

necessarily infringed by, I meant necessarily infringed the claims. Did you understand that? Let me try it again.

A. I wasn't quite sure what you were asking.

Q. Let me try it again, Mr. Nusbaum. Are there any claims that have issued from the '646 application that in your opinion are necessarily infringed by the manufacture of an SDRAM in compliance with any JEDEC promulgated standard?

A. I'm not familiar with any JEDEC promulgated standard other than Release 4. I can't answer that question.

Q. Okay. And as to Release 4, is your answer no?

A. I'm not aware that any claim in that application covers a Release 4 compliant product.

Q. Let me go start another chart that will be DX-19.

(DX Exhibit Number 19 was marked for identification.)

BY MR. STONE:

Q. And one of the other applications that you talked about was the '961 application, correct?

A. That is correct.

Q. And there were certain claims in the '961 application that you felt, had they issued, would have

been infringed by products manufactured in compliance with Release 4?

A. That's correct.

Q. And what are those claims?

A. If we focus on the January 6, 1995 amendment, it's claim 160, 164, claims 151, 159, 165 and 168.

Q. And those claims were all introduced into this application in did you say January of '95?

A. January 6, 1995.

Q. And we're comparing these claims to the November 1993 Release 4 SDRAM standard, correct?

A. That is correct.

Q. Now, is it your opinion that had these claims issued, a manufacturer of a product in compliance with Release 4 of the SDRAM standard would necessarily have had to take a license under the patent that included these claims in order to avoid infringement?

A. I believe that to be the case.

Q. And the Federal Circuit had before it the '961 application when it decided the appeal involving Infineon, did it not?

A. The Federal Circuit did, but I don't believe that the Federal Circuit was considering that -- these claims, they could not have.

Q. And the Federal Circuit said in its opinion,

Circuit opinion speaks for itself, he doesn't need --

JUDGE McGUIRE: It does speak for itself, so I don't think we need to get into it.

MS. MICHEL: To the extent that Mr. Stone does get into what the Federal Circuit opinion said, I think Mr. Nusbaum ought to be able to explain his disagreement with the decision.

JUDGE McGUIRE: Well, we'll see, but is there any point in continuing this line of inquiry, Mr. Stone?

MR. STONE: No, I will let it speak for itself, Your Honor.

JUDGE McGUIRE: Good, thank you.

BY MR. STONE:

Q. Let me move to the -- there's one other application, then, that you described for us today, am I right?

A. Yes.

Q. And which one is that?

A. Application serial number 469,490.

Q. I'll mark this as DX-20 for identification.

(DX Exhibit Number 20 was marked for identification.)

BY MR. STONE:

Q. And this will be the '490 application. And the claims of the '490 application that you talked about

earlier were which?

A. Claims 183 to 185.

Q. And you described these as substantially similar to the claims that you also discussed from the '961 application, did you not?

A. There was a great deal of commonality, yes.

Q. Did claims 183, 184 or 185 of the '490 application ever issue?

A. I don't believe they did.

Q. Okay. And to your knowledge, have those claims, 183, 184, 185 of the '490 application ever been asserted against any JEDEC-compliant SDRAM part?

A. I can't say that I've reviewed the claims in the patents that have been asserted to check to see whether claims which either were identical or substantially identical were asserted, but I'm not aware of any such claims that have been asserted.

Q. Okay. Could we bring up what we call NUS-004. This was earlier marked as part of DX-16, Mr. Nusbaum. Do you recognize it?

A. Yes, I do.

Q. If we look at the upper box, where we have CLK and a round circle.

A. Yes.

Q. That's the clock, correct?

A. That's an external clock, yes.

Q. Now, is there also a clock that relates to the information going from the memory controller into the DRAMs?

A. That was intended to be an indication of that -- of the clock signal that was coming from the memory controller.

Q. So, what you're describing on this portion of DX-16, the clock that you show in the upper box would be the same clock that would control the address command bus and data bus. Is that right?

A. It would be a clock signal that would be found on a line in it's not a single bus that's shown here, but it's just a conceptual representation of a number of buses, one of which would carry this clock signal.

Q. And my question, just to make sure, and I think you've answered it, is for each of these different bus signals, your understanding is that as depicted on this particular exhibit, DX-16, the same clock that we see at the top would be the clock that operated each of the bus lines?

A. Yes, sir.

Q. Okay. And let's go, then, to -- and it's also clear, is it not, that the data here that you show being sampled at both edges of the clock is just the data in

and not the data out?

A. It's only -- what is represented is the data coming in in this particular diagram, in accordance with the proposal.

Q. And then let's look at NUS-003, if we could. And you recognize this as being another one of the DX-16 charts?

A. Yes, this is a block diagram that I testified that I generated.

Q. And talking again about the upper box, we see a triangle that is labeled receiver.

A. That's correct.

Q. And what's that mean, receiver?

A. That was the label that NEC gave to a device that receives the external clock signal and that produces a signal which is the internal clock signal. It's my understanding that there's amplification of the signal that's occurring there.

Q. And then if we look down, we see another triangle in the same upper box that isn't labeled but that lies on the line between memory array and DQ. Do you see that?

A. Yes.

Q. Is that triangle also a receiver?

A. That's an output buffer.

Q. So, and an output buffer means that information is collected in that buffer from the memory array and then released?

A. Timed by the ICLK signal.

Q. And does the ICLK signal run into the buffer and then run back to the left into the memory array?

A. This is a proposal by NEC, and it just shows what it shows. It's indicated as just being an internal clock that drives that output buffer.

Q. As you understand this, is that internal clock, ICLK that runs into the output buffer, does it then go run into the memory array and cause anything inside the memory array to occur?

A. What it does, that internal clock is -- that that internal clock is necessary in order to -- for the critical memory operation of reading information out of the memory. It clocks the -- it drives the output buffer and the data from the memory array to the data bus. That's what NEC proposed, what else NEC had in mind by that proposal, I have no idea.

Q. You could only go on what you can read from the documents, right? And what Dr. Jacob has told you?

A. Exactly so.

Q. Based on your reading of the documents and what Dr. Jacob told you, because I'm not asking you to guess

about what was in anyone else's mind, does ICLK, ICLK, control when information goes from the memory array into the output buffer?

A. I'm not aware that it does, but it -- but for that ICLK, you would not have any data being read out of the memory array.

Q. But for that ICLK, you wouldn't have any memory being read out of the output buffer, correct, that's where it reads it out of.

A. Yeah, but the output buffer is the element that receives the data from the memory array.

Q. But ICLK does not control when or if the memory array sends data to the output buffer, does it? when or if the memory

proceed, Mr. Stone, cross examination.

BY MR. STONE:

Q. Thank you.

Mr. Nusbaum, you earlier described sort of the patent system and claims as a piece of property with fences. Do you recall that?

A. I do, yes.

Q. And if -- let me see if I can just carry through that metaphor properly right to the edge of its usefulness, but if we draw on what I'm going to mark as DX-21 a large parcel, and let's just say that's our parcel of land, or an inventor's invention, can you

to have a bunch of dependent claims, correct?

A. That certainly can be, yes.

Q. And some of which will overlap with each other, correct?

A. I'm not quite sure what you mean by overlap.

Q. Well, if we were to -- I was just trying to understand your analogy, if you will, to a piece of property and a fence is when you think of a patent in its totality, and the total number of claims in a patent, many of those claims, because some are independent and some are dependent, will overlap with each other, or fall inside of each other, won't they?

A. That's true. Each claim we need to consider individually.

Q. And it becomes a very complicated picture if we were to put -- try to put all the claims of one of these patents on a board and draw fences around each claim and see how they related to each other?

A. I wouldn't want to do it.

Q. Okay. If you want to understand the inventor's description of what they understood their invention to be, one place to look is the written description that we talked about earlier, right?

A. That's correct. And I did look to the written description on a number of occasions.

Q. And the written description for the original '898 patent application does talk about variable burst length, does it not?

A. I'm not sure that that's entirely true.

Q. And does it talk about programmable cast latency in the written description?

A. I don't believe that's entirely true for the -- a reason I have in mind.

Q. Does it talk about dual edge clock?

A. I am not sure whether it talks about dual edge

Q. But a reasonable and conservative patent attorney looking at those claims would have understood because he or she would have experienced it, that the claims might be broadened during the course of prosecution, correct?

A. To answer that question it's necessarily to view the specification in context, and the present or the invention, the present invention is described as including certain features that are repeated in a lot of the claims. With that being said, your question was couched in terms of would it be possible that the claims could be broadened and it's true, there's a possibility.

Q. So, a conservative and prudent lawyer if asked about that application would say, I can't tell you whether claims that ultimately issue from this would be broader than the claims we see in the original application or not, but they could be? Correct?

A. You want me to presume that the reasonable practitioner was asked a question as to whether it would be possible that the claims could be broadened?

Q. Okay, let's ask the reasonable and prudent practitioner that question.

A. In -- I've given you reasons why I think that there would have been a presumption of unnecessary limitations, but it's always possible that, like

anything else, that that kind of -- that that event could happen, they could be broadened.

Q. Now, the European equivalent, the PCT application that's the equivalent of the '898 application did become publicly available in 1992, didn't it?

A. I'm not sure of the exact --

Q. '91, I'm sorry. In October of '91.

A. I'm not sure of the exact period of time that it became public, but it's my understanding that it did.

Q. And as part of your thinking about me4IcE

Q. Did you ask -- in an effort to confirm your opinion that a reasonable attorney would not presume unnecessary limitations in the claims, did you ask to see -- is there any evidence that suggests that when

fewer lines than are required in a single address, and the -- with respect to the present invention, the bus does not have a chip select line, in so many words, in view of the prior art that was cited in the background of the invention, and the fact that there were 150, 160 pages of original claims, the vast majority of which were limited to this multiplex bus, that in my view somebody skilled in the art reading that patent application specification would have predicted, and there's some speculation involved in this, that the result would have been claims that were limited to a multiplex bus, and certainly not one that would cover the JEDEC-compliant SDRAM that has a chip select line which is the antithesis of what was stated in the first sentence of the present invention not requiring such.

Q. And I guess one way we could test the accuracy of your speculation would be to go back in time and talk to anyone who at the time looked at the application and formed their own views, correct?

A. I'm not quite sure if that would be a test of my view, it would be someone else's opinion.

Q. When you say multiplex bus, let me just make sure I understand. Do you mean a bus where necessarily either data, address or control information is multiplexed with something else, such as data being

multiplexed with address or address being multiplexed with control?

A. No, sir, I meant the limitations --

Q. Mr. Nusbaum, if the answer is no, sir, that's great, that's all I needed, we don't need to take any more time. Because I want to go to this issue of others looking at the application, and I want to bring up 2214-A, if we can, RX-2214-A.

This is a translation, maybe we can enlarge it a little bit on the screen, this is a translation of a document originally written in Japanese, Mr. Nusbaum, and did you in developing your view as to what a patent attorney, a reasonable patent attorney or engineer would think upon looking at the original '898 application, did you consider the fact that at Mitsubishi, they, in fact, asked someone, or a group of people, to consider that very application?

A. I've never seen this document before, I certainly didn't consider that, no.

Q. Okay, I want you to take a look at it, and do you see under guideline, which is halfway down the page, it says, "Do not discuss Rambus interface." Do you see that?

A. Yes.

Q. Do you understand Rambus interface to be the bus

that?

A. Yes.

Q. That's a description consistent at least with the original '898 application or the PCT application, one application, 150 claims, correct?

A. It's consistent with that, yes.

Q. I want to go to RX-2212, if we could. Now, this is in Japanese and I want to draw your attention to it in this fashion first and then to the translation because it's not all in translation, as you'll see in a minute. If you can enlarge it.

Now, you see how there's a box in the upper left

is a document that you were not shown by complaint counsel before you came to your view as to what somebody seeing the original '898 application would think, correct?

A. This is a document that I don't recall having seen before.

Q. Let's go to page 3. This is a translation of the document. And I want to draw your attention, we've talked about the number 103 earlier on the Japanese version, I want to draw your attention to 103, and then the content that goes below it, and you'll see in the lower right section, it starts, "Adjust access time in the access time register that can be adjusted by bus." Do you see that?

A. I do see it.

Q. And do you know whether that's a description of adjusting latency through the use of the register that you talked about earlier?

MS. MICHEL: Objection, Your Honor. Mr. Nusbaum stated he's never seen this document before and he's being asked questions about what it means.

JUDGE McGUIRE: Well, I think an adequate and a connection has been shown. If you can't answer the question, sir, don't hesitate to say I don't know, but I'll otherwise give counsel here some leeway on this

line of questioning.

BY MR. STONE:

Q. And I will not belabor it, I hope, Your Honor.

Just one more point on this document, Mr. Nusbaum. Do you see over below 103, it says, "Access adjustment," and then it says, "Important content."

A. I see that, yes.

Q. Do you know whether in 1993 someone looking at the original '898 application, not someone speculating, but either a prudent patent attorney or a person of

[illegible] that application

don't know whether this document is taking that into account or not.

BY MR. STONE:

Q. Do you know whether a person of ordinary skill in the art in 1991 or '92 or '93 would have understood that the inventions described in the '898 application were not necessarily limited to use in conjunction with a narrow bus?

A. I've given my opinion on how the information is presented in the patent specification with an emphasis on narrow bus, but I can't speak to that question.

Q. Because you do know, don't you, based on the testimony you've given us earlier today and the work you've done, you do know that you can use a programmable cast latency with a bus that is not narrow?

A. First of all, with respect to programmable cast latency, you certainly can use programmable cast latency without a narrow bus, as I've testified with respect to Release 4. I guess the confusion in your question is to the extent that it's saying that there's programmable cast latency, per se, described in the application, I can't speak to that.

Q. No, I know you can't. I know, I understand you can't. I understand you're -- that you've limited yourself with respect to what you can speak to about the

application, I didn't have application in my question, so let me put it to you again. I'm trying to stay in the areas where I think you've said that you have the ability to express opinions. So, let me try it again and see if we can't.

Isn't it correct that programmable cast latency, as you've testified earlier today, can be utilized in SDRAMs that do not have narrow buses?

A. Yes.

Q. And can't you also use dual edge clocking without the presence of the narrow bus?

A. Yes.

Q. And you can use PLL without the presence of a narrow bus?

A. Yes.

Q. And you can use variable burst length without the presence of a narrow bus?

A. Yes.

Q. Now, let's go to 2213, if we can.

JUDGE McGUIRE: RX?

BY MR. STONE:

Q. RX-2213, I need that reminder. And the document is in Japanese, and we're going to go to page 4. Go back, if you would. Go back to the Japanese. 2213, page 1, my fault. This is the same document we looked

at earlier, if you'll accept my representation on that, Mr. Nusbaum, except someone has added comments up along side claim 103 in the right-hand margin where they've written, "Latency, SDRAM," and then something that I think is in Japanese.

So, we have that additional comment to look at, and we're going to go to the translation, which is page 4. And you'll see, "New marginal note: Between latency and SDFAM," as opposed to SDRAM. "New marginal note: Between latency and SDFAM," except when I read it it was an R instead of an F. So, we have that comment added.

And what I want to know is whether you think as part of your opinion is it inconsistent with your opinion that someone in 1993 looking at the application would see a relationship between latency and SDRAM in claim 103 of the original '898 application. Is that consistent with or inconsistent with your opinion that you expressed earlier about what you would expect?

A. I've expressed an opinion that claim 103 is unequivocally limited to a bus that carries substantially all address, data and control signals, and has substantially fewer lines than are contained in a single address. But that's not to say that it's impossible for someone to look at that claim and see some connection.

Q. So, if someone looked at the claim and saw a connection between latency and SDRAM, that would be something other than what you would have expected based on your analysis and what you've testified to earlier, correct?

A. What I testified to earlier that someone would not have presumed that there were unnecessary limitations. Somebody could see a relationship and make a connection, and yet I believe because there were 14 U.S. patents cited in the background of the invention, that whoever drafted that claim felt that it was certainly necessary to have that limitation in there to make the claim patentable.

Q. Let's look at RX-2211, page 1. Most of this is in Japanese, as you'll see, but I want you to blow up, if you could, the right-hand column. And I want you to take a look two-thirds of the way down where it says, "Modifiable register." Do you see that? That part you can read, right?

A. Yes, I can.

Q. And then below that it says, "Access time approximately equal to SDRAM latency." Do you see that?

A. Yes.

Q. Do you understand that to be a reference to the variable latency or programmable latency feature that

you've talked about earlier in SDRAM?

MS. MICHEL: Objection, Your Honor. We don't know anything else that was on the front page of that document, and Mr. Nusbaum is being asked to take a couple of words completely out of context, for all he knows.

JUDGE McGUIRE: Mr. Stone, response?

MR. STONE: I think that you don't need anymore words than this. We could give the whole translation, but all I want to refer to is "access time is approximately equal to SDRAM latency." That's the point.

JUDGE McGUIRE: Overruled. I'll hear it. You can go into it again on any redirect.

BY MR. STONE:

Q. Do you have the question in mind, Mr. Nusbaum?

A. Could you repeat it, please?

Q. Sure. Do you understand this phrase, "Access time approximately equal to SDRAM latency" to be a reference to the programmable latency feature of SDRAM that we talked about earlier today or that you testified to earlier today?

A. I could speculate, and I would be happy to, if you would like me to, but I don't know for sure --

JUDGE McGUIRE: The court does not wish to hear,

you know, anymore speculation at this point. If you want to ask a question that you can have answered, I'll give you that opportunity. But it's not giving the court any good at this point to hear any further speculation.

BY MR. STONE:

Q. Let me go to one other document, if I can, Your Honor. RX-2203, page 3. Again, this is a translation. I want to draw your attention to the date, first, in the right-hand corner, 13 July 1993, Mr. Nusbaum.

A. I see that.

Q. And then I want you to go down with me, if you would, to the conclusions. Is it consistent with your opinion expressed earlier that in July of 1993 someone looking at the '898 application would have concluded that based on the specifications of the DRAM on the Rambus, that there are many different kinds of development and that the patent will be one that is separate from the bus? Do you see all that discussion there? Is that consistent or inconsistent with what you presumed a reasonable patent attorney would have concluded?

A. I haven't had an opportunity to digest paragraph 2, if you would give me a minute, please. I have no idea what -- precisely what this translation, which is

not in very good English, means.

Q. Did you as part of your preparation to testify read the opening statements?

A. I read part of the opening statement.

Q. You probably read Mr. Royall's and Mr. Oliver's and not mine, but did you, as part of that review of the opening statements, or any of the work you did, look at the Siemens and IBM documents that I talked about in my opening?

A. I don't believe so. And I don't know what documents you're referring to, so I don't think I read them.

that Rambus might get claims which read on SDRAM and DDR?

A. You're asking me a question whether someone might conclude? That's what you asked.

Q. Fine, let me narrow it down. Would a reasonably prudent patent attorney or a person of ordinary skill in the art in 1995 looking at the patents which had issued to Rambus and the applications Rambus had filed which were then publicly available have concluded that Rambus was likely to ultimately obtain patent coverage for SDRAM and DDR SDRAM?

A. I haven't reviewed the claims in the issued patents to take those into account which are part of your question.

Q. Okay. You testified earlier in terms of your background that one of the things that you have done is written hundreds of infringement opinions and invalidity opinions?

A. I did not testify to that earlier.

Q. Not to hundreds, am I wrong about that?

A. I testified that I wrote responses to hundreds of communications from the Patent & Trademark Office in the form of patent amendments. I have written numerous invalidity and noninfringement opinions. I don't believe I gave a number.

complaint counsel wish to engage in further redirect?

MS. MICHEL: No redirect, Your Honor.

JUDGE McGUIRE: Okay, thank you, Mr. Nusbaum, you are excused.

THE WITNESS: Thank you.

JUDGE McGUIRE: Thank you for your testimony. I assume that that concludes the presentation for today. Is that correct?

MR. OLIVER: Yes, it does, Your Honor.

MR. STONE: May I just move in exhibits, they are RX -- they are all RXs, 2214-A.

JUDGE McGUIRE: One at a time.

MR. STONE: Sure. 2214-A.

MS. MICHEL: We would object to all of the documents which were shown to Mr. Nusbaum, all of the RXs on the basis that no foundation has been laid with this witness or another as to these documents as to what they are.

MR. STONE: Well, the foundation for these documents, Your Honor, is one of the things that we tried to cover with our stipulation, and if need be, as you know, these are Mitsubishi documents which Judge Timony ordered produced.

JUDGE McGUIRE: Overruled. They're entered. At least that one is entered. Is it the same objection for

all of them? If so, I am going to enter all of them.

MS. MICHEL: Yes, Your Honor, it would be the same objection for each of the RXs.

JUDGE McGUIRE: Then you are overruled, they're entered. If you can just go back and state what they are.

MR. STONE: Yes, Your Honor, 2214-A, 2212, 2213, 2211, and 2203.

JUDGE McGUIRE: Okay, entered at this time.

(RX Exhibit Numbers 2203, 2211, 2212, 2213, 2214-A were admitted into evidence.)

JUDGE McGUIRE: Anything else?

MR. STONE: Your Honor, no, although we probably should alert you, tomorrow we're probably going to get to deposition testimony, I believe, that complaint counsel want to offer.

JUDGE McGUIRE: Are we talking about the taped deposition by Dr. Oh, is that what we're talking about?

MR. OLIVER: Your Honor, it's depending upon the timing. Either Dr. Oh or a Mr. Reece Brown.

JUDGE McGUIRE: Well, we're not going to entertain his testimony until I have had a chance to reach the order on the opposition that's been raised. I'm glad we brought this up. How soon can I anticipate a response to that objection on the issue of the -- I

think Dr. Oh's testimony?

MR. OLIVER: Either by 5:00 today or by first thing tomorrow morning.

JUDGE McGUIRE: Okay. Well, I at this point, I'm not going to allow any testimony by Dr. Oh, and I keep wanting to say Dr. No, because of my James Bond mode, until I've had the chance to issue any order. So, let's not intend on going into that on Tuesday. Now, is there something else we need to talk about?

MR. STONE: I think they are then prepared to go with deposition testimony from Reese Brown and we're prepared to read our responsive portions of that. I think part of that is video and part of that is going to be ten minutes or so of what was not videoed.

JUDGE McGUIRE: Don't forget we're starting at 11:00.

MR. STONE: Starting at 11:00.

JUDGE McGUIRE: Are we clear on everything? See you in the morning, hearing adjourned.

(Whereupon, at 4:07 p.m., the hearing was adjourned.)

C E R T I F I C A T E O F R E P O R T E R

DOCKET/FILE NUMBER: 9302

CASE TITLE: RAMBUS, INC.

HEARING DATE: MAY 12, 2003

I HEREBY CERTIFY that the transcript contained herein is a full and accurate transcript of the notes taken by me at the hearing on the above cause before the FEDERAL TRADE COMMISSION to the best of my knowledge and belief.

DATED: 5/13/03

Sally Jo Bowling

C E R T I F I C A T E O F P R O O F R E A D E R

I HEREBY CERTIFY that I proofread the transcript for accuracy in spelling, hyphenation, punctuation and format.

Sara J. Vance