

1 FEDERAL TRADE COMMISSION  
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 7 EXHIBITS FOR ID IN EVID  
 8 CX  
 9 Number 110 5351  
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 11 RX  
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 13 Number 250 5350  
 14 Number 562 5351  
 15 Number 1443 5351  
 16 Number 1695 5351  
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 18 DX  
 19 Numbers 62-94 5459  
 20 Numbers 95-99 5581  
 21 Number 100 5516  
 22 Number 101 5536  
 23 Number 102 5555  
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 25 Numbers 104-109 5581

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UNITED STATES OF AMERICA  
FEDERAL TRADE COMMISSION

In the Matter of: )  
Rambus, Inc. ) Docket No. 9302  
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Monday, June 16, 2003  
9:30 a.m.

TRIAL VOLUME 28  
PART 1  
PUBLIC RECORD

BEFORE THE HONORABLE STEPHEN J. McGUIRE  
Chief Administrative Law Judge  
Federal Trade Commission  
600 Pennsylvania Avenue, N.W.  
Washington, D.C.

Reported by: Josett F. Hall, RMR-CRR

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## P R O C E E D I N G S

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JUDGE McGUIRE: This hearing is now in order.

4

5

Counsel, good morning. We want to say hi to you back again, Mr. Detre. We heard the good news and we're very pleased to hear that.

6

7

MR. DETRE: Thank you very much, Your Honor.

8

JUDGE McGUIRE: Congratulations.

9

MR. DETRE: Thank you, Your Honor.

10

JUDGE McGUIRE: Any items we need to take up

11

before we get started this morning?

11

b few exhibits

11

b

exhibits

1 MR. DETRE: RX-1443, a Toshiba document about a  
2 meeting Mr. Kellogg attended.

3 MR. OLIVER: No objection.

4 JUDGE McGUIRE: Entered

5 (RX Exhibit Number 1443 was admitted into  
6 evidence.)

7 MR. DETRE: RX-1695, another e-mail by  
8 Mr. Kellogg.

9 MR. OLIVER: No objection.

10 JUDGE McGUIRE: Entered.

11 (RX Exhibit Number 1695 was admitted into  
12 evidence.)

13 MR. DETRE: And RX-562, some JEDEC meeting  
14 minutes.

15 MR. OLIVER: No objection.

16 JUDGE McGUIRE: Entered.

17 (RX Exhibit Number 562 was admitted into  
18 evidence.)

19 MR. OLIVER: Your Honor, we also wish to move  
20 in one exhibit, CX-110, the meeting minutes from the  
21 42.5 subcommittee of June 1996.

22 MR. DETRE: No objection.

23 JUDGE McGUIRE: So entered.

24 (CX Exhibit Number 110 was admitted into  
25 evidence.)

1 JUDGE McGUIRE: Thank you very much.  
2 Anything else we need to take up this morning  
3 before we begin?

4 MR. OLIVER: No, Your Honor.

5 JUDGE McGUIRE: Then at this time complaint  
6 counsel may call its next witness.

7 MR. OLIVER: Thank you, Your Honor.

8 Complaint counsel calls Professor Bruce Jacob.

9 JUDGE McGUIRE: Okay. Sir, would you please  
10 approach the bench and you'll be sworn in by the court  
11 reporter.

12 - - - - -

13 Whereupon --

14 BRUCE LEDLEY JACOB

15 a witness, called for examination, having been first  
16 duly sworn, was examined and testified as follows:

17 JUDGE McGUIRE: Go ahead, Mr. Oliver.

18 DIRECT EXAMINATION

19 BY MR. OLIVER:

20 Q. Good morning, Professor Jacob.

21 A. Good morning.

22 Q. How are you today?

23 A. I'm good.

24 Q. Could you please state your full name for the  
25 record.

1 A. Bruce Ledley Jacob.

2 Q. Professor Jacob, what is your current  
3 position?

4 A. I'm an associate professor at the University of  
5 Maryland in the electrical and computer engineering  
6 department.

7 Q. How long have you been a professor at the  
8 University of Maryland?

9 A. Six years.

10 Q. Are you tenured?

11 A. Yes, I am.

12 Q. When did you get tenure?

13 A. This past year.

14 Q. Congratulations.

15 A. Thank you very much.

16 Q. What does it mean to receive tenure at the  
17 University of Maryland?

18 A. It's a lifetime appointment and it means that  
19 you've done a very good job of doing research and  
20 advising students, employing students, that sort of  
21 thing, teaching.

22 Q. Could you please describe in general terms your  
23 field of research.

24 A. In general terms, I'm a computer architect and  
25 I study memory systems, meaning DRAM systems and cache



1 systems and that sort of thing.

2 Q. Now, why did you decide to specialize in memory  
3 systems?

4 A. Because it is perhaps the most important facet  
5 of computer design when you're trying to build faster  
6 systems, systems that perform better. The memory  
7 system is more important than speeding up the CPU at  
8 this point.

9 Q. Professor Jacob, let me take a step back and  
10 ask first about your educational background.

11 Did you receive an undergraduate degree?

12 A. Yes, I did.

13 Q. What was that degree?

14 A. The honors baccalaureate, a bachelor's,  
15 cum laude in mathematics from Harvard.

16 Q. Now, after graduating from Harvard, did you do  
17 any professional work relating to computer  
18 engineering?

19 A. Yes, I did.

20 Q. What was your first job in computer  
21 engineering?

22 A. I was a software engineer at  
23 Boston Technology.

24 Q. What did you do at Boston Technology?

25 A. I was -- I designed the software applications

1 for their embedded system.

2 Q. Can you explain in a bit more detail what your  
3 responsibilities were there?

4 A. I was building their voice mail system. It's a  
5 distributed telecommunications product and I was  
6 writing the software code that would implement things  
7 like foreign-language systems, Japanese, French,  
8 Spanish.

9 Q. Now, after Boston Technology, did you take  
10 another job in the computer engineering field?

11 A. Yes, I did.

12 Q. What was your second job?

13 A. I worked for a company called Priority Call  
14 Management. I was the sole engineer for the first nine  
15 months or so and I was the system architect. I  
16 implemented their product. I designed it and  
17 implemented it. It was also a distributed  
18 telecommunications product with a slightly different  
19 focus than Boston Technology's.

20 Q. Now, at some point did you decide to pursue  
21 graduate studies?

22 A. Yes, I did.

23 Q. And what graduate work did you pursue?

24 A. I obtained a master's and Ph.D. in computer  
25 science and engineering at the University of Michigan

1 in Ann Arbor.

2 Q. Can you please explain in a little bit more  
3 detail your field of study in your graduate studies?

4 A. I was trained to be a computer architect.

5 Q. What does that mean?

6 A. That means that I studied the design of complex  
7 chips and systems of chips, so, for example, CPU chips,  
8 memory controller chips and DRAM chips.

9 Q. Did you write a master's thesis?

10 A. Yes, I did.

11 Q. What was the subject of your master's thesis?

12 A. The subject was memory systems, specifically  
13 cache systems and DRAM systems and architectures.

14 Q. Can you describe in a bit more detail the  
15 subject of your master's thesis?

16 A. Yes. It was the optimization of cache systems  
17 and memory systems -- and DRAM systems, as well as disk  
18 subsystems. The optimization, for instance, in a given  
19 technology and cost, the performance parameters, what's  
20 the best arrangement of the system.

21 Q. Now, did your master's thesis work inBt

19

2 Q. Can you please describe in a bit more detail the

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Q. Iapt

Waldorf, Maryl 's thesis?

1           A. The DRAMs of the day. EDO, fast page mode,  
2 that sort of thing.

3           Q. Now, did you write a Ph.D. dissertation?

4           A. Yes, I did.

5           Q. What was the subject of your Ph.D.  
6 dissertation?

7           A. It was also in memory systems, so specifically  
8 cache systems and DRAM systems, architectures as well  
9 as software means for controlling their operation.

10          Q. Now, when did you become a professor at the  
11 University of Maryland?

12          A. In the fall of 1997.

13          Q. And since becoming a professor at the  
14 University of Maryland have you done any research  
15 involving DRAM architectures?

16          A. Yes, I have.

17          Q. We'll talk in just a moment about the specific  
18 studies that you've conducted, but before we do, could  
19 you just mention what types of DRAM architectures  
20 you've evaluated in the course of your studies.

21          A. Yes. We evaluated fast page mode; EDO;  
22 synchronous DRAM, SDRAM; several different Rambus  
23 designs, including concurrent Rambus and direct Rambus;  
24 SyncLink DRAM, SLDRAM; DDR; DDR-II. So a very wide  
25 range.

1           Q. Now, I'd like to talk a bit about the specific  
2 studies that you've conducted, and perhaps we'll just  
3 simply try to take them in chronological order if we  
4 could.

5                   What was the first work that you did at the  
6 University of Maryland involving DRAMs?

7           A. In the winter of '98, so this is the  
8 January-February time frame, I began a study of -- a  
9 comparative performance evaluation of different DRAM  
10 architectures that were commercially available at the  
11 time, including fast page mode, EDO, SDRAM, concurrent  
12 Rambus and direct Rambus, which had just been defined I  
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1 Q. Now, in the case of this study that you started  
2 in 1998, who wrote that software?

3 A. I wrote some of it and my graduate students  
4 wrote some of it.

5 Q. Now, can you please explain in a little more  
6 detail what your role in that study was?

7 A. Well, as I said, I wrote some of the software.  
8 I directed the work of my graduate students, told them  
9 what experiments to run, how to plot the results. I  
10 looked at the results, you know, gained the insights.  
11 I wrote the bulk of the paper.

12 Q. How long did it take to complete that study?

13 A. The study -- the research took around nine  
14 to -- somewhere between nine and twelve months, and the  
15 paper write-up took around three, four, five months.

16 Q. Why did it take so long to complete the study?

17 A. Because this is nontrivial work. This is what  
18 architecture design is about. That one study  
19 represents one architectural investigation.

20 Q. Now, did you publish the results of that  
21 study?

22 A. Yes, I did.

23 Q. And where was it published?

24 A. It was published in 1999 in ISCA, the

1 is the premier forum for research in computer  
2 architecture.

3 Q. Now, did you receive any type of award in  
4 connection with that study?

5 A. Yes, I did. For this research I -- or based  
6 upon this research I received the Prestigious Career  
7 Award from the National Science Foundation for my work  
8 in DRAM systems and architectures.

9 Q. What is the Prestigious Career Award from the  
10 National Science Foundation?

11 A. It's an award for young professors who do  
12 outstanding work.

13 Q. Now, what was the next study that you  
14 conducted at the University of Maryland in connection  
15 with DRAMs?

16 A. Well, the first thing we did was to extend  
17 that study, for example, adding in DDR to the mix and  
18 looking at a handful of other parameters, and  
19 published that in the IEEE Transactions on Computers  
20 in 2001.

21 Q. Okay. Can you please describe that extension  
22 of the study in a little more detail?

23 A. Well, for example, we looked at more  
24 architectures, changed the model so that we could  
25 obtain more -- obtain more information.





1 what parameters to graph and how, and I wrote pretty  
2 much the entire paper on that one.

3 Q. How long did it take to complete that study?

4 A. That study began in early 1999 and ran through  
5 late 2000, early 2001, and the study was published in  
6 2001 also in ISCA, the International Symposium on  
7 Computer Architecture. That was about a  
8 year-and-a-half study.

9 Q. And again, why did it take so long to complete  
10 that study?

11 A. Because it's nontrivial. There's a lot of work  
12 to these types of studies.

13 Q. Now, since the completion of the extension  
14 study that was published in the IEEE and the  
15 higher-level study you just mentioned was published in  
16 the International Symposium on Computer Architecture,  
17 have you done any additional work at the University of  
18 Maryland involving DRAMs?

19 A. Yes. I continue to direct a fairly large  
20 group of Ph.D. students who are investigating advanced  
21 issues in the design of DRAMs and DRAM systems, and  
22 currently we are pulling together a number of studies  
23 to put into a large treatise on DRAM systems and  
24 architectures.

25 Q. Do you have plans to publish that treatise?

1 A. Yes, I do.

2 MR. OLIVER: Your Honor, at this point  
3 complaint counsel tenders Professor Bruce Jacob as an  
4 expert in the field of memory architectures and  
5 systems.

6 JUDGE McGUIRE: Any opposition by respondent?

7 MR. DETRE: No opposition to the extent that  
8 Professor Jacob can testify based on an academic  
9 understanding of those fields, but if he -- since he  
10 doesn't have any experience in actual DRAM design --

11 JUDGE McGUIRE: You can take that up on  
12 cross-exam. Okay? Otherwise, he's deemed qualified in  
13 that area as an expert.

14 MR. OLIVER: Thank you, Your Honor.

15 BY MR. OLIVER:

16 Q. Professor Jacob, before we discuss your  
17 conclusions in detail, could you please summarize the  
18 questions that you were asked to answer?

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1 intellectual property rights over the work that JEDEC  
2 was doing based on the '898 application.

3 I was asked to look at Rambus patents that  
4 were pending at the time and granted at the time,  
5 looking at the claims in those patents to see if those  
6 claims would cover work that was going on in JEDEC  
7 42.3.

8 And I was asked to look at the implications of  
9 modern redesign, what if DRAM -- what if the DRAM  
10 industry had to design new DRAMs to remove the  
11 technologies under dispute and replace them with  
12 alternatives.

13 Q. Let's look at these questions one at a time if  
14 we could, and starting just with a general overview,  
15 could you please summarize briefly your conclusion as  
16 to whether in the 1991 to 1996 time period engineers  
17 had available to them technological alternatives to the  
18 four technologies at issue in this case.

19 MR. DETRE: Objection, Your Honor.

20 Professor Jacob has not done any kind of  
21 modeling or testing or study of the economic  
22 feasibility of his alternatives. Given that, it's  
23 speculative. There is case law that alternative design  
24 evidence should not be admitted in the absence of some  
25 sort of modeling or testing that those alternatives

1 would actually be feasible or work.

2 So we object on the grounds of speculation.

3 JUDGE McGUIRE: Overruled.

4 MR. OLIVER: Thank you, Your Honor.

5 BY MR. OLIVER:

6 Q. Professor Jacob, do you have the question in  
7 mind?

8 A. No, I do not.

9 Q. Let me restate it then.

10 Could you please summarize briefly your  
11 conclusion as to whether in the 1991 to 1996 time  
12 period engineers had available to them technological  
13 alternatives to the four technologies at issue in this  
14 case.

15 A. Yes, they did.

16 Q. And can you please state briefly your  
17 conclusions as to whether Rambus' '898 patent  
18 application or the patents listed in Rambus'  
19 withdrawal letter to JEDEC would have alerted  
20 reasonable engineers that Rambus could claim patent  
21 rights over the subject matter of JEDEC's SDRAM and  
22 DDR SDRAM work?

23 MR. DETRE: Objection, Your Honor.

24 Professor Jacob, based on his own definition of  
25 a person of ordinary skill in the art to which that

1 patent application relates, is not a person of ordinary  
2 skill because he does not have the DRAM design  
3 experience required, and he simply cannot testify about  
4 what somebody who is of ordinary skill in that art  
5 would have understood from looking at that patent  
6 application.

7 He's a very qualified gentleman in many  
8 respects, but he's not qualified to speak to that  
9 topic.

10 JUDGE McGUIRE: Mr. Oliver, any response?

11 MR. OLIVER: Yes, Your Honor. We will be going  
12 through the bases for his conclusion in quite a bit of  
13 detail. There's ample opportunity for Mr. Detre to go  
14 into that on cross-examination.

15 JUDGE McGUIRE: Overruled.

16 MR. OLIVER: Thank you, Your Honor.

17 THE WITNESS: I believe the question is related  
18 to whether they would have suspected anything based on  
19 the information, and the answer is no, they would not  
20 have.

21 BY MR. OLIVER:

22 Q. Can you please summarize briefly your  
23 conclusion as to whether a reasonable engineer would  
24 conclude that claims in certain of Rambus' pending  
25 patent applications in the 1991 to 1996 time period or

1 in the issued '327 patent could cover technologies that  
2 were the subject of JEDEC's SDRAM and DDR SDRAM  
3 standards?

4 A. Yes. Claims covered the work that was going on  
5 in JEDEC 42.3.

6 Q. And could you summarize briefly your conclusion  
7 as to what the technical implications would be today of  
8 redesigning SDRAM and DDR SDRAM products to incorporate  
9 alternative technologies in place of the four  
10 technologies at issue.

11 A. If one were to redesign DRAMs to get rid of all  
12 of the technologies in dispute and replace them with  
13 alternatives, it would result in a DRAM that is not  
14 compatible with any JEDEC-compliant system.

15 Q. Let's focus then on the first question that  
16 was posed to you, and before we walk through some of  
17 the specific alternatives, I'd like to explore just  
18 briefly the work that you did to arrive at your  
19 conclusions.

20 Could you please summarize first, again  
21 briefly, what types of textbooks, treatises, articles,  
22 publications, et cetera, or other engineering  
23 materials that you consulted in the context of doing  
24 your work.

25 A. Well, I consulted a large range of engineering

1 material, including, for example, treatises, technical  
2 articles, things that I found on the Web.

3 I also read through an enormous number of  
4 JEDEC minutes and read through the presentations made  
5 at JEDEC meetings. These are the attachments of the  
6 minutes.

7 I read through -- well, yeah, I read through  
8 those presentations.

9 And I also consulted with engineers in the DRAM  
10 industry to confirm my understanding of, for instance,  
11 what was done in those meetings, what was being  
12 presented in those meetings.

13 Q. Just to follow up from what you mentioned, the  
14 Web, did you conduct any Internet searches in  
15 connection with your work?

16 A. Yes. Absolutely.

17 Q. And did you find any useful materials in the  
18 course of --

19 A. Oh, yes. Yes.

20 Q. You mentioned JEDEC documents, particularly  
21 minutes.

22 Were you referring to minutes from the  
23 meetings --

24 A. Yes. I'm sorry. Minutes of the meetings of  
25 the 42.3 subcommittee.

1 Q. And what time --

2 A. And presentations made.

3 Q. What time period of the minutes did you  
4 consult?

5 A. 1991 to 1996.

6 Q. And you also mentioned that you interviewed a



1 architecture, programmable CAS latency is a  
2 convenience that allows parts of different  
3 generations with potentially different performance  
4 characteristics to coexist in the same system and  
5 have the same performance in that system, have the  
6 same behavior.

7 Q. Now, focusing on the 1991 to 1996 time period,  
8 what alternatives, if any, existed to programmable  
9 CAS latency as used in the JEDEC SDRAM and DDR SDRAM  
10 standards?

11 A. Well, we have a nice demonstrative here.

12 For example, JEDEC could have chosen to use  
13 fixed CAS latency parts.

14 They could have decided to program CAS latency,  
15 essentially use a fixed CAS latency part, by doing so  
16 after the packaging steps or by blowing fuses on the  
17 DRAM.

18 They could have chosen to scale the CAS latency  
19 with the clock frequency.

20 They could have chosen to use dedicated pins to  
21 transmit the latency information to the DRAM, so  
22 between the memory controller and the DRAM.

23 They could have chosen to explicitly encode the  
24 latency information in the control packet.

25 And they could have decided, for example, to

1 stay with an asynchronous style DRAM.

2 Q. Okay. Let's look at these individually if we  
3 could, starting with fixed CAS latency.

4 What do you mean by "fixed CAS latency"?

5 A. That means that a part would only have the  
6 ability to perform one -- well, to perform with one  
7 latency, to respond with one latency.

8 Q. Now, how could a manufacturer fix the CAS  
9 latency?

10 A. Well, the manufacturer, for example, could  
11 decide to define a fixed latency in the design stage  
12 and it could decide to define the fixed latency in the  
13 processing stage or it could decide to define the fixed  
14 latency in the packaging phase.

15 Q. Okay. Starting with the design stage, how  
16 would a manufacturer fix the --

17 JUDGE McGUIRE: Mr. Oliver, before we proceed,  
18 do you intend to have the screens marked as DX  
19 exhibits?

20 MR. OLIVER: Yes, Your Honor, I do.  
21 Unfortunately, we don't have a color copy with us.  
22 We'll see if we can print it out during the lunch break  
23 and have it to the court by this afternoon.

24 JUDGE McGUIRE: And then at that time we'll go  
25 into each one and have it marked? Is that the

1 appropriate time or is it better to do that as we go?  
2 Only for the record.

3 MR. OLIVER: We could assign numbers as we go.

4 JUDGE McGUIRE: That might be easier so we'll  
5 understand it as we go back through it. I don't mean

14 3 STONcGUIWi7, evnDiyour fi un onetat oht, but e go?

1           DX-67 would be a slide entitled Fixed CAS  
2 Latency.

3           BY MR. OLIVER:

4           Q. Professor Jacob, if you could then explain with  
5 reference to DX-67 how a manufacturer could fix  
6 CAS latency at the design stage.

7           A. Yes. Yes. At the design stage, the DRAM  
8 manufacturer would design a part to only perform, you  
9 know, with one CAS latency.

10           For example, this picture shows that you would  
11 have some CAS latency circuitry, but it would only be  
12 told to use CAS latency 2, for example.

13           Q. Now, could you explain how a manufacturer could  
14 fix CAS latency in the processing stage.

15           A. Yes. I think there's another demonstrative for  
16 that.

17           Q. Well, if we could move up to DX-68, please.

18           A. This would be a metal mask option, and the  
19 idea is that you would have hard-wired onto the chip  
20 the value 2 and the value 3 and during the processing  
21 steps as one of the final steps within the processing

1 Q. Now, you referred to a metal mask.

2 What is a metal mask?

3 A. A metal mask is one of the final steps in --  
4 well, the metal mask is the actual -- the mask that  
5 helps you lay down a piece of metal onto the  
6 semiconductor chip and it's one of the final steps in  
7 the processing stages.

8 Q. Would it be fair to say that it helps to  
9 establish -- to lay down connections among different  
10 elements in the chip?

11 A. Yes. I'm sorry. Yes. I forget who I'm  
12 speaking with.

13 Yes, this is -- when you lay down pieces of  
14 metal on a chip, these establish different connections  
15 between the circuits. That's how circuits talk to each  
16 other, through metal wires.

17 So if there's no metal wire connecting two  
18 things, that means that there is no circuit between  
19 them, there's no connection between them. That means  
20 they can't interact.

21 Q. Now, DX-68 shows a connection between the box  
22 CAS 2 and the CAS latency circuitry, but I understand  
23 from what you said that it would be equally possible at  
24 the metal mask stage to establish a connection, instead  
25 of between CAS 2 and the CAS latency circuitry, between

1 CAS 3 and the CAS latency circuitry?

2 A. Yes. Exactly.

3 Q. Now, can you please explain how a manufacturer  
4 could fix CAS latency during the packaging phase?

5 A. Yes. I believe we have a demonstrative for  
6 that as well.

7 Q. That would be DX-69.

8 A. Yes.

9 In this option, the part through the  
10 processing phases would have the configuration shown  
11 here.

12 So for example, you have two hard-wired values  
13 of CAS 2 and CAS 3 both connected to the CAS latency  
14 circuitry, but they would be connected through a  
15 multiplexer, labeled "mux" in the figure, and the  
16 selection of whether it would be a CAS latency 2 or CAS  
17 latency 3 would be done by that mux and the mux would  
18 be hard-wired to either the power pins or the ground  
19 pins, and this is something that could be done with a  
20 bond wire during packaging.

21 So you would simply -- you would fabricate one  
22 chip, but during packaging you would connect that mux  
23 to either power or ground and then select either the  
24 value 2 or the value 3.

25 Q. Now, you referred to a bond wire.

1           What is a bond wire?

2           A. The bond wire is a packaging mechanism that  
3 connects the semiconductor chip or, rather, the  
4 semiconductor die to the pins of the chip.

5           Q. Now, in comparison with use of a mode register  
6 to program CAS latency, what advantages, if any, would  
7 have been realized by using fixed CAS latency in the  
8 1991 to 1996 time period?

9           A. It would be potentially a simpler design.  
10 Certainly you don't have a mode register, so that's a  
11 simpler mechanism.

12           You potentially would have fewer testing  
13 stages, and again, that depends on where you decide to  
14 fix the CAS latency. For example, if you fix it  
15 earlier in the design stage, you don't actually have  
16 to test the fabricated part for multiple CAS  
17 latencies.

18           So the test costs and design costs can go  
19 down.

20           Q. You referred to a simpler design. Why do you  
21 include that as among the advantages?

22           A. Well, because you don't have to build and test  
23 a mode register.

24           Q. Are you familiar with the term "die size"?

1 Q. And what does "die size" mean?

2 A. Thank you.

3 It's the size of the semiconductor die. And  
4 the cost of manufacturing goes roughly with the area  
5 to the third power, the area of this semiconductor  
6 part, so if you have a part that is 1 percent larger,  
7 it's approximately 3 percent more expensive to  
8 manufacture.

9 So for example, if you eliminate a mode  
10 register, you eliminate some of the size of the part  
11 and it can make it smaller and therefore cheaper.

12 Q. Now, what, if anything, would be the impact on  
13 die size if JEDEC had chosen in the 1991 to 1996 time  
14 period to use fixed CAS latency rather than a mode  
15 register?

16 A. It would have been a simpler design and  
17 therefore a smaller design. In this instance you would  
18 have eliminated circuitry, you would have eliminated  
19 the mode register, and so it would have been a smaller  
20 design and therefore smaller die.

21 Q. Again compared to use of a mode register to  
22 program CAS latency, what, if any, would have been the  
23 disadvantages of using fixed CAS latency in the 1991 to  
24 1996 time period?

25 A. The -- for instance, the manufacturer would



1 have to be a bit more clear about the labeling of these  
2 devices, because if you made no changes to the memory  
3 controller, for example, it would be possible to put --  
4 well, if JEDEC had decided to standardize, for example,  
5 on two different CAS latencies and each part had a  
6 fixed latency, then it would be possible to put DIMMs  
7 with two different latencies in a system and that could  
8 potentially cause compatibility problems, but that  
9 could have been solved by building a more sophisticated  
10 memory controller.

11 So you would either have the scenario where the  
12 memory manufacturers would need to be and the memory  
13 module manufacturers would need to be more explicit  
14 about the behavior of these things and users would have  
15 to understand that or, again, you could put that onto  
16 the shoulders of the memory controller.

17 Q. If we could turn to the next alternative you  
18 mentioned, which is determining CAS latency by fuses.

19 A. Yes.

20 Q. Can you please explain what you mean by  
21 "program CAS latency by blowing fuses on the DRAM"?

22 A. Well, this would be similar to having the fixed  
23 CAS latency part because what you would have is a  
24 de facto fixed CAS latency part, but it would become  
25 that fixed CAS latency part after you've blown the

1 fuse, so this would be, for example, an option that you  
2 would do after packaging of the die so that the DRAM  
3 manufacturer could ship a part that was capable of  
4 performing as a CAS latency 2 part or a CAS latency 3  
5 part, ship that part to the OEM and the OEM would blow  
6 a fuse and it would at that point become a fixed  
7 latency part, but it would have either 2 or 3.

8 Q. I believe we have a couple of demonstratives  
9 that help explain this, if we could bring up --  
10 actually DX-70 I think will be the slide entitled  
11 Alternatives to Programmable CAS Latency with number 2  
12 highlighted and DX-71 will be the first demonstrative  
13 relating to blowing fuses. It bears the caption  
14 Set CAS Latency With Fuses.

15 Would you please use DX-71 to help explain how  
16 fuses could be used to determine CAS latency.

17 A. Yes. Depicted in this figure is a -- in the  
18 box labeled "circuitry" we have a hard-wired value of 2  
19 and a hard-wired value of 3, and these are both  
20 connected to the box labeled "CAS latency circuitry"  
21 through wires, and those wires have fuses on them, and  
22 if you blow one of those fuses, then that connection is  
23 no longer established so that after blowing one of  
24 those fuses, only the value 2 or the value 3 would be  
25 driving that CAS latency circuitry, so once you blow a

1 fuse, the part would behave as a de facto fixed latency  
2 part.

3 Q. Now, how would the fuse be blown?

4 A. It would be blown electrically after  
5 packaging.

6 Q. Is that the only way to blow a fuse?

7 A. No. No. There are laser-blown fuses as well,  
8 but those need to be blown before packaging.

9 Q. If we could pull up DX-72.

10 What does DX-72 show?

11 A. This shows a laser-blown fuse.

12 Q. And in DX-72, which would be the CAS latency  
13 that would operate on this DRAM?

14 A. In this instance CAS latency 2 would be the  
15 value that would be sent to the rest of the circuit;  
16 therefore, the circuit would behave as a fixed CAS  
17 latency 2 part.

18 Q. Now, if we could bring up the next  
19 demonstrative, which would be demonstrative DX-73.

20 This has the caption CAS Latency Hardware With  
21 Fuses - Electrical Pulse. Could you please explain  
22 what's shown in DX-73.

23 A. Yes. This is showing the blowing of the fuse,  
24 that the fuse would be blown using an electrical pulse  
25 rather than a laser, so this is something that could be

1 done after the part is packaged.

2 Q. And again on DX-73, which is the latency value  
3 that would operate on the DRAM?

4 A. It's the same as before. The value of CAS  
5 latency 2 would be driving the circuitry, so therefore  
6 the part would be a fixed CAS latency of 2 part.

7 Q. Now, with respect to the fuses that you've been  
8 discussing, do synchronous DRAMs today contain fuses of  
9 this sort?

10 A. Yes, they do.

11 Q. What's the purpose of using fuses of this sort  
12 in synchronous DRAMs today?

13 A. Most of the fuses are involved in enabling  
14 redundant storage elements so that if defects in the  
15 storage elements or the storage arrays are found, they  
16 can connect the redundant elements in place of the  
17 damaged elements.

18 Q. So in other words, it's a means of rerouting  
19 the circuitry to replace a portion of the circuitry?

20 A. Yes. Absolutely.

21 Q. Now, the fuses that are used in synchronous  
22 DRAMs today, are they laser blown or electrically blown  
23 or both or other?

24 A. They are both. They are -- some manufacturers  
25 use laser-blown fuses; other manufacturers use

1 electrically blown fuses.

2 Q. Now, compared to using a mode register to  
3 program CAS latency, what, if any, would have been the  
4 advantages in the 1991 to 1996 time period of using  
5 fuses to determine the CAS latency?

6 A. It would be potentially a simpler design. You  
7 would eliminate the mode register. It would be  
8 potentially a smaller design and therefore a cheaper  
9 design. After blowing the fuse, you would only need to  
10 test one CAS latency value instead of having to test  
11 all possible CAS latency values, so it would be a  
12 cheaper alternative potentially.

13 Q. Now, again compared with using a mode register  
14 to program CAS latency, what would have been the  
15 disadvantages to using fuses to determine CAS latency  
16 in the 1991 to 1996 time period?

17 A. Well, again, what you're dealing with is what  
18 is -- well, what is in effect a fixed CAS latency part  
19 once the fuse is blown, and it can't be used in a  
20 system until the fuse is blown, so it's a de facto  
21 fixed CAS latency part, so the manufacturers would have  
22 to be a little bit more explicit about these things and  
23 users would, you know, have to be more savvy if they  
24 were going to use these things in their systems. But  
25 again, this could be solved with the memory controller

1 redesign.

2 Q. Now, the next alternative that you mentioned I  
3 believe was scaling CAS latency with clock frequency.  
4 You have a demonstrative DX-74 which again reads  
5 "Alternatives to Programmable CAS Latency" with item  
6 number 3 highlighted.

7 Can you please explain what you mean by "scale  
8 CAS latency with clock frequency"?

9 A. Yes. Here the DRAM would not be told what  
10 latency to use but, rather, what clock frequency to  
11 use, and it would determine how many cycles that  
12 represented based upon its inherent latency.

13 Q. Well, I guess, what would actually determine  
14 what latency or what frequency to use?

15 A. Either the memory controller could tell the  
16 DRAM explicitly what frequency the bus would be running  
17 at or the DRAM could learn that information on its own  
18 by having an internal circuit that would sense the bus  
19 speed and determine, for example, if it's higher or  
20 lower than a reference and therefore it would choose  
21 between the two possible values or more.

22 Q. Could you please explain in a bit more detail  
23 how the DRAM could itself determine the operating speed  
24 of the bus.

25 A. Yes. For example, let's say that the part was

1 meant to work at either 100 megahertz or 150 megahertz.  
2 It could have an internal oscillator that would be  
3 somewhere in between, expected to run somewhere in  
4 between 100 and 150 megahertz, just to pick something,  
5 133 megahertz.

6 And it would have a simple circuit that would  
7 look at the bus frequency, the existing bus frequency,  
8 and do an edge detect to see if the bus frequency is  
9 faster than or slower than the internal reference.  
10 And if it was faster than the internal reference, it  
11 would therefore be a 150 megahertz part. If it was  
12 slower -- or, rather, it would be a 150 megahertz bus.  
13 If the external bus clock would be slower than the  
14 internal reference, then it would be a 100 megahertz  
15 bus.

16 Q. And again, just to be clear, I think you said  
17 that was one of the two options. The other option  
18 would be the memory controller signaling to the DRAM  
19 what the bus speed was?

20 A. Yes. That would be the other -- another  
21 option.

22 Q. Now, what, if any, would have been the  
23 advantages had JEDEC chosen to scale CAS latency with  
24 clock frequency rather than using a mode register to  
25 determine CAS latency in the 1991 to 1996 time period?

1           A. Well, for example, the part would always  
2 operate with the fastest latency possible rather than  
3 being told to wait longer than it would be possible.

4           So if it was capable of producing something  
5 with a latency of 2, it would produce something with a  
6 latency of 2.

7           So the systems would always be designed to have  
8 the best possible performance.

9           Q. Now, what, if any, would have been the  
10 disadvantages had JEDEC chosen to scale CAS latency  
11 with clock frequency rather than using a mode register  
12 to determine CAS latency?

13          A. Well, again, the manufacturers would need to  
14 be more precise about the labeling of these parts and  
15 the labeling of their systems and labeling them so  
16 that everyone would understand what parts are  
17 compatible with what systems, and users would be --  
18 would need to be a bit more savvy about plugging in a  
19 DIMM with these types of DRAMs on it into a system and  
20 know that the system would actually work with this  
21 DIMM.

22          Q. I believe the next alternative you identified  
23 is using an existing pin or a new, dedicated pin to  
24 identify the latency.

25          A. Yes.



1           Q. DX-75 is a slide also entitled Alternatives to  
2 Programmable CAS Latency with item number 4  
3 highlighted.

4           Can you please explain the alternative of using  
5 a pin to identify latency?

6           A. Yes. The idea is that rather than placing the  
7 value in a mode register, you send that same value over  
8 a dedicated pin, and so that pin would contain only --  
9 or it would transmit only that information during the  
10 lifetime of the DRAM.

11           While the system is operative, that value would  
12 never change, and so the information would be usable by  
13 the DRAM exactly as if the information came from a mode  
14 register, only it would be coming from the input from  
15 the pins instead, so it would be the same information.  
16 It would be used in an identical manner, only rather  
17 than holding it in the mode register you'd send it over  
18 a pin.

19           Q. Just to be clear with respect to this  
20 alternative here, you are talking about using a  
21 dedicated pin?

22           A. Yes. A dedicated pin that would, for instance,  
23 transmit only CAS latency information.

24           So you would have one pin that if it had a low  
25 voltage asserted on it, that would mean, for example,

1 CAS latency 2; if it had a high voltage, it would  
2 indicate use CAS latency 3.

3 Q. Now, would this option have required that  
4 additional pins be included in the DRAM?

5 A. Not in all cases. In many examples there are  
6 no-connect pins on DRAMs. There are pins left over  
7 after the specification is made that have no function  
8 assigned to them, and so these could have been used to  
9 transmit this information.

10 Q. Now, with respect to this alternative, would  
11 the signals on the pins change dynamically during the  
12 operation of the DRAM?

13 A. Not in a JEDEC-style system. In a JEDEC-style  
14 organization, you set that value at system  
15 initialization and it does not change throughout the  
16 lifetime of the system while the system is powered on.  
17 It's a constant value while the system is running, and  
18 so this alternative would be used in that same manner.  
19 While the system is running, the memory controller  
20 would assert the same value and it would not be  
21 changing dynamically.

22 Q. Now, what, if any, implications would that have  
23 for the type of current on the pin?

24 A. It would be a DC signal. It would not be an AC  
25 signal. It would not be changing. It would be

1 constant and therefore the receiver on the DRAM side  
2 would be much simpler.

3 The pin could be on a part of the package  
4 that's not desirable for the faster types of pins, so  
5 it would be a cheaper pin to implement. It would be a  
6 cheaper pad to locate on the DRAM die. It would be  
7 much simpler and much cheaper to add than, for example,  
8 adding another data pin or, you know, something that's  
9 expected to change rapidly.

10 Q. Now, in your opinion, what would the advantages  
11 of using a dedicated pin to determine CAS latency have  
12 been as opposed to using a mode register to determine  
13 CAS latency?

14 A. Well, it would be a simpler design because you  
15 would eliminate the mode register as well as the  
16 interface required to put information into the mode  
17 register, and it would be a smaller design and  
18 therefore a cheaper design to manufacture, so it would  
19 be simpler and cheaper.

20 Q. Now, in your opinion, what would have been the  
21 disadvantages, if any, had JEDEC chosen to use a  
22 dedicated pin to determine CAS latency as opposed to  
23 using a mode register?

24 A. If they had no-connect pins available, there  
25 would be no disadvantage. If there were no no-connect

1 pins available or not enough no-connect pins available,  
2 then you would have to add new pins to the package, and  
3 that would increase cost. But it would be relatively  
4 insignificant.

5 Q. Why do you say it would be relatively  
6 insignificant?

7 A. Because, again, as I said, these -- this type  
8 of interface, a DC-type interface, is much less  
9 expensive than adding, for instance, what they call a  
10 high-speed pin, a data-type pin.

11 Q. If we could turn then to your next alternative,  
12 explicitly identify CAS latency in the read command,  
13 and this will be marked then DX-76, the slide that's  
14 also entitled Alternatives to Programmable CAS Latency  
15 with number 5 highlighted.

16 Can you please explain what you mean by  
17 "explicitly identify CAS latency in the read command"?

18 A. By this I mean that you would have multiple  
19 commands for multiple latencies, so if you wanted to  
20 transmit or have the DRAM use two different latencies,  
21 you would have two different commands, one that says  
22 read with latency 2, one that indicates to read with  
23 latency 3, and so that information would be transmitted  
24 across the bus at the time of the command.

25 Q. Okay. So this command then would be

1 originating in the memory controller?

2 A. Yes, it would.

3 Q. And what pins would be used to transmit this  
4 command?

5 A. Well, for example, there are a number of  
6 existing pins that encode control information, for  
7 example, the RAS pin, the CAS pin, clock enable, and so  
8 forth, DQ mask and write enable, and these together  
9 form a de facto control bus with 32 possibilities for  
10 their combinations, and currently in the standard not  
11 all 32 possibilities are encoded, so you could use some  
12 of those unused combinations to encode this additional  
13 information.

14 Q. Can you please explain how five pins could send  
15 32 different commands?

16 A. Well, it's basic mathematics. If you have five  
17 variables each of which can take on two values, you  
18 have to 25 combinations, which is 32.

19 Q. So in other words, one pin can send two  
20 possibilities?

21 A. And the next pin can send 2 different values,  
22 so the two pins together can send 4 values, three pins  
23 together can send 8 different values, four pins  
24 together can send 16 different values, and five pins  
25 together can send 32 different values, and so forth.

1 Q. And I believe you identified the RAS, CAS,  
2 clock enable, DQ and then write enable --

3 A. Yes.

4 Q. -- as the pins.

5 Do you have an understanding of how many  
6 different commands will currently send synchronous  
7 DRAMs across these pins?

8 A. Yes. Far less than 32. It's on the order of a  
9 dozen.

10 Q. So in other words, there would be sufficient  
11 remaining combinations to permit this alternative?

12 A. Yes, there would.

13 Q. Now, what, if any, would have been the  
14 advantages had JEDEC chosen to explicitly identify CAS  
15 latency in the read command rather than using a mode  
16 register to program CAS latency?

17 A. The advantage would be that you would eliminate  
18 the mode register and the circuitry required to decode  
19 special commands and put that information into the mode  
20 register, so it would make the part potentially smaller  
21 and simpler.

22 Q. And would that have had any implication for  
23 cost?

24 A. Yes. That potentially would reduce the cost of  
25 the part.

1           Q.  What, if any, would have been the  
2           disadvantages had JEDEC chose to explicitly identify  
3           CAS latency in the read command rather than using a  
4           mode register?

5           A.  The disadvantage would be that it would make  
6           the decoding logic on the DRAM more complex because you  
7           would have these additional commands that would need to  
8           be decoded, so that would make the part more complex,  
9           so you'd have a trade-off there.

10           And if, for example, there were certain  
11           combinations that you had to support and you didn't  
12           want to redefine, for example, the DQ mask pins in the  
13           way I've described, it might require an additional  
14           pin.

15           Q.  Focusing on the use of existing pins for the  
16           moment, you mentioned that it might require more  
17           complex decode circuitry?

18           A.  Yes.

19           Q.  How significant would that be?

20           A.  Not very significant.  It would be on the order  
21           of the complexity that you're removing by not having to  
22           decode the initialization commands.

23           Q.  In other words, on the order of the complexity  
24           that would be removed by taking off the mode register?

25           A.  Absolutely.

1 Q. Now, by the way, this alternative of explicitly  
2 identifying CAS latency in the read command, would that  
3 require a register on the DRAM?

4 A. No, it would not.

5 Q. Would it require some means of receiving  
6 information?

7 A. Yes, it would.

8 Q. And how would that be done?

9 A. You could latch the information.

10 Q. What is a latch?

11 A. A latch is a circuit that retains its state.  
12 It's a way of capturing data and holding on to it.

13 Q. Now, how, if at all, does a latch differ from a  
14 register?

15 A. A latch is a specific implementation. A  
16 register implies how a piece of storage is being used.

17 So for instance, a register might be built out  
18 of latches, but a register is not a latch. A register  
19 could be built out of latches or D flip-flops or any  
20 number of mechanisms.

21 Q. If we could turn to the final alternative that  
22 you've listed here, and we'll now look at DX-77, which  
23 is a slide also entitled Alternatives to Programmable  
24 CAS Latency with item number 6 highlighted, stay with  
25 asynchronous DRAM (e.g., burst EDO).



1           Can you please explain what you mean by the  
2 alternative of stay with asynchronous DRAM?

3           A. Yes. Since the latency on a synchronous DRAM,  
4 the time which it drives data out onto the bus, is  
5 determined by the memory controller and the point of  
6 programmable CAS latency is to make parts of  
7 different -- potentially different generations  
8 compatible with each other, an asynchronous DRAM gives  
9 you that compatibility inherently.

10          Q. Perhaps as just a start, if you could explain  
11 your understanding of what you mean by "asynchronous  
12 DRAM."

13          A. This is the term that is used to describe DRAMs  
14 prior to SDRAMs, those who are driven off the RAS and  
15 CAS signals where the RAS and CAS actually control the  
16 operation of the DRAM rather than a clock.

17          Q. Are there similarities between asynchronous  
18 DRAMs and synchronous DRAMs?

19          A. Oh, very much so. They're very similar. They  
20 have -- they do the same thing. They have the same  
21 internal circuits.

22                 The primary difference between an asynchronous  
23 system and a synchronous system, for example, is in a  
24 synchronous system you have a system clock that is  
25 driving the memory controller and the DRAMs, in an

1 asynchronous system the system clock drives the memory  
2 controller directly. It does not drive the DRAMs  
3 directly but, rather, indirectly through the memory  
4 controller so that the clock drives the memory  
5 controller and the memory controller then drives the  
6 DRAMs through the RAS and CAS timing signals.

7 Q. Can you please explain how the memory  
8 controller would drive the DRAM through the RAS and CAS  
9 signals?

10 A. Well, those are the signals that cause the DRAM  
11 to do things. The RAS is the equivalent of a row  
12 activate system. The CAS is the equivalent of a, you  
13 know, read command or a write command.

14 Q. Now, focusing again on the early to mid-1990s  
15 time period, what, if any, would have been the  
16 advantages had JEDEC chosen to continue to develop  
17 asynchronous memory rather than using synchronous  
18 memory?

19 A. It would have been a simpler transition because  
20 the technology existed at the time. This was a  
21 technology that the engineers of the time were more  
22 familiar with. Asynchronous DRAM tended to have  
23 smaller die sizes like burst EDO at the time had a  
24 smaller die size than SDRAM and had better performance  
25 at the same speeds.

1           So asynchronous potentially had better  
2 performance and cheaper implementation.

3           Q. Now, what, if any, would have been the  
4 disadvantages had JEDEC chosen to continue to develop  
5 future generations of asynchronous relative than moving  
6 to synchronous?

7           A. I don't see enormous disadvantages. The  
8 general -- the general view is that moving to  
9 synchronous allows you to scale to higher speeds more  
10 easily and so it's a faster upgrade path.

11           It's a simpler design mechanism e to9crhvo9cto hnormo  
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93           Q. If weo could moe on now topropgrmmabaleburst.  
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1 system to use the same -- to produce the same amount of  
2 data or to read the same amount of data per  
3 transaction, and usually this is chosen to correspond  
4 with the size of the cache block in the system.

5 So that if the cache block in the system is  
6 64 bytes, the memory controller sets the DRAMs to read  
7 and write in granularities of 64 bytes, the DIMMs to --  
8 the DIMMs read and write to with a granularity of  
9 64 bytes.

10 Q. And there's a demonstrative DX-78 that consists  
11 of a slide labeled Burst Length.

12 Now, what, if any, were the alternatives to  
13 programmable burst length that existed and were  
14 available to JEDEC in the 1991 to 1996 time period?

15 A. I believe we have a demonstrative for that.  
16 Oh, yeah.

17 For example --

18 Q. Let me just mention that's DX-79, a slide  
19 entitled Alternatives to Programmable Burst Length.

20 A. So for example, the manufacturers could have  
21 used fixed burst length parts.

22 They could have programmed DRAMs to use a  
23 de facto fixed burst length by blowing fuses on the  
24 DRAM.

25 They could have used an existing pin or a new,

1 dedicated pin to transmit the information, identify the  
2 burst length.

3 They could have extended the command set so  
4 that different burst lengths would be transmitted with  
5 the read commands so that for two different burst  
6 lengths you would have two different read commands.

7 They could have used a burst terminate  
8 mechanism so that the part, for example, would use by  
9 default a burst length of eight, but systems that  
10 wanted to use a burst length of four would either  
11 implicitly or explicitly terminate the burst to a  
12 length of four instead of eight.

13 And lastly, they could have used a CAS pulse to  
14 control the data output, which means the DRAM would  
15 only return data when it saw a toggle on the CAS pin.  
16 So that if the memory controller wanted a length of  
17 eight, it would toggle CAS eight times; if it wanted a  
18 length of four, it would toggle CAS four times.

19 Q. Okay. Let's see if we can look at these one at  
20 a time.

21 Now, some of these I think will be fairly  
22 similar to the ones we looked at in CAS latency and  
23 we'll see if we can move through those a little bit  
24 more quickly.

25 The first one, use fixed burst length parts,

1 can you please explain briefly what that one entails?

2 A. Yes. So again for a fixed burst length part,  
3 you could either define the burst length to be fixed at  
4 the design phase, during the manufacturing phase or  
5 during the packaging phase.

6 And here, we are showing in this diagram the  
7 decision being made during the design phase so that the  
8 part would only have a value of 4, so this would be a  
9 hard-wired value of 4 driving your burst length  
10 circuitry, so this would be a design that would only be  
11 able to give you a burst length of 4.

12 Q. For the record, you're referring to a slide  
13 that has a caption of Fixed Burst Length and in the top  
14 box circuitry burst length 4. That will be marked as  
15 DX-80.

16 Now, is it also possible to determine the burst  
17 length in the manufacturing process?

18 A. Yes, it is.

19 Q. If we could perhaps pull up the next slide to  
20 be marked as DX-81.

21 A. This is the metal mask option, and the part as  
22 designed would have a hard-wired value of 4 and a  
23 hard-wired value of 8, but at the time of  
24 manufacturing, in one of the last steps of the  
25 processing stages you would put down a piece of metal

1 that either connects -- so you would have two masks and  
2 you would use either the one mask or the other mask to  
3 put down either one piece of metal connecting burst 4  
4 to the burst length circuitry or you would use a  
5 different mask to put down a different wire that would  
6 connect the hard-coded value of 8 to the burst length  
7 circuitry.

8 So you would have the design, the design would  
9 give you the option of doing 4 or 8, but at the time of  
10 manufacturing you would choose only one of those to be  
11 connected to your burst length circuitry, so at that  
12 point the part would become a de facto burst length  
13 part.

14 In this instance, we're showing that the  
15 hard-wired value of 4 is connected to the burst length  
16 circuitry, so that's -- that would be the part's  
17 behavior. It would have a burst length of 4.

18 Q. And does it operate in a similar manner to the  
19 way you described the metal mask option in CAS  
20 latency?

21 A. Absolutely. The same mechanism.

22 Q. And would it also be possible to determine the  
23 CAS latency at the packaging phase of manufacturing?

24 A. Yes, it would.

25 Q. And perhaps we can bring up the next

1 demonstrative which will be marked as DX-82 and that  
2 reads "Fixed Burst Length Packaging Option."

3           Could you please explain what's shown in  
4 DX-82.

5           A. Yes. This is similar to the packaging option  
6 for determining fixed CAS latency, and here you would  
7 have a burst length of 4 or a burst length of 8 as  
8 options.

9           You would have a hard-wired value of 4 or a  
10 hard-wired value of 8, both being connected indirectly  
11 to the burst length circuitry through a multiplexer,  
12 which is labeled "mux" here, and the multiplexer would  
13 choose between either 4 or 8, would choose either the  
14 value 4 or the value 8, choose between the two based  
15 upon the control signal which would be connected to  
16 either power or ground.

17           It would be essentially hard-wired to either  
18 power or ground, and that decision whether it was  
19 hard-wired to power or ground would be made at the  
20 packaging time through the use of bond wires that would  
21 connect that wire to either the power pin or a ground  
22 pin.

23           Q. Now, what, if any, would have been the  
24 advantages had JEDEC chosen to use fixed burst length  
25 rather than use a mode register to program burst



1 length?

2 A. You would have a simpler design because you  
3 would have the -- you would eliminate the mode register  
4 and eliminate the circuitry used to initialize the mode  
5 register, so it would be a smaller part, a cheaper part  
6 to manufacture, and depending upon at what point you  
7 decide to fix the burst length, it would potentially be  
8 a cheaper part to test.

9 Q. And what, if any, would be the disadvantages  
10 had JEDEC chosen to use a fixed burst length rather  
11 than a mode register to program burst length?

12 A. Just as in fixed CAS latency, the  
13 manufacturers would need to be explicit about the  
14 behavior of these parts, be very clear about the  
15 labeling of these parts. Users who would plug these  
16 parts into their systems would have to be a little bit  
17 more savvy to ensure that they did not put parts with  
18 different behavior into the same system because they  
19 might not work paystru t\*(sou )TjT e p(sou )Tj sight not w

1 compatibility issues at all.

2 Q. If we could turn to the next alternative that  
3 you identified, which I believe was use of fuses.

4 We'll pull up the next demonstrative, which  
5 will be marked as DX-83. This slide is captioned Set  
6 Burst Length With Fuses.

7 Can you please explain just very briefly what  
8 DX-83 shows?

9 A. Yes. This is similar to setting the CAS  
10 latency with fuses. And the idea is that you have the  
11 same burst length circuitry that you would have today  
12 and you would have two hard-wired values, for instance,  
13 a burst length of 4 or a burst length of 8.

14 So you would have the hard-wired value of 4 or  
15 the hard-wired value of 8, and these values would be  
16 connected indirectly to the burst length circuitry  
17 through fuses, one of which could be blown, thereby  
18 breaking the connection so that after the fuse is  
19 blown, only one of these hard-coded values would be  
20 connected to the burst length circuitry.

21 Q. As with the case of CAS latency, could these  
22 fuses be blown either with a laser or electrically?

23 A. Yes.

24 Q. If we can bring up DX-84, which does that  
25 show?

1           A. This shows blowing the fuse with a laser.

2           Q. And if we can bring up DX-85?

3           A. This shows the fuse being blown with an  
4   electrical pulse.

5           Q. Okay. Can you please explain briefly what, if

1 behavior and users might need to be more savvy about  
2 their use.

3 But again, this could be solved by making a  
4 memory controller a bit more sophisticated and  
5 adaptable and able to deal with mixed-mode parts.

6 Q. Now, I believe the next alternative that you  
7 identified was using pins to set the burst length.

8 And again, in this option I think that you're  
9 referring to using a dedicated pin; is that right?

10 A. Yes.

11 Q. Just for the record, we've brought DX-69 back  
12 up again.

13 Can you please explain, again very briefly, how  
14 use of a -- or how a dedicated pin could be used to  
15 determine burst length?

16 A. This would be similar to the mechanism used to  
17 define different CAS latencies. Rather than storing a  
18 value indicating burst length in a mode register, you  
19 would send the same value over a dedicated pin that  
20 would not change while the system is running or while  
21 the DRAM is operative.

22 So just as the value can be taken out of a mode  
23 register, a DRAM could take the same value off of a pin  
24 and use that to select between different burst length  
25 circuitry.

1           Q. Now, when you were discussing use of a pin, a  
2 dedicated pin, to determine CAS latency, I believe you  
3 described certain attributes, such as DC power,  
4 et cetera.

5                    Would those attributes also apply to the pin  
6 that you'd have in mind to determine burst length?

7           A. Absolutely. The same -- the same conditions  
8 apply.

9           Q. Now, what, if any, would have been the  
10 advantages had JEDEC chosen to use a dedicated pin to  
11 determine burst length rather than using programming  
12 through a mode register?

13          A. Well, again you would eliminate the mode  
14 register and the circuitry required to initialize it,  
15 which would make the part potentially smaller, cheaper  
16 to manufacture, potentially cheaper to test, easier to  
17 design.

18          Q. Now, what, if any, would have been the  
19 disadvantages had JEDEC chosen to use a dedicated pin  
20 to determine burst length rather than programming burst  
21 length through the mode register?

22          A. If there existed a no-connect pin available to  
23 transmit this information, there would be no  
24 disadvantage. If the -- if the specification did not  
25 have enough unused pins, then you would have to add a

1 new pin to the package, and that would increase cost.

2 Q. How significant would the cost increases have  
3 been had it been necessary to add an additional pin?

4 A. Not -- as I said before, not as significant as  
5 adding a data pin because this would be a signal that  
6 would not be changing over -- it would not be changing  
7 dynamically, so it would be a DC value, it would be a  
8 simpler receiver, the pin could be in an undesirable  
9 location on the package, the pad could be in an  
10 undesirable location on the DRAM die, and much simpler  
11 to add this.

12 Q. Now, if we can turn next to the fourth  
13 alternative you've identified, explicitly identify  
14 burst length in the read command, can you please  
15 explain briefly what that means?

16 A. This is similar to the method of identifying  
17 the CAS latency. You would encode the information for  
18 burst length in the read command using the control bus,  
19 redefining the definitions of those pins I mentioned  
20 earlier so that you would transmit several different  
21 read commands to identify several different burst  
22 lengths.

23 Q. And this would use the same five pins that you  
24 identified earlier in connection with CAS latency?

25 A. Yes, it would.

1           Q. Are there sufficient commands available to  
2 permit explicitly identifying both the CAS latency and  
3 the burst length in the read command?

4           A. Yes, there would be.

5           Q. Now, what, if any, would have been the  
6 advantages had JEDEC chosen to identify burst length in  
7 the read command rather than programming it through a  
8 mode register?

9           A. Well, again, you would get rid of the mode  
10 register and therefore the circuitry required to  
11 initialize it, which would make the part simpler to  
12 design and test and potentially cheaper to  
13 manufacture.

14          Q. What, if any, would have been the  
15 disadvantages had JEDEC chosen to identify burst  
16 length in the read command rather than using a  
17 programmable mode register?

18          A. Well, you would increase the complexity of the  
19 decoding logic so that the part would have to recognize  
20 more, more commands.

21          Q. Now, the next alternative that you have  
22 identified is use a burst terminate command. Perhaps  
23 we could start simply by explaining briefly what is a  
24 burst terminate command.

25          A. The way that SDRAMs are defined currently, if

1     you have a long burst, let's say the part is defined to  
2     work with a burst length of 8, it's been programmed to  
3     work with a burst length of 8, and you send a read  
4     command at one instance of time and then follow that up  
5     with another read command four cycles later, the DRAM  
6     is going to implicitly interrupt itself.

7             The first command will only transmit four beats



1           So that if a memory controller only wanted  
2 four pieces of data, four beats of data to return on a  
3 read, it would either send a following read command  
4 four units of time later or it would explicitly  
5 terminate the burst if it had no other pending  
6 requests.

7           Q. Now, the burst terminate command would  
8 originate at the memory controller?

9           A. Yes, it would.

10          Q. And would it be sent to the DRAM via a pin?

11          A. Yes, it would.

12          Q. Now, would this alternative require use of any  
13 additional pins?

14          A. No, it would not because this is already in the  
15 specification.

16          Q. Now, what, if any, would have been the  
17 advantages had JEDEC chosen to use a long fixed burst  
18 length together with a burst terminate command rather  
19 than programmable burst length through the mode  
20 register?

21          A. You would have had a simpler part because you'd  
22 have no mode register, no -- the part would not need to  
23 have to determine -- behave with several different  
24 burst lengths, and so it would be a simpler part to  
25 design and test and manufacture.

1           Q. Now, what, if any, would have been the  
2           disadvantages had JEDEC chosen to use a long burst  
3           length with a burst terminate command rather than  
4           programming burst length through the mode register?

5           A. You potentially could run into inefficiencies  
6           on the bus depending upon how you -- depending upon  
7           how the memory controller handles those situations  
8           where you want to terminate the burst down to 4 from 8.

9           Q. How significant a disadvantage would that have  
10          been?

11          A. I don't believe it would have been very  
12          significant.

13          Q. And then finally you identified use CAS pulse  
14          to control data output. Can you please explain what  
15          you have in mind with that alternative?

16          A. Yes. The way that burst length is defined  
17          currently in the standard, you -- all you need to do is  
18          toggle CAS once to get, for example, four beats of data  
19          back or eight beats of data back, and while data is  
20          coming back on the DRAM bus, the CAS is not toggling.  
21          It's sitting there idle.

22                 Rather than having that scenario, they could  
23          have used CAS to explicitly control the driving of data  
24          onto the bus or the receiving of data off the bus at  
25          the DRAM side. So the memory controller has to

1 four beats of data, then it would toggle CAS four  
2 times; if the memory controller wanted to send or  
3 receive eight beats of data, then it would toggle CAS  
4 eight times.

5 Q. So in other words, the DRAM would return data  
6 only in response to a toggle of the CAS signal?

7 A. Yes. Correct.

8 Q. Now, what, if any, would have been the

1 JUDGE McGUIRE: I think it would be. Let's  
2 take a ten-minute break.

3 Off the record.

4 (Recess)

5 JUDGE McGUIRE: Mr. Oliver, you may proceed.

6 MR. OLIVER: Thank you, Your Honor.

7 BY MR. OLIVER:

8 Q. Professor Jacob, if we could turn next to the  
9 alternatives for dual-edge clocking, and first if I  
10 could ask you to please explain your understanding of  
11 how dual-edge clocking works.

12 A. Yes. Dual-edge clocking is the transmission  
13 and receiving of data on both edges of the clock,  
14 meaning both edges of the clock cause data to be  
15 latched or sent via DRAM to the memory controller and  
16 the same thing at the memory controller side, so rather  
17 than sending or receiving one piece of data per clock  
18 cycle, you're sending two pieces of data per clock  
19 cycle.

20 Q. Let me state for the record that we're showing  
21 DX-86, which is a slide that simply reads "Dual-Edge  
22 Clocking."

23 And Professor Jacob, I believe you have another  
24 demonstrative that we'll call DX-87 that helps explain  
25 dual-edge clocking?

1           A. Yes, I do.

2           Q. DX-87 will be a slide marked Single-Edged  
3 Clocking versus Dual-Edged Clocking?

4           A. Yes.

5           Q. Can you please explain what this slide  
6 indicates?

7           A. Well, this is showing you the difference  
8 between using a single-edged clocking scheme versus a  
9 dual-edged clocking scheme. And in both systems you  
10 have data transmission that's at about the same rate,  
11 but what's shown is that in the top we have a  
12 single-edged clocking scheme, which means that the  
13 clock transitions from low to high at twice the rate of  
14 the data.

15                   The data only goes from low to high, say, once  
16 per cycle, where the cycle is the clock going from high  
17 to low and then back again, so the data can only  
18 transition from zero to one or one to zero once per  
19 clock cycle, whereas the clock goes from zero to one --  
20 makes two transitions, goes from zero to one and one to  
21 zero twice per clock cycle, so the clock is  
22 transitioning at twice the speed of the data.

23                   The advantage here is that you have, as shown  
24 in the middle there, you have two clock edges per data,  
25 per beat of data. You have a clock edge that coincides

1 with the driving of the data and you have a clock edge  
2 that corresponds to the receiving of the data, the  
3 vertical lines showing that one edge of the clock is  
4 synchronous with the edge of the data and one is center  
5 aligned with the data.

6 On the bottom, you've got a dual-edged clocking  
7 scheme so that the clock transitions at the same rate  
8 as the data, so if the data transitions, say, 100 times  
9 per second, let's say a hundred megabits per second,  
10 the clock is going -- is essentially a 50 megahertz  
11 clock, so the difference here is that you only have one  
12 clock edge per beat of data.

13 So instead of having an edge at the beginning  
14 of the data and an edge at the middle of the data, you  
15 only have a clock edge at the beginning of the data in  
16 this example.

17 Q. Now, in your opinion, did JEDEC have available  
18 to it alternatives to dual-edged clocking as that  
19 concept was incorporated in the DDR SDRAM standard?

20 A. Yes, I do.

21 Q. Could you please explain what alternatives to  
22 dual-edged clocking were available to JEDEC.

23 A. Yes. Again it would help me if we have a  
24 demonstrative.

25 Q. Let me just note for the record that this will

1     be DX-88.  It's a slide entitled Alternatives to  
2     Dual-Edged Clocking.

3             Sorry to interrupt.  Could you please explain  
4     the alternatives that you identified.

1 bandwidth, this doubling the clock rate, but you  
2 wouldn't have to double the clock rate. It's a slower



1 Q. Do you regard toggle mode as an alternative to  
2 dual-edged clocking?

3 A. I believe -- I personally believe toggle mode  
4 is a dual-edged clocking scheme, but it is listed here  
5 sort of for completeness because Rambus apparently  
6 believes that toggle mode is distinct from their  
7 implementation of dual-edged clocking, it's not the  
8 same thing as dual-edged clocking, so I've listed it  
9 here as an alternative.

10 Q. If we could focus first on use two or more  
11 interleaved memory banks on-chip, could you please  
12 explain in a little more detail how that would work.

13 A. Yes. Interleaving is a mechanism that has been  
14 around for quite a while, since the '60s, and the idea  
15 is to go back and forth between two banks.

16 Here we go. We have a demonstrative showing  
17 this.

18 The idea is that you go back and forth between  
19 two banks and so you delay the commands sent to the  
20 second bank so that you -- if bank 1 can give you data  
21 every ten nanoseconds, for example, and bank 2 can give  
22 you data every ten nanoseconds, but you delay the  
23 operation of bank 2 by five nanoseconds and you go back  
24 and forth between bank 1, you say read, read, read,  
25 read back and forth, so read to bank 1, read to bank 2,

1 read to bank 1, read to bank 2, every five nanoseconds,  
2 then in effect you're getting data every five  
3 nanoseconds, whereas each bank is only giving you data  
4 every ten nanoseconds, so you are doubling the  
5 bandwidth of the part without having to double the  
6 bandwidth of a single bank.

7 And as this -- the illustration on the left  
8 shows, here's one implementation where on the DRAM chip  
9 you would have two banks and you would send them both  
10 the same clock signal, you would send them both the  
11 same command signal, only to the second bank on the  
12 chip you would insert the delay of half a cycle.

13 Q. Let the record reflect that the witness is  
14 referring to a slide entitled Interleave On-Chip Banks  
15 that will be marked as DX-89.

16 Now, Professor Jacob, there are two separate  
17 diagrams on DX-89. What's represented by the two  
18 separate diagrams?

19 A. Well, the second diagram is another  
20 implementation of essentially the same thing where  
21 your interleaving the banks is also on the DRAM chip,  
22 but the way that you get the delayed clock signal  
23 would be, rather than having the DRAM being  
24 responsible for delaying the clock signal to the  
25 second bank, the memory controller would be

1 responsible for delaying the clock to the second bank,  
2 but what this would require would be two clock signals  
3 sent to the DRAM chip, so this would double the number  
4 of clock signals to the DRAM chip between the memory  
5 controller and the DRAM, so it would be doubled from  
6 one to two. So each bank would have its own separate  
7 clock.

8 Q. Apart from that difference, is there any

9 fundamental distinyyyeelsf

5 fundamental distinyT

1 cycle needs to be very close to 50 percent and your  
2 rise time and fall time of the clock needs to be --  
3 those two need to be very symmetric. They need to be  
4 equal. So you have to have a very, very symmetric  
5 clock signal, a very regular shape, a very even shape.

6           Whereas for a single-edged clocking scheme,  
7 which is what you could use in both of these examples,  
8 for a single-edged clocking scheme, your edge rates,  
9 meaning the rise time and the fall time, need not be  
10 the same and your duty cycle need not be 50 percent.  
11 And you still get, you know, very good behavior.

12           So it's simpler to design a single-edged clock  
13 than it is to design a clock with a dual-edged clocking  
14 scheme.

15           Q. I believe you have another demonstrative that  
16 may help to explain that.

17           A. Oh, okay.

18           Q. If we could bring up the slide entitled Duty  
19 Cycle and Slew Rates.

20           A. Thank you.

21           Q. And we'll label this as DX-90.

22           Now, you referred in your answer to duty  
23 cycle?

24           A. Yes.

25           Q. Can you please explain with reference to DX-90

1 if it helps what you mean by "duty cycle"?

2 A. Yes. The duty cycle represents the proportion  
3 of time that the clock is high versus the proportion of  
4 time that the clock signal is low, so if you have a  
5 duty cycle that is 50 percent, that means the clock  
6 is -- 50 percent of the time it's high, 50 percent of  
7 the time the clock is low.

8 And for a dual-edged clocking scheme, you need  
9 to have something that's very close to 50 percent  
10 because otherwise that means that every other piece of  
11 data is going to have a shorter window and that makes  
12 it harder to design the system.

13 So that's what's shown in the top figure there.  
14 For a dual-edged clocking scheme you have to have the  
15 symmetric duty cycle, you have to have something that's  
16 close to 50 percent, and the slopes that go up and the  
17 slopes that go down need to be rising and falling at  
18 the same time for your system to behave well.

19 Whereas in the bottom figure we're showing the  
20 type of clock that could be used to implement a  
21 single-edged clocking scheme, and notice that the clock  
22 is not nearly as symmetric as the one on top.

23 For example, we're showing here that the rise  
24 time of the clock is relatively fast and the fall time  
25 of the clock is relatively slow. That's perfectly

1 acceptable for a single-edged clocking scheme.

2 And note that it also shows an asymmetric duty  
3 cycle where it's -- the clock period or the clock  
4 signal is high for longer than it is low. That's also  
5 acceptable in a single-edged clocking scheme, whereas,  
6 again, it's -- that type of behavior is much less  
7 desirable if you've got a dual-edged clocking scheme.

8 So the top signal is harder to produce; the  
9 bottom signal is easy to produce.

10 Q. Professor Jacob, you included an awful lot in  
11 that answer.

12 A. Yeah. I'm sorry.

13 Q. I'd like to be certain that we keep the record  
14 clear on this.

15 Your demonstrative DX-90 refers to slew rates.

16 Could you please explain what is meant by "slew  
17 rates."

18 A. Slew rate corresponds to the rise time and the  
19 fall time. That's the slopes of those wires that go up  
20 and down.

21 Q. So in other words, the duty cycle is the amount  
22 of time above 50 percent -- the amount of time high  
23 versus the amount of time low?

24 A. Yes.

25 Q. And the slew rates are the rise slope --

1           A. The rise time and the fall time.

2           Q. The rise time versus the fall time?

3           A. Yes.

4           Q. Now, when you were explaining the potential  
5 advantages of interleaving on-chip banks through use of  
6 a single-edged clock, you made reference to duty cycle  
7 and slew rates.

8                    Could you please explain how the concept of  
9 duty cycle and slew rates that you just explained would  
10 translate into an advantage for interleaving banks  
11 on-chip rather than using a dual-edged clock.

12           A. Yes. In an interleaved scheme you can use the  
13 type of clock that is depicted in the bottom of this  
14 figure. You can have a clock that is -- that has  
15 asymmetric duty cycle and slew rates. It need not be  
16 as clean, pristine, as the clock in the top. You can  
17 have -- you can have asymmetric duty cycles and slew  
18 rates, whereas that type of behavior is not acceptable  
19 in a dual-edged clocking scheme.

20           Q. And why is it an advantage to be able to use  
21 the type of clock illustrated in the bottom portion of  
22 DX-90?

23           A. Because it is much easier to build a clock  
24 generation scheme. It's a far simpler circuit, easier  
25 to build, easier to test, than it is to build a circuit

1 that produces a perfectly symmetric scheme.

2 Q. Now, returning to the alternative of  
3 interleaving on-chip banks, what, if any, would have  
4 been the disadvantages had JEDEC chosen to interleave  
5 banks on a chip rather than using dual-edged clocking?

6 A. I don't think there would have been much of a  
7 disadvantage. You would have to have the delayed clock  
8 and potentially an extra wire if you were going to  
9 transmit two clocks, but -- so perhaps an increase in  
10 the cost.

11 Q. So in other words, with reference to DX-89, if  
12 you were to do the implementation depicted on the  
13 right-hand side, would that might require the extra  
14 clock wire?

15 A. Yes. It would require an extra pin on the DRAM  
16 and an extra wire.

17 And on the left-hand side it would require an  
18 extra delay element on the DRAM.

19 Q. And how significant would those disadvantages  
20 have been?

21 A. Not very.

22 Q. Okay. If we can turn to your next  
23 alternative, if we can go back to the slide DX-88,  
24 which was the slide entitled Alternatives to Dual-Edged  
25 Clocking.





1 pointed to by rank 1 and rank 2, four of those white  
2 boxes, each of those white boxes represent a DRAM chip,  
3 so this would be a module that has four DRAM chips on  
4 it logically partitioned into rank 1 and rank 2, and  
5 you would interleave between rank 1 and rank 2 so that  
6 the same command would be sent to each of those ranks,  
7 but the clock signal would be delayed to rank 2 with  
8 respect to rank 1 so that rank 2 would operate just a  
9 fraction of a second behind rank 1, therefore toggling  
10 back and forth between rank 1 and rank 2 when you were  
11 handling data.

12 And as shown in this picture, the delay  
13 mechanism could be on the module, or as mentioned in  
14 the bottom of the figure, you could have two clock  
15 signals where the delay mechanism is on the memory  
16 controller. That would require an extra connector on  
17 the module and an extra wire connecting the memory  
18 controller to the module.

19 Q. Now, what, if any, would have been the  
20 advantages had JEDEC chosen to interleave on-module  
21 ranks rather than use dual-edged clocking?

22 A. It simplifies the design of the DRAM. You  
23 don't have to move to higher bandwidths coming off the  
24 DRAM itself and you achieve that bandwidth at the  
25 module level instead.

1           Q. And what, if any, would have been the  
2           disadvantages had JEDEC chosen to use interleaving of  
3           on-module ranks rather than dual-edged clocking?

4           A. Well, it pushes the complexity out of the DRAM  
5           onto the shoulders of the module designer so that now  
6           your module, for instance, would have to have an extra  
7           clock line or would have to have that delay element  
8           that's pictured in the figure, so it would complicate  
9           the module slightly.

10          Q. By the way, going back to the advantages of  
11          using interleaving on-module ranks, would this  
12          alternative also permit use of a clock signal that  
13          does not have a close to perfect duty cycle or slew  
14          rate?

15          A. Yes. Yes. This is similar to the interleaving  
16          on-chip banks where you would be able to use one of  
17          those -- a single-edged clocking scheme where you would  
18          not have to have a perfect 50 percent duty cycle and  
19          you would not have to have matching rise times and fall  
20          times and you would not have to have as perfect a clock  
21          signal as you would have to have if you did a  
22          dual-edged clocking scheme.

23          Q. If we could pull back up DX-88, which was the  
24          slide entitled Alternatives to Dual-Edged Clocking.

25                 And if we could turn next to the third of the

1 alternatives that you've identified, increase the  
2 number of pins per DRAM.

3 Can you please explain how increasing the  
4 number of pins per DRAM could increase the speed of  
5 transferred data?

6 A. Yes. The idea of dual-edged clocking is to,  
7 for example, double the bandwidth of the part by  
8 doubling the pin bandwidth, meaning having the data pin  
9 transition at twice the rate previously without having  
10 to increase the speed of the clock.

11 Alternatively, you could get the same bandwidth  
12 out of the part by simply doubling the number of data  
13 pins and going with a single-edged clocking scheme and  
14 you would not have to increase the clock speed at all.  
15 You would also not increase the data pin speed at all.  
16 You would simply increase the number of data pins. You  
17 would achieve the same bandwidth without having to  
18 increase the speed.

19 Q. In order to double the rate of data transfer,  
20 would it be necessary to double the total number of  
21 pins in the DRAM?

22 A. No, it would not.

23 Q. What pins or what number of pins would have to  
24 be increased?

25 A. You would have to -- for example, if you wanted

1 to double the bandwidth of the part, you would have to  
2 double the number of data pins and then you would have  
3 to increase the number of power and ground pins to  
4 support the new data pins that were added.

5 Q. What about command pins?

6 A. No. The number of command pins and address  
7 pins would remain the same.

8 Q. Now, what, if any, would have been the  
9 advantages had JEDEC chosen to increase the number of  
10 pins per DRAM rather than using a dual-edged clock?

11 A. Again, you could retain the use of the  
12 single-edged clocking scheme, which means that you  
13 could use a far simpler clock circuit design. It would  
14 mean that your signals are transitioning at a slower  
15 rate than, for instance, a DDR-type interface, so  
16 rather than having a 200-megabit-per-second data pin,  
17 now you stick with a 100-megabit-per-second data pin,  
18 so the power of the DRAM actually goes down  
19 comparatively.

20 Let's see. That's it.

21 Q. And what, if any, would have been the  
22 disadvantages had JEDEC chosen to increase the number  
23 of pins rather than using a dual-edged clock?

24 A. Well, it would be the cost of increasing the  
25 number of pins, the number of pads and receivers on the

1 DRAM, so it would increase the size of the DRAM die.  
2 It would increase the size of the package and therefore  
3 the cost of the die and the cost of the package. And  
4 it would potentially increase the noise in the DRAM,  
5 but you would have more pins to spread that noise  
6 around, so it would be a net balance.

7 Q. Now, the next alternative that you identify is  
8 increase the number of pins per module. Can you please  
9 explain what that concept is?

10 A. That is the same general idea as the previous  
11 one, except now you push the bandwidth issue out to the  
12 module level so that you don't increase the DRAM's  
13 bandwidth at all, you don't increase the number of pins  
14 on the DRAM, you don't increase the speed of the DRAM,  
15 so you can use the same width of the DRAM as before in  
16 a single-edged clocking scheme, but you have a wider  
17 memory bus between the memory controller and the  
18 module.

19 Q. Now, would this require more DRAMs to be  
20 mounted on the module?

21 A. No, it would not.

22 Q. Now, would this alternative have required any  
23 differences in the design of the DRAMs?

24 A. No, it would not.

25 Q. What, if any, would have been the advantages

1 had JEDEC chosen to increase the number of pins per  
2 module rather than using a dual-edged clock?

3 A. It's a very simple mechanism as far as the DRAM

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1 thing and have 128 bits of data coming off of the  
2 module, and this would require 128 wires on your  
3 motherboard and 128 data pins on your memory  
4 controller.

5 So it would increase the cost of your memory  
6 controller and your motherboard but not necessarily the  
7 cost of the memory module.

8 Q. If we can turn to the next alternative, double  
9 the clock frequency.

10 Now, what do you mean by "double the clock  
11 frequency"?

12 A. That means using a single-edged clocking  
13 scheme and simply doubling that clock, at least for  
14 read commands, and doubling the data bandwidth as  
15 well.

16 Q. Can you explain in a bit more detail how this  
17 alternative would work?

18 A. Yes. It would be similar to a DDR system of  
19 today except that the data strobe, for example, would  
20 run at twice the frequency that it runs at now.

21 Q. This example, would this require any increase  
22 in the speed or frequency of command signals?

23 A. No, it would not. You would still send your  
24 command and addresses at the same rates that you send  
25 them now. The only thing that would change would be



1 the data rate and it would be similar to or, rather --  
2 I'm sorry.

3 The only thing that would change would be the  
4 clock frequency that accompanies your data  
5 transmission. Your data rates would be the same as in  
6 DDR parts of today, but your clock frequency would be  
7 twice what it is.

8 Q. Now, what, if any, would have been the  
9 advantages of running a single-edged clock at twice the  
10 frequency rather than using a dual-edged clock?

11 A. The advantages include the fact that you have  
12 the single-edged clock versus a dual-edged clock,  
13 meaning that the edge rates need not be symmetric, the  
14 duty cycle need not be 50 percent, and it gives you  
15 those extra edges per data packet that are not present  
16 in a dual-edged clocking scheme, you have an edge to  
17 transmit data as well as another edge to receive data,  
18 whereas in a dual-edged clocking scheme you only have  
19 an edge to drive data or you have an edge to receive  
20 data, but you don't have both.

21 Q. Now, what, if any, would have been the  
22 disadvantages had JEDEC chosen to double the frequency  
23 of a single-edged clock rather than using a dual-edged  
24 clock?

25 A. You have a clock signal that is transitioning

1 at twice the rate of present, of present systems, which

1 rate of data transfer.

2 A. Well, there are several reasons why it would be  
3 beneficial.

4 One, it allows you to perform reads and writes  
5 at the same time, simultaneously. In traditional  
6 systems, writes have to wait for reads to finish and  
7 reads have to wait for writes to finish, but here you  
8 can be processing both simultaneously on the bus.

9 It also makes your bus usage more efficient by  
10 allowing you to more naturally pipeline the data. So  
11 if you don't interleave reads and writes on the bus,  
12 you get a very efficient pipelining effect, whereas if  
13 you have to interleave reads and writes, this  
14 introduces dead cycles on the bus where the bus can't  
15 be used for anything. So this would eliminate all  
16 those inefficiencies.

17 And this would also -- this scheme thirdly  
18 would eliminate instances where reads would have to  
19 stall waiting for previous writes, which currently  
20 slows down your reads.

21 Q. Now, what, if any, would have been the  
22 advantages had JEDEC chosen to use simultaneous  
23 bidirectional I/O drivers to increase data transfer  
24 rates rather than dual-edged clocking?

25 A. Well, it would allow you to increase the

1 bandwidth of the system, as I just mentioned, without  
2 having to increase the speed of the system, so this  
3 would not increase the power consumption of the system.  
4 It would not increase the power consumption of the  
5 clock or power dissipation of the clock.

6 Q. What, if any, would have been the  
7 disadvantages had JEDEC chosen to use simultaneous  
8 bidirectional I/O drivers rather than dual-edged  
9 clocking?

10 A. Well, for example, it's a more complex driver  
11 design, so they would have had to use a more complex  
12 mechanism.

13 The other disadvantage is a potential  
14 disadvantage because the benefit that you would receive  
15 from using this is dependent upon your application, so  
16 for instance, if an application never performed any  
17 writes whatsoever and all it ever did was read data, it  
18 would receive no benefit from this at all because,  
19 well, you can't perform writes at the same time a have been t

1 The advantages are limited by your applications, but  
2 most applications have a healthy balance of reads and  
3 writes.

4 Q. And then again, the seventh item is toggle  
5 mode, and just so the record is clear, did you regard  
6 that as an alternative to dual-edged clocking?

7 A. I believe that toggle mode is a dual-edged  
8 clocking scheme and it is included here more for  
9 completeness.

10 Q. If we could turn next then to alternatives to  
11 on-chip PLL and DLL, and if -- actually let me just  
12 mention for the record that we have pulled up the next  
13 demonstrative, which will be DX-92, which is simply a  
14 slide reading "PLL/DLL."

15 Perhaps if I could start by asking you to  
16 please explain the problem of aligning data to the  
17 system clock on a read operation.

18 A. I believe we have a demonstrative.



1 to the fact that signals have to propagate through the  
 2 DRAM chip and be amplified within the DRAM chip, and  
 3 that's represented by the black circuits on the DRAMs  
 4 (indicating).

5 And so by the time that module A or the DRAM  
 6 on module A would be sending the corresponding result  
 7 back to the memory controller, it would be -- actually  
 8 those clocks are meant to be different. I'm sorry.  
 9 Those two black clocks, one labeled "a" and one  
 10 labeled "b", should be swapped. I'm sorry. This  
 11 would be my fault.

12 So there's a delay through the chip so that at  
 13 time quarter after, module A would be sending a result  
 14 back out onto the bus. At time twenty after, module B,  
 15 the DRAM on module B, would be sending the result back  
 16 out onto the data bus.

17 And so the time that the data would arrive at  
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1           So all of these delays introduce timing  
2           uncertainties, and what this means is that you have to  
3           have a relatively wide window of time that you're  
4           looking for the arrival of the data at the memory  
5           controller.

6           And corresponding to the older, slower rates  
7           of speed, this would be, for example, this would  
8           correspond to, let's say, a window of time that would  
9           represent an hour or two hours, and so the fact that  
10          the data would arrive back at the memory controller,  
11          you know, in a fifteen-minute window or ten-minute  
12          window, depending upon which module you're talking  
13          about, that would be insignificant relative to this  
14          two-hour time period or even this one-hour time  
15          period.

16          But as you go to higher rates of speed, now  
17          you're talking about thirty-minute windows and  
18          twenty-minute windows and fifteen-minute windows and  
19          smaller windows of time, and now the difference at  
20          which that window of time that differs depending upon  
21          which module you're talking about, suddenly that window  
22          of time becomes very significant.

23          Q. Now, the various delays that you've described,





1 DDR SDRAM is?

2 A. What that does is it cancels out the  
3 internal -- or it rectifies the internal delays so  
4 that the DRAMs appear to have less of an on-chip  
5 delay.

6 Well, less timing differential. Not less of a  
7 delay. Less of a -- less skew, less differences in  
8 timing.

9 Q. By the way, are you familiar with a  
10 phase-locked loop or a PLL?

11 A. Yes, I am.

12 Q. Can you briefly compare a phase-locked loop or  
13 PLL with a delay-locked loop or DLL?

14 A. They are very similar. The primary difference  
15 is that a PLL contains an oscillator and a DLL  
16 doesn't.

17 Q. Now, in your opinion, is an on-chip PLL or DLL  
18 necessary for high-speed DRAMs?

19 A. No, it is not.

20 Q. Why not?

21 A. Because all that is necessary is that you  
22 cancel out some of these timing uncertainties and there  
23 are numerous mechanisms that can do that just as  
24 effectively as an on-chip PLL or DLL.

25 Q. Now, in your opinion, did JEDEC have available

1 to it other options for canceling out portions of the  
2 delay that you've described at the time that it was  
3 working on what became the DDR SDRAM standard?

4 A. Yes, they did.

5 Q. Can you please identify what some of those  
6 alternatives were?

7 A. Yes. I believe we have a demonstrative that  
8 would list them.

9 Q. If we can pull up the demonstrative entitled  
10 Alternatives to On-Chip PLL/DLL. We'll mark this as  
11 DX-94.

12 A. For example, they -- JEDEC could have decided  
13 to put a DLL on the memory controller.

14 JEDEC could have decided to put a DLL on the  
15 module.

16 They could have used a vernier method to  
17 account for skew, which is a static timing mechanism.  
18 It's not a dynamic one the way a DLL is.

19 They could have achieved a higher bandwidth  
20 using more pins, either at the DRAM level or at the  
21 module level, rather than trying to increase clock  
22 frequency, because as I just showed, the reason that  
23 these problems occurred is because you were trying to  
24 increase your clock frequency and your data frequency,  
25 and so if you can achieve higher bandwidth without

1 increasing your clock and data frequency, then the DLL  
 2 becomes less of an issue.

3           Lastly, you could dispense with the DLL and  
 4 rely upon source synchronous data strobes such as the  
 5 DQS data strobe to provide timing.

6           Q. Okay. If we could look at these one at a time,  
 7 starting with the first one, what do you mean by  
 8 putting the DLL on the memory controller?

9           A. Well, initially, the idea is that you're  
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1           A. For example, you could have two clocks, one  
2           that drives the control, the control information and  
3           the latching of the control data to the DRAMs, and  
4           another that drives the data portion of the interface,  
5           so one that's latching control on addresses and the  
6           other that tells the DRAM to begin driving data out  
7           onto the bus. And the memory controller would maintain  
8           the amount of phase difference between these two clocks  
9           so that for the receipt of data all of it would arrive  
10          in sync.

11          Q. Now, I believe in the previous demonstrative  
12          you had identified outbound delay, internal delay and  
13          return delay.

14                 Which, if any, of those delay elements would  
15          be addressed by placing the DLL on the memory  
16          controller?

17          A. Every single one of them.

18          Q. Now, what, if any, would have been the  
19          advantages had JEDEC chosen to place a DLL on the

1 don't have this PLL or, rather, this DLL that would be  
2 part of the DRAM.

3 It would be a simpler design because it would  
4 not include a DLL and therefore cheaper, take less  
5 time. And it would cancel out more timing uncertainty  
6 than simply putting the DLL out on the DRAM itself, so  
7 you could potentially reach higher rates of speed than  
8 just using an on-chip DLL alone.

9 Q. Now, what, if any, would have been the  
10 disadvantages had JEDEC chosen to place DLL on the  
11 memory controller rather than on the DRAM?

12 A. Well, for example, it could require extra  
13 clocks, as I described, one for the command and one for  
14 the data, which would increase -- potentially increase  
15 the number of pins on the DRAM or the number of pins on  
16 the module and -- or connectors on the module and the  
17 number of wires on the bus.

18 It would increase the design complexity of the  
19 memory controller because now the memory controller  
20 would have a DLL on board or as part of its design, so  
21 the memory controller design would be more complex and  
22 therefore more costly, and you would have potentially  
23 more pads on the memory controller, more pins on the  
24 memory controller package.

25 Q. Now, taking it in totality, how significant

1 would those disadvantages have been?

2 A. Some of them would have been relatively  
3 significant. Well, the advantages would have been  
4 significant, the reduction in power, but then you had  
5 the corresponding increase in power on the memory  
6 controller level. You simplify the design of the  
7 DRAMs, but you increase the design complexity of the  
8 memory controller. I think it would probably balance  
9 out.

10 Q. Now, the second alternative you have listed  
11 here is use off-chip or on-module DLLs. Can you please  
12 explain what you mean by that?

13 A. Yes. The idea is that rather than having the  
14 DRAM decide for itself whether or not it's in sync with  
15 the global system clock, the module would decide  
16 whether or not each DRAM is in sync with the global  
17 system clock.

18 And so you would have a DLL, a single DLL chip  
19 on the module with perhaps one DLL on that chip or  
20 perhaps more than one DLL on that chip, depending upon  
21 what rates of speed you want to reach, but the module  
22 would then decide how in sync with the global system  
23 clock each DLL would be and delay its local concept of  
24 clock.

25 Q. Just to follow up on that one point you just

1 mentioned, you said that you'd have one DLL chip on the  
2 module?

3 A. Yes.

4 Q. But then you said you might have one DLL or you  
5 might have more than one DLL?

6 A. Yes.

7 Q. Can you please explain what you mean by that?

8 A. Yes. Well, in looking at the rates of speed  
9 that they were considering, you would probably need  
10 simply just one DLL to ensure that all DRAMs are in  
11 sync with the system, with the system clock, but if you  
12 envision going to much higher rates of speed, you could  
13 require a separate DLL per DRAM on the module, but  
14 these could be put into the same chip.

15 Q. So in other words, you'd have one chip on the  
16 module that would contain multiple DLLs, one for each  
17 DRAM?

18 A. Yes.

19 Q. Now, with respect to the three sources of delay  
20 that you had mentioned when explaining the problem, the  
21 outbound delay, the internal delay and the return  
22 delay, which, if any, of those sources of delay would  
23 be accounted for by a DLL on the module?

24 A. This would be -- this would account for the  
25 internal delay of the DRAM.



1           Q. Now, what, if any, would have been the  
2 advantages had JEDEC chosen to place DLL -- one or more  
3 DLLs in a single DLL chip on the module as opposed to  
4 placing DLLs in the DRAMs?

5           A. You eliminate the on-chip DLL from the DRAM,  
6 thereby reducing its power consumption, reducing its  
7 cost, reducing the design time.

8           Q. And what, if any, would have been the  
9 disadvantages had JEDEC chosen to place a single DLL  
10 chip containing one or more DLLs on the module as  
11 opposed to placing DLLs on the DRAMs?

12          A. Well, you then move that design complexity onto  
13 a special DLL chip that goes onto the module, so you  
14 would be trading one for the other.

15          Q. Now, the next alternative you have listed is  
16 using a vernier method to account for skew.

17                 Can you please explain first what is a vernier  
18 method?

19          A. A vernier is a delay component that's a very  
20 accurate variable-delay circuit that provides a static  
21 delay to a circuit, but that static delay can be  
22 changed by modifying the vernier circuit dynamically.

23          Q. And then you say "to account for skew." What  
24 did you mean by "skew"?

25          A. Oh, this is what I'm talking about, the timing

1       uncertainty between parts. This is what we were  
2       talking about with the demonstrative showing the  
3       problem. The problem is technically skew. That's the  
4       problem that you're trying to eliminate. The  
5       differences in timing between different things.

6           Q. So in other words, in this context "skew" might  
7       refer to data being out of sync or out of alignment  
8       with the system clock?

9           A. Yes.

10          Q. Can you please explain how a vernier method  
11       might be used to account for skew?

12          A. Yes. For example, you could put a vernier on  
13       each DRAM instead of a DLL on each DRAM and the memory  
14       controller would initialize the system to determine  
15       what the timing of each DRAM was in the system and set  
16       its local vernier so that all of the DRAMs, as far as  
17       the memory controller is concerned, all the DRAMs would  
18       produce data that would arrive at the memory controller  
19       in sync with each other, so it would cancel out the  
20       skew between the DRAMs.

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1           Q. Now, what, if any, would have been the  
2 advantages had JEDEC chosen to use a vernier method to  
3 account for clock skew rather than using on-chip DLLs?

4           A. It's simpler to design than a DLL and it would  
5 cancel out potentially more skew than a DLL so you  
6 could potentially achieve higher data rates using it.  
7 And burn less power.

8           Q. Would that also include the other advantages  
9 you've described of not having the DLL on the chip?

10          A. Yes. Yes. I'm sorry.

11          Q. In other words, the reduction of power,  
12 simplicity, et cetera?

13          A. Yes.

14          Q. Now, what, if any, would have been the  
15 disadvantages of using a vernier method to account for  
16 clock skew?

17          A. Well, by itself, because the mechanism is not  
18 dynamic, as is a DLL, a DLL is continuously updating  
19 its concept of how much to delay the local clock  
20 signal, a vernier mechanism would not be a dynamic  
21 mechanism, and so it would not account for dynamic  
22 changes in skew, so these are, for instance,  
23 fluctuations in temperature of the system and  
24 fluctuations in voltage levels.

25                 So those types of fluctuations would cause



1           A. Yes. The use of the DLL in DDR is there  
2 because you're attempting to achieve high bandwidths by  
3 scaling the frequency of the data bus. And this  
4 alternative is to say let's achieve high bandwidths,  
5 rather than by scaling the speed of the data bus, let's  
6 scale the width of the data bus, either -- for  
7 instance, by having more pins, data pins on the DRAM.

8           Q. Now, is this the same alternative that you had  
9 proposed as an alternative to dual-edged clocking?

10          A. Yes, it is.

11          Q. So in other words, it might have been possible  
12 for JEDEC to use more DRAM pins in order to avoid both  
13 a dual-edged clock and an on-chip DLL?

14          A. Yes.

15          Q. Now, what, if any, would have been the  
16 advantages had JEDEC chosen to use more DRAM pins  
17 rather than placing a DLL on the DRAMs?

18          A. Well, it would be your data rates would be  
19 slower, so you would consume less power on your -- in  
20 your data I/O. It's easier to achieve slower rates of  
21 speed than it is to achieve higher rates of speed, so  
22 it would make your system simpler. You would eliminate  
23 your DLL, so you would eliminate the costs associated  
24 with that as I've described before.

25          Q. If I could follow up on something you just

1 said, you said the data rates would be slower?

2 A. Yes.

3 Q. You're referring to data rates across any  
4 particular wire and any particular pin?

5 A. Yes. Yes. I'm sorry. Across the data pins,  
6 so rather than toggling your data pin at 200 million  
7 times a second, you would toggle the data across any  
8 particular pin at 100 million times a second, but you  
9 would have twice as many pins so that you would have  
10 total bandwidth that's the same, but each pin would  
11 toggle at half the rate.

12 Q. Again, so the record is clear, in terms of  
13 system-wide performance, would the data rate be any  
14 slower?

15 A. The total bandwidth would be the same.

16 Q. And by "bandwidth" you're referring to the --

17 A. The amount of data received per unit of time.

18 Q. Now, you've already described the  
19 disadvantages of using more DRAM pins when you  
20 explained this option in connection with dual-edged  
21 clocking.

22 Are there any other disadvantages that would  
23 arise here other than what you've already described  
24 previously?

25 A. No.

1           Q.   And then finally you list relying on DQS data  
2   strobe to provide timing.

3                   First of all, can you please explain what is a  
4   DQS data strobe?

5           A.   This is a timing signal that accompanies your  
6   data that indicates -- for example, on DRAM writes,

1 different means of measurement?

2 A. Exactly. This provides a different means of  
3 alignment, so the data is aligned with the strobe and  
4 so the recipient of the data would look at the strobe  
5 rather than the system clock.

6 Q. Now, with respect to the three components of  
7 delay that you identified when you explained the  
8 problem, which components, in other words, outbound,  
9 internal and return, which of those components would be  
10 accounted for by relying upon a DQS data strobe to  
11 provide timing?

12 A. Potentially all.

13 Q. Now, what, if any, would be the advantages of  
14 relying on a DQS data strobe to provide timing rather  
15 than using on-chip DLLs?

16 A. Well, you would eliminate your DLL, which would  
17 make your design simpler. It would consume less power.  
18 The design would be smaller, cheaper to manufacture,  
19 and so forth.

20 Q. And what, if any, would be the disadvantages of  
21 relying on the data strobe to provide timing rather  
22 than using an on-chip DLL?

23 A. Well, what this suggests is that you would  
24 not -- that the memory controller would not be relying  
25 upon the global clock for the return data, which would





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A F T E R N O O N    S E S S I O N

(1:30 p.m.)

(DX Exhibit Numbers 62 through 94 were marked for identification.)

JUDGE McGUIRE: This hearing is now in order. At this time you may proceed, Mr. Oliver.

MR. OLIVER: Could we have just one moment, Your Honor?

JUDGE McGUIRE: Sure.

(Pause in the proceedings.)

MR. OLIVER: I apologize, Your Honor. We were short a document and our computer operator went to look for the document. She's not back yet.

JUDGE McGUIRE: Do you want to take a break here, just a short two minutes?

MR. OLIVER: I think if we had just a couple minutes, we could figure it out. I apologize for that.

JUDGE McGUIRE: All right. Go ahead.

(Pause in the proceedings.)

MR. OLIVER: Your Honor, respondent has come to our rescue with copies of the document.

JUDGE McGUIRE: Thanks very much, Mr. Detre.

BY MR. OLIVER:

Q. Good afternoon, Professor Jacob.

1           A. Good afternoon.

2           Q. If we could turn then to the second question  
3 that you were asked, whether reasonable engineers in  
4 the early to mid-1990s would have understood from  
5 Rambus' '898 patent application that Rambus might be  
6 able to obtain patents with claims covering the  
7 technologies in question as proposed for use in JEDEC's  
8 SDRAM and DDR SDRAM standards.

9                   And first, can you please summarize the  
10 conclusion that you reached to this question?

11                   MR. DETRE: Objection, Your Honor.

12                   Just renewing the objection from earlier,  
13 there's been no foundation laid for this witness to  
14 testify about the state of mind of engineers in the

1 through time up to the present have used many different  
2 forms of memory, including asynchronous memory, such as  
3 EDO and fast page mode memory, which were in -- which  
4 were developed in the late 1980s and in use in the  
5 early 1990s.

6 In addition, as I think the testimony will make  
7 clear, what we are doing is looking at the Rambus  
8 '898 application in order to determine the  
9 understanding that can be drawn out of that  
10 application.

11 JUDGE McGUIRE: Overruled. I'll hear the  
12 question.

13 MR. OLIVER: Thank you, Your Honor.

14 BY MR. OLIVER:

15 Q. Professor Jacob, can you please summarize your  
16 conclusion to that second question?

17 A. No, engineers would not have suspected  
18 infringement.

19 Q. Why not?

20 A. Because everything described -- the  
21 technologies described in the '898 application are  
22 either different implementations than the -- we'll  
23 compare these to the technologies in dispute.

24 They're either different implementations or  
25 they were mechanisms that are clearly there in the

1 Rambus application or the Rambus specification to solve  
2 problems that are inherent in Rambus' narrow,  
3 multiplexed, packetized bus structure.

4 MR. OLIVER: Your Honor, may I approach?

5 JUDGE McGUIRE: Yes.

6 BY MR. OLIVER:

7 Q. Professor Jacob, I've handed you a copy of a  
8 document marked CX-1451. This is a copy of Rambus'  
9 original '898 patent application.

10 Is this a document that you reviewed in the  
11 course of your work in this matter?

12 A. Yes, it is.

13 Q. And if we could start, please, with the  
14 so-called description of the invention -- or summary  
15 of the invention -- excuse me -- that appears on  
16 page 9 of CX-1451, internal page 7. That runs through  
17 page 12 and followed by a brief description of the  
18 drawings.

19 Did you review that portion of the application  
20 at the time that you reviewed CX-1451?

21 A. Yes, I did.

22 Q. Can you please give a brief overview of your  
23 understanding of the Rambus invention as described in  
24 CX-1451?

25 A. It is a narrow bus, multiplexed bus, meaning

1 all of the information required to carry on a  
2 transaction is transmitted over the same wires rather  
3 than having separate, dedicated wires to carry the  
4 information. And there are no point-to-point  
5 connections in it. It's -- for instance, there's no  
6 chip-select network.

7 Q. If on page 9 I can direct your attention  
8 underneath Summary of the Invention to the line, which  
9 is apparently I believe in line 16, "and the bus has  
10 substantially fewer bus lines than the number of bits  
11 in a single address."

12 Do you see that?

13 A. Yes, I do.

14 Q. Can you please explain your understanding of  
15 what that means?

16 A. Well the addresses of the day were typically  
17 several dozen. There are several dozen bits in an  
18 address. So for instance, if you had a 32-bit address,  
19 that's a four-gigabyte space.

20 So this is saying that your bus width in this  
21 invention is significantly narrower than a single  
22 address. And if a single address has 24 to 32 bits in  
23 it, then their width of the bus is significantly or,  
24 rather, substantially smaller than that, so this is  
25 what they're talking about, for instance, an eight-bit

1 bus.

2 Q. And how does that compare with the bus used  
3 with a JEDEC-compliant synchronous DRAM?

4 A. These days buses are about 144 bits plus  
5 chip-select information -- well, there's a lot of wires  
6 generally.

7 Q. Now, Professor Jacob, do you have an  
8 understanding of the term "multiplexed" as it would be  
9 applied to a bus architecture?

10 A. Yes, I do.

11 Q. And what does the term "multiplexed" refer to?

12 A. It means at different times different  
13 information, different classes of information, are  
14 transmitted over the same wire.

15 So for example, the main classes of  
16 information would be control information, address  
17 information, and data, and in a multiplexed bus, for  
18 example, if you transmit data and/or address and/or  
19 control over the same wire at different points in  
20 time, then that would be a multiplexed wire, so a bus  
21 is one that transmits the different pieces of  
22 information at different times rather than having a  
23 separate, dedicated set of wires for each class of  
24 information.

25 Q. Now, how, if at all, does the term or does the

1 concept of multiplexing relate to the Rambus invention  
2 as described in this '898 application?

3 A. Could you repeat the question.

4 Q. Yes.

5 How, if at all, is the concept of multiplexing  
6 related to the Rambus invention as it's described in  
7 the '898 application?

8 A. Oh, it's inherent in the design.

9 Q. The concept of multiplexing is inherent in the  
10 Rambus design?

11 A. Yes. Yes. They are using the same bus to  
12 transmit the request to the DRAM that they use to  
13 transmit the data from the DRAM back to the memory  
14 controller, so you're transmitting request information  
15 and data information all in the same set of wires, so  
16 that, by definition, is multiplexed.

17 Q. Now, how, if at all, does the concept of  
18 multiplexing apply to bus architecture in  
19 JEDEC-compliant synchronous DRAMs?

20 A. There's very little multiplexing going on. You  
21 have a separate control bus, you have a separate  
22 address bus, you have a separate data bus, and you have  
23 a separate chip-select bus, so those classes of  
24 information are being passed down their own separate  
25 wires.



1 Q. And Professor Jacob, are you familiar with the  
2 concept of packets?

3 A. Yes, I am.

4 Q. Can you please explain your understanding of  
5 the concept of packets?

6 A. A packet would be when you send a -- well, it's  
7 the term that is used to mean a bundle of information  
8 and the implication is that that bundle is sent over  
9 multiple cycles of time rather than transmitted all at  
10 once, and so if you had a narrow bus, if you have, say,  
11 more information than can be put onto the bus in one  
12 cycle, then that means it takes more than one cycle to  
13 transmit that information. Therefore, what you end up  
14 with is a packetized structure.

15 Q. Now, how, if at all, does the concept of  
16 packets or packetized system relate to the Rambus  
17 invention described in the '898 application?

18 A. Again, it's inherent in the design.

19 Q. In other words, a packetized system is inherent  
20 in the Rambus design as described in the  
21 '898 application?

22 A. Yes, it is.

23 Q. And how, if at all, does the concept of  
24 packets or packetized system relate to JEDEC-compliant  
25 SDRAMs?

1           A. They're not packetized in the same way.

2           Q. Now, based on your review of the  
3 '898 application, CX-1451, did you see a description of  
4 any particular clock system in CX-1451?

5           A. Yes, I did.

6           Q. Can you please explain the clock system that  
7 you saw described in that application?

8           A. Yes. The clock is what has been usually  
9 referred to as a U-shaped clock, meaning that what you  
10 do is you send out on a piece of wire a clock signal,  
11 and it traverses through the system and sends its  
12 signal to every component in the system, and then at  
13 the far end it turns around and comes back, and every  
14 component in the system sees the return signal as  
15 well, so you have an early version of the signal and a  
16 late version of the same signal that are then  
17 propagated to each component in the system, meaning  
18 each DRAM in the system as well as the memory  
19 controller.

20                   And so what they're doing is they're sending on  
21 one wire two logical signals, an early version of a  
22 clock signal and a late version of a clock signal.

23           Q. I believe that you have a demonstrative that  
24 helps to explain this?

25           A. Yes, I do.

1           Q.  And while we're pulling that up, let me state  
2           for the record that we had shown a demonstrative  
3           entitled Second Central Question which would be DX-95,  
4           and the next demonstrative that we'll bring up will be  
5           DX-96.

6                     DX-96 has a caption Rambus Clock  
7           Synchronization, and can you please explain what is  
8           shown in DX-96?

9           A.  Well, this is the picture of that U-shaped --  
10          this is a picture of that U-shaped clock where you  
11          have an outgoing version of the signal and then it  
12          turns around at the far left-hand side -- I'm sorry --  
13          far right-hand side, and it turns around and comes  
14          back.

15                    And so what's happening is you send the clock  
16          pulse -- for example, I've got little clock faces here  
17          to show the arrival of the signal, the time at which a  
18          signal arrives at a given point.

19                    The signal is sent out at noon.  It arrives at  
20          the first DRAM several minutes later.  It arrives at  
21          the second DRAM several minutes later after that.  It  
22          arrives at the third DRAM a little later, and so  
23          forth.  Finally it arrives at the turnaround point of  
24          the U-shaped wire at quarter past and it makes its  
25          return path and connects to each of those DRAMs as a

1 separate signal, so that's why it's called clock 1 and  
2 clock 2.

3 In Rambus' terminology they use both early and  
4 late clocks and clock 1 and clock 2.

5 So this shows the time at which it arrives at  
6 each of those locations as well. Finally, the signal  
7 arrives back at the bus master at half past, and so if  
8 the bus master and each of the DRAMs has a local  
9 circuit that can take the early version of the signal  
10 and the late version of the signal and find a time  
11 average between these two, then they can all synthesize  
12 an internal clock signal that is essentially a  
13 representation of what time it is out at the turnaround  
14 point, meaning quarter past.

15 Q. Now, again just so the record is clear, the  
16 clock signal would be leaving the bus master where it  
17 reads "outbound clock" at the top of the bus master  
18 box?

19 A. Yes.

20 Q. And then it would traverse out to the right,  
21 turn around at the far right and come back to the point  
22 where it reads "inbound clock"; is that right?

23 A. Yes.

24 Q. Now, Professor Jacob, I've directed your  
25 attention specifically to pages 9 through 13 of

1 CX-1451, which is the '898 application.

2 Looking at page 13, there's a caption that  
3 reads "Detailed Description" and then behind that of  
4 course there are many pages that continue.

5 Just in very general terms, what is described  
6 starting at page 13 through the rest of CX-1451?

7 A. This describes the Rambus mechanism, the  
8 details of the system.

9 Q. Let's look if we could, please, at figure 2 of  
10 the application. This appears at page 130 of CX-1451.

11 Now, did you review figure 2 when you were  
12 reviewing the '898 application?

13 A. Yes, I did.

1 Q. And what are the sets of vertical lines?

2 A. Those are each component's connection to the  
3 bus.

4 Q. Now, how, if at all, does the bus illustrated  
5 in figure 2 differ from the bus structure of a  
6 JEDEC-compliant SDRAM?

7 A. It's very different. For one thing, all of the  
8 major components of the bus are bused -- bus  
9 interfaces. They're multidrop interfaces so they're  
10 shared wires, they're shared between all the components  
11 using the system as opposed to having point-to-point  
12 connections.

13 And there's only a small number of bus data  
14 lines. There's eight them, bus data 7, 6, 5, 4, 3, 2,  
15 1 shown along the right-hand side. You have eight bus  
16 data lines, and all the necessary information passes  
17 across those and added valid -- including control  
18 information, address information and data, everything  
19 propagates those few wires as opposed to a JEDEC system  
20 which has lots, lots of wires, an order of magnitude  
21 more.

22 Q. Professor Jacob, are you familiar with the  
23 concept of a chip-select line?

24 A. Yes, I am.

25 Q. What is a chip-select line?

1           A. A chip-select line is an -- it's a wire in  
2 JEDEC architecture, JEDEC memory architecture, that  
3 enables a rank of DRAMs and that identifies a rank of  
4 DRAMs.

5           Q. Now, on figure 2, does that contain a  
6 chip-select line?

7           A. No, it does not.

8           Q. And I believe you mentioned that  
9 JEDEC-compliant SDRAMs do?

10          A. Yes. Yes, they do.

11          Q. In the Rambus architecture, how does that  
12 architecture designate a particular DRAM or a rank of  
13 DRAMs?

14          A. It does it by encoding information in the  
15 packet itself.

16                 So for example, when a packet is sent out by  
17 the CPU or the bus master, every DRAM in the system  
18 needs to decode that packet and determine if the packet  
19 is designated for that particular DRAM or some other  
20 DRAM in the system.

21          Q. If I could ask you to turn within CX-1451 to  
22 pages 20 through 25, please, and again, these are pages  
23 designated in the very lower right-hand corner.

24                 Beginning on page 20, towards the bottom the  
25 caption reads "Bus." Do you see that?

1 A. Yes, I do.

2 Q. And then underneath that, continuing on the  
3 next page, the description of bus followed by a caption  
4 Protocol and Bus Operation?

5 A. Yes.

6 Q. Can you explain just in general terms what is  
7 described in the pages 20 through 25 of CX-1451?

8 A. Yes. This describes the physical organization  
9 of the bus as well as the operation of the bus, its  
10 protocol, the format of the information that's put out  
11 onto that bus.

12 Q. If I could direct your attention in particular  
13 to page 23.

14 And towards the bottom of page 23 there's a  
15 paragraph that begins "Any preferred implementation of  
16 this invention shown in figure 4, a request packet 22,"  
17 et cetera, and then it continues.

18 Do you see that?

19 A. Yes, I do.

20 Q. Now, what is the request packet that is being  
21 referred to there?

22 A. That is the information that's required to  
23 handle particular requests, the information that's sent  
24 to a DRAM to get it to perform a request or a read  
25 request or a write request or something along that.



1           Q. That paragraph references figure 4, so why  
2           don't we turn to figure 4. That appears on page 131 of  
3           CX-1451.

4                    Can you please explain what is depicted in  
5           figure 4 of CX-1451?

6           A. Yes. This is the format of that request  
7           packet.

8           Q. Let me start, if I could, by directing your  
9           attention to the top box and then within that box in  
10          the top there are a number of vertical lines that go  
11          partway down the box just above "access type  
12          master 03."

13                    Do you see those vertical lines                   5          figure 4s

1 top row would be transmitted on the first bus cycle,  
2 the next row would be transmitted on the next bus  
3 cycle, and so forth, so that the packet takes six bus  
4 cycles to transmit.

5 Q. And that was the particular packet illustrated  
6 in figure 4 would take six --

7 A. Yes. That packet would take six cycles, yes.

8 Q. And then could you give us a brief description  
9 of the information that's being transmitted in the six  
10 various clock cycles.

11 A. Yes. Along the top row we have access type and  
12 master. The access type is a four-bit field. It shows  
13 access type 0 through 3. That's what that means,  
14 0 bit, 1, 2, 3. That is information identifying what  
15 type of access it is, for instance, whether it is a  
16 read or a write. And it also identifies whether the  
17 read or write should perform a row activate before a  
18 column read or not. And it ultimately indicates a  
19 latency to use.

20 The other four bits, the master bits, indicate  
21 something about the entity that's driving the request  
22 out onto the bus.

23 Q. And then the rows below that reads address?

24 A. Yes.

25 Q. What does that indicate?

1           A. This indicates that those bits are the --  
2 together several different cycles worth of information  
3 make up a single address, so first -- the first row of  
4 address, address 0 through 8, that indicates that  
5 that's the first nine bits of the address. The next  
6 row is the next nine bits of the address, and so forth.  
7 And finally, in the last row, you have the last four  
8 bits of the address and four bits worth of block size  
9 information.

10           Q. Now, within the address information, that would  
11 contain both the row address and the column address  
12 information?

13           A. Yes, it would.

14           Q. We'll return to block size in a moment.

15                   Now, how, if at all, does the system depicted  
16 in figure 4 differ from the operation of a  
17 JEDEC-compliant SDRAM?

18           A. In a JEDEC-compliant SDRAM, much of the same  
19 information is transmitted, but instead of being  
20 transmitted over multiple cycles over the same sets of  
21 wires, the information in the JEDEC system is  
22 transmitted in one bus cycle over a large number of  
23 dedicated wires.

24           Q. Now, with reference to the '898 application as  
25 a whole, that is, CX-1451 as a whole, does that



1 delineates the block size.

2       A. Okay. So for example, if you have four bits of  
3 data, that can represent any number from 0 to 15, so if  
4 a DRAM sees the number 0 in that bit field in the block  
5 size bit field of the packets, it would take that to  
6 mean that zero bytes were to be transferred.

7               If it saw the value 1, it would think that  
8 there should be one byte transferred, and the same goes  
9 up to 7 and 8.

10               If it sees the value 9 in the block size field,  
11 it takes that to mean that 16 bytes should be

1 the variable block size feature that is depicted here  
2 in pages 29 and 30 of CX-1451 differ from the  
3 implementation of programmable burst length in the  
4 JEDEC-compliant SDRAM?

5 A. In the Rambus mechanism it is a dynamic  
6 mechanism, meaning that this block size information is  
7 carried in the request packet, so it can change from  
8 request to request very easily, very efficiently.

9 In a JEDEC mechanism, the programmable burst  
10 length feature is something that must be programmed by  
11 a special initialization command, so -- and it is  
12 typically used in a JEDEC system such that it's set  
13 once at the system start-up and never changed again, so  
14 the JEDEC mechanism is not dynamic. This mechanism,  
15 the Rambus mechanism, is very dynamic.

16 Q. Well, is the use of the block size feature as  
17 described in the '898 application related in any way to  
18 the narrow bus, multiplexed bus structure?

19 A. Yes. The block size feature as described here  
20 is really -- it's clearly there to solve a scheduling  
21 problem that is inherent in the narrow, packetized bus  
22 structure that Rambus has described.

23 If you have a narrow, multiplexed bus  
24 architecture where the requests are being -- are using  
25 the same set of wires that the data is using, then

1 without a feature such as this where you can very  
2 efficiently change the block size on a  
3 request-by-request basis, it becomes very inefficient  
4 to try to use this in a system where you expect your  
5 data size needs to change.

6 Q. Now, how, if at all, does that differ from the  
7 way in which programmable burst length is used in a  
8 JEDEC-compliant SDRAM?

9 A. In a JEDEC-compliant SDRAM, programmable burst  
10 length is there as a convenience. It is something that  
11 is set once and not changed again, because it's not  
12 necessary for bus scheduling in the JEDEC system  
13 because you have separate buses. Because the control  
14 information uses a totally separate bus from the data  
15 information, you naturally get this -- a very efficient  
16 pipelined nature of data transfer without having to  
17 resort to something like this.

18 Q. Now, in your opinion, would an engineer reading  
19 the '898 application, CX-1451, in the early to  
20 mid-1990s have thought that Rambus could obtain patent  
21 rights over the programmable burst length feature as it  
22 was used in the JEDEC SDRAM standard?

23 A. No, they would not.

24 Q. Why not?

2523 A.3m t - not? cb - ntata teuta p dare as

1 solve the problems that are inherent in the narrow,  
2 multiplexed bus architecture. It's inherently tied to  
3 that narrow, multiplexed bus architecture.

4 Q. Let me ask you to turn next, please, to  
5 pages 16 and 17 of CX-1451.

6 And if I could direct your attention in  
7 particular on page 16 to the bottom paragraph appearing  
8 on that page.

9 You'll see that there's a reference to  
10 access-time registers on that page?

11 A. Yes, I do.

12 Q. Can you please explain the concept of access  
13 time as used in Rambus' '898 application?

14 A. Access time refers to the transpiring of time  
15 between a -- the receiving of a request and the  
16 response to that request, so it's a delay between  
17 receiving a request and, for instance, driving the  
18 corresponding data out onto the bus.

19 Q. If I could then ask you to turn, please, to  
20 page 29 of CX-1451.

21 And I'd like to direct your attention to the  
22 table appearing at the top of page 29, please.

23 And one of the columns of the table in the  
24 right-hand side reads "Access Time."

25 Do you see that?



1           A.  Yes, I do.

2           Q.  Now, could you please explain what is being  
3 depicted in this table with particular reference to  
4 access time.

5           A.  Well, this is showing the relationship between  
6 those access-time registers and the concept of access  
7 time as well as the bits in the request packet that are  
8 called access type.  Remember, the first four bits of  
9 each packet are called this access type value.

10           So depending upon what value you see in that  
11 access type field in the request packet, this causes  
12 the -- and so that's corresponding to the first column  
13 in the table.  Depending upon the value that you see in  
14 that field, the DRAM -- or depending upon what value  
15 the DRAM sees in that field, the DRAM would then use an  
16 access time corresponding to the value held in one of  
17 these access registers, and that's shown in the far  
18 right column.

19           So for example, if the DRAM sees the value 6 or  
20 7 in the access type field, it would use access  
21 register 3 to determine its latency.  If it sees the  
22 value 4 or 5, it would use access register 2 to  
23 determine its access time.  And in the middle column it  
24 tells you what type of DRAM access would be then  
25 performed, whether it's a column read only or a row

1 activate and a column read.

2 Q. Now, how, if at all, does the implementation of  
3 the access-time register described in the  
4 '898 application differ from programmable CAS latency  
5 as implemented in JEDEC-compliant SDRAMs?

6 A. It differs in that it's a very dynamic  
7 mechanism. The fact that you can choose between  
8 multiple access times by setting different values in  
9 your request packet enables you to dynamically change  
10 the latency of each request on a request-by-request  
11 basis and do so very efficiently, whereas in the JEDEC  
12 mechanism you have to change the programmable CAS  
13 latency value through a special initialization or a  
14 special command that takes extra time and you can't  
15 change it on a request-by-request basis without going  
16 through that special command.

17 So in JEDEC-compliant systems you program that  
18 feature once at start-up and never change it again,  
19 whereas in the Rambus mechanism the fact that you can  
20 select different latencies based on bits in the request  
21 packet enables a far more dynamic system.

22 Q. Now, based on your review of the  
23 '898 application, how, if at all, is the  
24 implementation of the access-time register that you've  
25 described related to the narrow bus or packetized



1 programmable CAS latency as that feature was used in  
2 the JEDEC SDRAM standard?

3 A. No, they would not.

4 Q. Why not?

5 A. Because this is clearly there to solve -- it's  
6 clearly in the Rambus mechanism to solve scheduling  
7 problems that are inherent in the narrow, multiplexed

1 clock 1. And when it gets to the end of the wire on  
2 the left-hand side, it turns around and comes back.

3 And note that each chip has two connections to  
4 that one wire, so each chip gets two logical clock  
5 signals. It gets clock 1, which is the early version  
6 of the clock, and it gets clock 2, which is the late  
7 version of the clock.

8 Q. Again, just to be certain the description is  
9 clear, how many actual clock wires are there in the  
10 bus?

11 A. There is one clock wire and that one clock wire  
12 carries two logical signals.

13 Q. And again, to be certain the record is clear,  
14 the outbound signal would be on the top horizontal wire  
15 in figure 8a?

16 A. Yes.

17 Q. And that would loop around the left-hand side  
18 and come back in the lower horizontal line in  
19 figure 8a?

20 A. Yes. Labeled "clock 2." Yes.

21 Q. Now, does this correspond to the demonstrative  
22 that you explained a moment ago with the outbound clock  
23 and the inbound clock?

24 A. Yes. Absolutely.

25 Q. If we could next turn to page 148 of CX-1451.



1 A. No, its does not.

2 Q. Does figure 12 show a DLL?

3 A. No, it does not.

4 Q. How does the circuit depicted in figure 12  
5 differ from a DLL circuit as it would appear in a  
6 DDR SDRAM?

7 A. Actually I have a demonstrative that would  
8 illustrate that.

9 Q. If we could pull up the next demonstrative,  
10 please, I believe that will be DX-97.

11 This is a slide with the title Rambus' Delay  
12 Circuit versus a DLL.

13 Professor Jacob, perhaps you could explain  
14 using DX-97 how the circuit depicted in figure 12 of  
15 Rambus' '898 application differs from a delay-locked  
16 loop circuit.

17 A. Well, as I said, Rambus' delay circuit takes an  
18 early clock and a late clock and finds the time average  
19 between the two, and a delay-locked loop takes two  
20 signals as input and delays one so that it becomes in  
21 sync with the other. They perform very different  
22 functions.

23 And as this demonstrative shows, the circuits  
24 are very different. One is not equal to the other.

25 The one on the right is a typical delay-locked

1 loop implementation. I pulled that out of Dally and  
2 Poulton's book on high-speed circuits.

3 And the figure on the left is Rambus' figure 12  
4 from their '898 application.

5 Q. Now, how, if at all, does the function of the  
6 circuit depicted in figure 12 of Rambus'  
7 '898 application differ from the function of a DLL in a  
8 DDR SDRAM?

9 A. It -- they don't have the same function at  
10 all.

11 The circuit depicted in the figure on the left  
12 takes two clocks and finds the time average -- takes  
13 two clock signals and finds the time average between  
14 them.

15 The figure on the right delays the top signal,  
16 which is labeled "ref. clock e "ref. clo7msr1tMTe fusc8 signa



1 '898 application ever refer to a PLL or a phase-locked  
2 loop?

3 A. No, it does not.

4 Q. Does the '898 application ever refer to a DLL  
5 or a delay-locked loop?

6 A. No, it does not.

7 Q. In your opinion, would an engineer reading the  
8 '898 application during the mid to late 1990s have  
9 understood that Rambus might claim patent rights to  
10 on-chip DLL as it was used in the JEDEC DDR SDRAM  
11 standard?

12 A. No, they would not.

13 Q. Why not?

14 A. Thoroughly different implementation, different  
15 circuit, different function. They are nothing alike.

16 Q. If I could ask you to turn, please, to page 149  
17 of CX-1451. And I'd like to direct your attention to  
18 figure 13 appearing at the top of the page.

19 And again, did you review figure 13 at the time  
20 you reviewed the entire '898 application?

21 A. Yes, I did.

22 Q. Can you please explain what is depicted in  
23 figure 13 at page 149 of CX-1451?

24 A. Yes. This is a timing diagram showing the time  
25 at which certain events happen.



1 Q. The data signals you referred to, that would be  
2 127 and 125?

3 A. Yes. Yes.

4 Q. Now, in figure 13, is the data latched in time  
5 with either of the external clock signals?

6 A. No, it is not.

7 Q. With what clock signal is the data latched  
8 with?

9 A. It is latched in sync with no external signal  
10 in the system. It's latched out of phase with respect  
11 to the external clock. And moreover, each DRAM in the  
12 system will bear a different phase relationship between  
13 that clock signal and when the data is latched, the  
14 latched --

15 Q. So in other words, it's latched only in phase  
16 with the internal clock?

17 A. Yes.

18 Q. And the internal clock is out of phase with  
19 each of the external clock signals?

20 A. Yes, it is.

21 Q. Now, how, if at all, does the implementation of  
22 the clocking scheme as described in the  
23 '898 application differ from the implementation of the  
24 dual-edged clocking scheme in JEDEC's DDR SDRAM  
25 standard?

1           A. Well, for one thing, the JEDEC DDR clocking  
2 scheme, as opposed to the Rambus clocking scheme which  
3 uses one wire to transmit two logical clock signals,  
4 the JEDEC DDR standard uses two wires to transmit one  
5 logical clock signal. That's the definition of the  
6 differential signal.

7           In addition, the data in DDR is latched in sync  
8 with the external clock and for each DRAM in the  
9 system, each DRAM bears the same phase relationship  
10 between the external clock and when the data is  
11 latched, as opposed to Rambus where it's latched out of  
12 phase with the external bus clock and each DRAM bears a  
13 different phase relationship between when the data is  
14 latched and the external signal.

15          Q. Now, in your opinion, would an engineer  
16 reading the '898 patent application during the 1990s  
17 have thought that Rambus could obtain patent rights  
18 over the dual-edged clocking feature as it was  
19 proposed for use or used in the JEDEC DDR SDRAM  
20 standard?

21          A. No.

22          Q. Can you please explain why?

23          A. Because they're different implementations.

24          Q. Next, Professor Jacob, I'd like to consider the  
25 claims contained in Rambus' '898 application.

1           Have you reviewed the original 150 claims of  
2           the '898 application?

3           A.   Yes, I have.

4           Q.   In your opinion, would any of those claims  
5           have alerted an engineer in the 1990s that Rambus  
6           might seek to obtain patent rights over features  
7           proposed for use or used in the JEDEC SDRAM or  
8           DDR SDRAM standards?

9           A.   No.

10          Q.   Why not?

11          A.   Because all of the claims deal with -- or each  
12          of the claims either deals with Rambus' clocking  
13          mechanism, which was different from JEDEC's clocking  
14          mechanism, or the claim deals with Rambus' packaging  
15          techniques, which are different from the packaging  
16          techniques that JEDEC was dealing with, or the claim is  
17          explicitly limited to the narrow, multiplexed,  
18          packetized bus structure, which was unlike the bus  
19          organization considered by JEDEC.

20          Q.   I'd like to take a look at three claims and to  
21          help illustrate what you just said.

22                 If I could ask you to turn, please, first to  
23          page 64, looking at claim number 1.

24                 Do you have that in front of you?

25          A.   Yes, I do.

1           Q. Now, what, if anything, in claim number 1  
2 indicates to you that this claim would not apply  
3 outside of the specific Rambus architecture?

4           A. Well, for instance, the last two clauses said  
5 "bus containing substantially fewer bus lines than the  
6 number of bits in a single address" and "said bus  
7 carrying device-select information without the need for  
8 separate device-select lines connected directly to  
9 individual memory devices."

10           Both of these are very different from the  
11 memory bus architectures of the day, the DRAM bus  
12 architectures of the day.

13           Q. Looking at the first clause you identified,  
14 said bus containing substantially fewer bus lines than  
15 the number of bits in a single address, what about that  
16 clause indicates it will be different from the way that  
17 JEDEC implemented its SDRAM standard?

18           A. The way JEDEC implemented its DRAM standard was  
19 similar to the way DRAMs had been -- DRAM interfaces  
20 had been orchestrated, used, had substantially more bus  
21 lines than the number of bits in a single address. In  
22 a typical memory bus architecture.

23           Q. Now, looking at the second of the two clauses  
24 that you identified, said bus carrying device-select  
25 information without the need for separate

1 device-select lines connected directly to the  
2 individual memory devices, again, what is it about  
3 that clause that would serve to distinguish this claim  
4 from the way in which JEDEC implemented its SDRAM  
5 standard?

6 A. Well, JEDEC-compliant DRAM organizations did  
7 have a need for a separate device-select line  
8 connected directly to each individual memory device.  
9 That was the way things had been built and this is the  
10 way JEDEC continues to build their memory systems, so  
11 this is very different from the way things have been  
12 done.

13 Q. Would that device-select line be the  
14 chip-select line you referred to earlier?

15 A. Exactly. That would be the chip-select line  
16 that I referred to.

17 Q. Let me ask if you could, please, to turn to  
18 claim number 73. I believe it appears at page 89 of  
19 CX-1451.

20 It actually begins on page 89 and carries over  
21 to the top three lines of page 90.

22 Now, what, if anything, about claim 73  
23 indicates to you that this claim would not relate to  
24 the JEDEC SDRAM standard?

25 A. This describes the Rambus clocking scheme that

1 generates an early version of the clock signal as well  
2 as a late version of the clock signal.

3 Q. I assume from what you're saying that is then  
4 different from the JEDEC --

5 A. I'm sorry. Yes. This is very different from  
6 the clocking scheme that was considered by JEDEC,  
7 where you don't consider early and late versions of  
8 the clock signal; you just have one, one logical  
9 signal.

10 Q. And I asked you specifically about JEDEC's  
11 SDRAM standard.

12 A. Yes.

13 Q. Is there anything about claim 73 that would  
14 serve to indicate that it would not apply to the JEDEC  
15 DDR SDRAM standard?

16 A. The same, the same is true. The SDRAM and  
17 DDR SDRAM both use a single logical clock signal, not  
18 this dual local clock signal with early and late  
19 signals that are described, for instance, in the  
20 second, third and fourth elements of this claim. This  
21 is nothing like what was used in SDRAM or DDR SDRAM.

22 Q. If I could then ask you to turn, please, to  
23 claim number 91, which I believe appears at page 99.

24 Now, what, if anything, in claim 91 indicates  
25 to you that this claim would not apply outside of the



1 particular Rambus architecture?

2 A. So this describes Rambus' packaging scheme  
3 which was to place the connectors of a DRAM only on  
4 one edge of the DRAM chip as shown, for example, in  
5 the last two lines or the last three lines of the  
6 claim, talking about the connections are placed along  
7 a single side of the package, and this is very unlike  
8 the DRAM packages of the day which used both sides of  
9 the package. They used, you know, more than one edge  
10 of the package to connect to the rest of the system.

11 MR. OLIVER: May I approach, Your Honor?

12 JUDGE McGUIRE: Yes.

13 BY MR. OLIVER:

14 Q. Professor Jacob, I've handed you a document  
15 marked as CX-1460. I'll give you just a moment to look  
16 at it.

17 (Pause in the proceedings.)

18 A. All right.

19 Q. CX-1460 is a copy of the Rambus patent  
20 number 5,243,703 issued September 7, 1993.

21 Professor Jacob, did you review Rambus'  
22 '703 patent in connection with your work in this case?

23 A. Yes, I did.

24 Q. In your opinion, would Rambus' '703 patent have  
25 alerted an engineer during the 1990s that Rambus might

1 seek to obtain patent rights over features contained in  
2 the JEDEC SDRAM or DDR SDRAM standards?

3 A. No, it would not.

4 Q. Why not?

5 A. Because this patent deals with the U-shaped  
6 clock or the reflected clock. It's a -- it deals with  
7 schemes using two logical clock signals, an early  
8 version of the signal and a late version of the signal,  
9 finding the time average between the two.

10 Q. If I could ask you to turn to page number 24,  
11 please, in CX-1460.

12 And I'd like to direct your attention to claim  
13 number 1, starting a third of the way down the  
14 left-hand column on page 24 and continuing onto the  
15 right-hand column.

16 And can you please explain what it is about  
17 this claim number 1 that indicates to you that the  
18 claim was limited to the particular Rambus clocking  
19 scheme?

20 A. Well, the claim deals with what I was talking  
21 about, a clock system that delivers an early version of  
22 a signal and a late version of a signal, and the reason  
23 that you can determine this is because it talks about  
24 path length matching between clock 1 and clock 2 and a  
25 turnaround point.

1           For example, lines -- somewhere around line 38  
2           or -- we'll start at line 35 in the first column,  
3           wherein the first clock signal generation means is  
4           coupled at, one, a first point of the transmission line  
5           means for receiving the clock signal, the global clock  
6           signal, and two, a second point of the transmission  
7           line means for receiving the global clock signal  
8           wherein the first point is between the first end and  
9           the midpoint, wherein the second point is between the  
10          midpoint and the second, they're talking about the path  
11          length matching things so that the reflection time for  
12          the first -- for the first clock and the second clock,  
13          they're equal, their transmission to the midpoint are  
14          equal so that you can have a nice midpoint between the  
15          two so that every chip in the system has the same time  
16          average.

17                 And you know, you get the same sort of language  
18                 at the end of the claim that talks about synchronizing  
19                 between these two.

20                 Q.   And that describes the U-shaped, the loop clock  
21                 that you had described earlier?

22                 A.   Yes.   Exactly.

23                 Q.   Now, within the '703 patent there's the  
24                 so-called specification, which is the language  
25                 appearing before you reach the actual claims.

1           Is there any -- based on your review of that  
2 part of the patent, is there anything in that portion  
3 of the patent that differed in any substantial way from  
4 the description you mentioned provided in the  
5 '898 application?

6           A. Nothing that I noted. It seemed to be  
7 substantially the same as what was in the  
8 '898 application.

9           Q. Was there then anything in the specification  
10 portion of the '703 patent that would have alerted an  
11 engineer during the 1990s that Rambus might be able to  
12 obtain patent rights over features contained in JEDEC  
13 SDRAM or DDR SDRAM standards?

14          A. No.

15           MR. OLIVER: May I approach?

16           JUDGE McGUIRE: You may.

17           BY MR. OLIVER:

18          Q. Professor Jacob, I've handed you a document  
19 marked CX-887. It's a two-page document. The first  
20 page is a letter to Mr. Ken McGhee of Electronic  
21 Industries Association, dated June 17, 1996, from  
22 Mr. Richard Crisp. And the second page is also dated  
23 June 17, 1996, with a caption Rambus U.S. and Foreign  
24 Patents, followed by a list of numbers.

25           Professor Jacob, did you review CX-887 in

1 connection with your work on this case?

2 A. Yes, I did.

3 Q. And did you review the various patents that are  
4 listed on page 2 of CX-887?

5 A. Yes, I did.

6 Q. Now, in your opinion, would the patents listed  
7 in the attachment to the letter that is on page 2 of  
8 CX-887 have alerted an engineer in the 1990s that  
9 Rambus might be able to obtain patent rights over  
10 features incorporated in the JEDEC SDRAM or DDR SDRAM  
11 standards?

12 A. No.

13 Q. Why not?

14 A. Because in each of the cases the patents fall  
15 under one of several different categories. They  
16 either are restricted to the -- explicitly restricted  
17 to the narrow, packetized, multiplexed bus  
18 organization, or they contain -- or deal with the  
19 topic that lies outside of the scope of JEDEC 42.3, or  
20 they are describing material that could have related  
21 to or could have been within the scope of JEDEC 42.3  
22 but cover minor implementation details that JEDEC did  
23 not consider in the definition of the standard.

24 Q. Professor Jacob, I'd like to turn now to the  
25 third of the four questions that you addressed, and

1 that's the question of whether Rambus had issued  
2 patents or pending patent applications before June of  
3 1996 that contained claims that a reasonable engineer  
4 would believe covered the four technologies at issue in  
5 this case.

6 Now, Professor Jacob, have you reviewed the  
7 claims of any patent applications that Rambus  
8 submitted to the Patent and Trademark Office before  
9 June of 1996?

10 A. Yes, I have.

11 Q. And have you reached a conclusion as to  
12 whether any of those claims would or might be  
13 considered to cover the technologies at issue in this  
14 case?

15 A. Yes.

16 Q. Could you summarize very briefly what your  
17 conclusion is.

18 A. That there do exist patent claims that cover  
19 each of the technologies in dispute.

20 Q. By the way, I should note for the record that  
21 we have pulled up another demonstrative slide,  
22 entitled Third Central Question. I believe that would  
23 be DX-98.

24 JUDGE McGUIRE: Mr. Oliver, can I get some hard  
25 copies of these screens, these demonstratives, at some

1 point?

2 MR. OLIVER: Yes. Absolutely, Your Honor. I  
3 don't know if we'll have a set for you by today but  
4 certainly by tomorrow morning.

5 JUDGE McGUIRE: That's fine.

6 BY MR. OLIVER:

7 Q. Professor Jacob, let's start with programmable  
8 CAS latency.

9 Have you formed any opinions as to whether an  
10 engineer could reasonably construe any of the claims

11 that you reviewed to cover programmable Have youMCS6 cs 0  
Add look's also 1 ewe30 0 0 scnburstS lngth,ttely, Your Honor. I1

Add briefwe'lw 1 so y havou clusuldlutely 3.03 MR. OLIVER:

1           A. That one could -- yes, an engineer could  
2           construe that claims did cover programmable burst  
3           length as was discussed in JEDEC 42.3.

4           MR. OLIVER: Your Honor, if we could have just  
5           a moment to set up an easel in order to -- in a moment  
6           or two we want to set up a couple of demonstratives on  
7           the easel.

8           JUDGE McGUIRE: Take a few moments.

9           We'll just go off the record for two minutes.  
10          If you want to get up and stretch, go ahead.

11          (Recess)

12          JUDGE McGUIRE: Mr. Detre.

13          MR. DETRE: Your Honor, before Mr. Oliver  
14          begins this line of questioning, it looks to me like  
15          he's about to get into programmable CAS latency,  
16          purported programmable CAS latency claims which are,  
17          according to the demonstratives they shared with us,  
18          are the same ones that Mr. Nussbaum testified about.

19          In other cases, the FTC has always taken a  
20          position that there should be one expert per topic.  
21          This is cumulative, Your Honor, and I don't think we  
22          should hear it again.

23          JUDGE McGUIRE: Mr. Oliver?

24          MR. OLIVER: We're simply presenting two  
25          points. First of all, we're merely presenting it from



1 a different point of view, from a technical expert as  
2 opposed to a patent expert, depending on whether either  
3 you or the commission wishes to attach more weight to a  
4 patent expert or more weight to a technical expert.  
5 It's not cumulative because it's coming from an  
6 additional point of view.

7 In addition, I believe that Professor Jacob may  
8 have additional information and understanding with  
9 respect to certain aspects of the technology that may  
10 bear upon his testimony.

11 JUDGE McGUIRE: Overruled.

12 MR. OLIVER: May I approach, Your Honor?

13 JUDGE McGUIRE: Yes.

14 BY MR. OLIVER:

15 Q. Professor Jacob, I've handed you a document  
16 marked CX-1504, which is a prosecution history of a  
17 Rambus patent, and I'd like to ask you to turn in  
18 particular to page 216 of CX-1504.

19 A. Okay.

20 Q. And beginning on page 216 is a portion of this  
21 prosecution history that consists of an amendment at  
22 the top captioned In The United States Patent and  
23 Trademark Office. In the box on the right-hand side is  
24 a date, January 6, 1995. The left-hand side indicates  
25 the serial number 07/847,961.

1                   Professor Jacob, did you read this amendment to  
2           the '961 patent application in the course of your work  
3           in this matter?

1

JUDGE McGUIRE: Okay. Go ahead.

1 referring to page 1 of DX-99?

2 A. Yes.

3 Q. And Professor Jacob, we have also placed a copy  
4 of a page from release 4 of the JEDEC SDRAM standard on  
5 the easel, and if it is helpful for you to do so,  
6 please feel free to approach that, and if you wish to  
7 mark up or make any marks on the blowup, please feel  
8 free to do so. I have a marker here that I believe  
9 will work. The ones next to you probably don't work,  
10 but I think this one here should work.

11 A. Okay. Great. Thanks.

12 Q. And with those materials, please make use of  
13 any of those materials you find helpful, but can you  
14 please explain your conclusion as to why you believe  
15 that a reasonable engineer could construe claim 160 of  
16 the amendment to the '961 application as potentially  
17 covering a CAS latency feature as proposed for use in  
18 the JEDEC SDRAM standard?

19 A. All right. Well, let's go through this element  
20 by element.

21 So element 1 describes a memory storage system  
22 including a bus and a semiconductor device, and this is  
23 clearly the work of JEDEC 42.3 that describes or  
24 defines specifications for semiconductor devices and

1 example, up here on page 134 of JX-56.

2 Element 2 reads "having that is configurable  
3 by a device external to the semiconductor device," and  
4 I'm reading that as if the word "that" is a typo.  
5 "That" should be eliminated so that the phrase would  
6 read a semiconductor device that is configurable by a  
7 device.

8 So element 2 describes a -- the fact that the  
9 semiconductor device is configurable by an external  
10 device and in comparison to JEDEC work is the  
11 configuration information that's provided to the SDRAM  
12 by the bus controller, and the type of information  
13 that's provided to initialize the DRAM to configure it  
14 is described in JX-56 at, for example, pages 114, 115  
15 and 116.

16 Element 3 describes a -- the fact that the  
17 semiconductor must have at least one pin to couple the  
18 semiconductor to the bus, and for example, pinouts can  
19 be found within the JEDEC specification, for example,  
20 page 106 of JX-56.

21 Element 4 describes a register operative to  
22 store information within the semiconductor device.

23 And for example, up in the diagram on the easel  
24 or the illustration up on the easel we have pictured  
25 the SDRAM mode register. That is a register within the



1 pin.

2 So that clearly specifies a manner in which the  
3 DRAM is to respond to transaction requests.

4 Element 6 describes the fact that the --  
5 describes how the information is received by the  
6 semiconductor device, so it says that the information  
7 is received when the semiconductor device is  
8 configured and the semiconductor device stores that  
9 information that is received from the bus lines into  
10 the register.

11 And for instance, in the JEDEC spec, JX-56,  
12 pages 14 -- 114, 115 and 116, the power-on  
13 configuration sequence is described wherein the memory  
14 controller puts information out onto the bus. That  
15 information is grabbed directly off of the bus by the  
16 DRAM device and that information is put directly into  
17 that SDRAM mode register. And that's all described  
18 within the spec.

19 So there's clearly a relationship there.

20 And element 7 is sort of a restatement of  
21 element 5. It says thereafter the semiconductor -- or  
22 thereafter responds to transaction requests in the  
23 manner specified by the information in a mode  
24 register.

25 So for example, we'll return to the burst

1 length example. As shown in the SDRAM mode register,  
2 you have a burst length value that can change the way  
3 that the DRAM part responds to a read request or a  
4 write request.

5 JUDGE McGUIRE: All right. Just so I'm clear,  
6 I want to inquire here. What is meant in this column 2  
7 when it says "JEDEC Work"? What exactly does that term  
8 imply?

9 THE WITNESS: In column 2?

10 JUDGE McGUIRE: DX-99, at the top of the page  
11 there. It seems sort of broad. I'm trying to get an  
12 understanding of what that entails.

13 THE WITNESS: Oh, what this is meant to show  
14 is a comparison between the claim language in claims  
15 that were outstanding at the time that Rambus was a  
16 member of JEDEC to work that was going on within the  
17 JEDEC 42.3 subcommittee while Rambus was there, so  
18 this points to specific instances of things that were  
19 happening at the time that Rambus was a member of  
20 42.3.

21 JUDGE McGUIRE: Okay. Go ahead, Mr. Oliver.

22 MR. OLIVER: Thank you, Your Honor.

23 Your Honor, could I invite Professor Jacob to  
24 mark on the demonstrative any particular elements that  
25 he was referring to?



1 JUDGE MCGUIRE: He may approach.

2 BY MR. OLIVER:

3 Q. Professor Jacob, could I ask you to use this  
4 pen to mark on the demonstrative the mode register that  
5 you've referred to.

6 A. (Witness complies.)

7 Q. And Professor Jacob, can you mark the  
8 particular portion of the mode register that you  
9 referred to that would determine the burst length?

10 A. (Witness complies.)

11 These are simply two different representations  
12 of the same register, whereas this simply says that  
13 this is reserved to test mode. This bit is not one  
14 that's for test mode (indicating).

15 These are both the mode register. The only  
16 difference is that when this bit is a 1, it's in test  
17 mode.

18 So the bottom three bits correspond to the  
19 burst length information. This box right here  
20 indicates for the eight different values that these  
21 three bits can represent, these three bits can  
22 represent numbers between and including 0 to 7. For  
23 the eight different possibilities that can be held  
24 here, how the DRAM should respond (indicating).

25 So there are eight different things that the

1 DRAM could possibly do.

2 Q. Would you please label the two circles you've  
3 just drawn as relating to burst length.

4 A. Yes.

5 (Witness complies.)

6 Q. And Professor Jacob, while you're there, could  
7 you also mark on that demonstrative which portion, if  
8 any, of the mode register would relate to CAS latency.

9 A. (Witness complies.)

10 The three bits that are labeled "LTMODE" within  
11 the mode register, those bits hold CAS latency  
12 information (indicating).

13 And this is tied to the bottom-most box down  
14 here that shows for the eight different values that  
15 could be held in LTMODE how the DRAM should respond to  
16 requests.

17 So clearly different values of LTMODE  
18 correspond to different behaviors caused by the --  
19 caused -- different behaviors that the DRAM would  
20 have.

21 Q. Let the record reflect that the witness is  
22 pointing to a box labeled "latency mode" towards the  
23 bottom of the demonstrative.

24 Your Honor, could we mark this demonstrative as  
25 DX-100?

1 JUDGE McGUIRE: Yes.

2 THE WITNESS: So -- (witness indicating).

3 And I have labeled the diagram further to show  
4 that the burst length subtable -- or I don't know what  
5 you want to call this, but this little table that's  
6 call Burst Length and this little table that's called  
7 Latency Mode, both of these tables specify manners in  
8 which the DRAM is to respond to requests received by  
9 the DRAM from the memory controller.

10 BY MR. OLIVER:

11 Q. Thank you, Professor Jacob.

12 A. You're welcome.

13 JUDGE McGUIRE: Do you want to go ahead and  
14 just have that marked as DX-100 while you're up there.

15 MR. OLIVER: May I approach, Your Honor?

16 JUDGE McGUIRE: Yes.

17 (DX Exhibit Number 100 was marked for  
18 identification.)

19 BY MR. OLIVER:

20 Q. Now, Professor Jacob, just so the record is  
21 clear, I believe my question was framed specifically  
22 with respect to CAS latency, but I believe in your  
23 discussion you referred both to CAS latency and burst  
24 length.

25 A. Oh. I'm sorry.

1 Q. That's quite all right.

2 I just wanted to be clear, though, that first  
3 of all with respect to the explanation that you've  
4 given, the claim table on page 1 of DX-99, does that  
5 set forth the basis for your conclusion that claim 160  
6 of the amendment to the '961 application could be  
7 reasonably interpreted by an engineer as covering the  
8 CAS latency feature as incorporated in the JEDEC SDRAM  
9 standard?

10 A. Yes, it does.

11 Q. And does the claim chart set forth on page 1 of  
12 DX-99 also set forth the basis for your conclusion --

13 A. Yes, it does.

14 Q. Let me make sure the record is clear.

15 It also sets forth the basis of your conclusion  
16 that claim 160 of the amendment to the '961 application  
17 could also be construed by a reasonable engineer to  
18 cover the burst length feature as incorporated in the  
19 JEDEC SDRAM standard?

20 A. Yes.

21 Q. Now, Professor Jacob, in interpreting the  
22 claim 160 of the amendment to the '961 application, did  
23 you interpret the word "bus" in that claim to be a  
24 narrow, multiplexed bus of the type that you described  
25 earlier?

1 A. No, I did not.

2 Q. Why not?

3 A. I interpreted "bus" to -- using the normal and  
4 common definition of the term, which is simply a  
5 collection of wires.

6 MR. OLIVER: May I approach, Your Honor?

7 JUDGE McGUIRE: Yes.

8 BY MR. OLIVER:

9 Q. Professor Jacob, I've handed you a document  
10 that's been marked as CX-1892. It's a report of  
11 William Huber regarding claim construction and  
12 infringement of U.S. patent numbers in connection with  
13 the Micron versus Rambus litigation.

14 Is this a document that you considered in the  
15 course of your work on this matter?

16 A. Yes, it is.

17 Q. And generally, what is the subject matter of  
18 CX-1892?

19 A. It describes claim construction and  
20 infringement of patents.

21 Q. Could you turn, please, to page 25 of CX-1892.

22 And if I could direct your attention in  
23 particular to the bottom box on page 25, the left-hand  
24 side that reads "a bus or external bus." Do you see  
25 that?

1 A. Yes, I do.

2 Q. And then in the right-hand side there's a  
3 caption towards the top that says "Meaning and Basis"  
4 and then in the box next to "bus" under Meaning and  
5 Basis it reads, "A bus is a set of signal lines used by  
6 an interface system to which a number of devices are  
7 connected and over which information is transferred  
8 between devices."

9 Do you see that?

10 A. Yes, I do.

11 Q. Did you consider that definition of a bus in  
12 connection with your claim interpretation?

13 A. Yes, I did.

14 Q. And is that definition of a bus appearing at  
15 page 25 of CX-1892 consistent with the way that you  
16 defined "bus" for purposes of this analysis?

17 A. Yes, it is.

18 Q. And by the way, Professor Jacob, did you  
19 understand Mr. Huber to be working on behalf of Micron  
20 or on behalf of Rambus in connection with this  
21 litigation?

22 A. I believe he was working on the behalf of  
23 Rambus.

24 MR. OLIVER: May I approach, Your Honor?

25 JUDGE McGUIRE: Yes.

1 BY MR. OLIVER:

2 Q. Professor Jacob, I've handed you a document  
3 marked as CX-1875. It's also an expert report of  
4 William Huber and in this case in connection with the  
5 litigation of Rambus versus Infineon.

6 Now, did you consult CX-1875 in connection with  
7 your analysis of the patent claims?

8 A. Yes, I did.

9 Q. If I could ask you to turn, please, to page 77  
10 of CX-1875.

11 I'd like to direct your attention here to the  
12 line starting on the left-hand side with "bus" that  
13 appears in the second row on page 77.

14 A. Uh-huh.

15 Q. And again --

16 A. Yes.

17 Q. -- in that row on the right-hand side under  
18 Meaning and Basis, "A bus is a set of signal lines used  
19 by an interface system to which a number of devices are  
20 connected and over which information is transferred  
21 between devices."

22 Again, is that definition of the term "bus"  
23 consistent with the way that you defined "bus" in your  
24 interpretation of claim 160 in the amendment to the  
25 '961 application?

1 A. Yes, it is.

2 MR. OLIVER: May I approach, Your Honor?

3 JUDGE McGUIRE: Yes.

4 BY MR. OLIVER:

5 Q. Professor Jacob, I've handed you a document  
6 that's been marked as CX-1893. This is an expert  
7 report of Robert Murphy in connection with the Micron  
8 versus Rambus litigation.

9 Did you consult CX-1893 in connection with your  
10 claims analysis?

11 A. Yes, I did.

12 Q. If I could ask you to turn, please, to page 27.

13 Professor Jacob, on page 27, the term --  
14 focusing particularly on the paragraph in the middle of  
15 the page, stating "Bus: A plurality of conductors  
16 capable of being connected to at least two  
17 communicating entities," is that statement of bus  
18 consistent with your interpretation of the term "bus"  
19 as you used it interpreting claim 160 of the amendment  
20 to the '961 application?

21 A. Yes, it is.

22 Q. Now, Professor Jacob, returning for a moment to  
23 the language of the claim 160 as set forth on page 1 of  
24 DX-99, there's a term "transaction request."

25 Now, what is a transaction request?



1           A. That's a general term meaning to be inclusive  
2 of read requests and write requests and perhaps control  
3 information as well.

4           Q. Is that the way that you interpreted that term  
5 in connection with your interpretation of claim 160 of  
6 the amendment to the '961 application?

7           A. Yes, it is.

8           MR. OLIVER: May I approach, Your Honor?

9           JUDGE McGUIRE: Yes.

10          BY MR. OLIVER:

11          Q. Professor Jacob, I've handed you a document  
12 marked as CX-1881. This is the supplemental report of  
13 William Huber in the Rambus versus Infineon  
14 litigation.

15                 And if I could ask you to turn, please, to  
16 page 18 of CX-1881.

17                 And I'd like to focus on the box in the  
18 left-hand side that reads "transaction request" and  
19 then on the right-hand side under Meaning and Basis it  
20 reads: "Transaction request is an instruction to  
21 perform one of a set of possible memory operations,  
22 such as writing data to or reading data from the  
23 specified memory cells of the memory. These operations  
24 are specified by binary logic levels provided to the  
25 memory device during a single clock cycle and received

1 by the memory device in response to a clock  
2 transition."

3 Do you see that?

4 A. Yes.

5 Q. Now, is that description of a transaction  
6 request consistent with the way that you interpreted

1 opinion as to whether a reasonable engineer could  
2 conclude that claim 164 of the January 1995 amendment  
3 could cover the programmable CAS latency feature as  
4 contained in the JEDEC SDRAM standard.

5 A. Yes. Absolutely.

6 Q. Could you please explain your conclusion.

7 A. Well, claim 164 is an extension of claim 160,  
8 further narrowing the scope of the 160, and as we  
9 described earlier, claim 160 describes the mode  
10 register. This further limits that to a mode register  
11 or a register holding the value indicative of an access  
12 time.

13 So for example, if we go through this claim  
14 by -- element by element, element 2 is that  
15 restriction, an access-time register, and it's  
16 described -- that LTMODE portion of the SDRAM mode  
17 register contains CAS latency information, which is an  
18 access time. It is -- it defines the amount of time  
19 that should transpire between the DRAM receiving a read  
20 request and the moment that the DRAM begins placing the  
21 corresponding data out onto the DRAM, so that is a  
22 latency, that is an access time, that is a variable  
23 amount of delay. So that is a de facto access-time  
24 register in the SDRAM specification.

25 Element 3 states that the DRAM should use this

1 access time information in response to a transaction  
2 request specifying the semiconductor. And for example,  
3 that -- such a transaction request could specify the  
4 semiconductor using a JEDEC or, rather, in the JEDEC  
5 organization using the chip-select bus.

6 Q. Focusing --

7 A. I'm sorry. As shown on pages 21 and 121 of  
8 JX-56.

9 Q. Focusing on the language you just mentioned,  
10 the transaction request specifying a semiconductor  
11 device, does claim 164 indicate how the transaction  
12 request would specify the semiconductor device?

13 A. No, it does not.

14 Q. And could a chip-select line specify the  
15 semiconductor device?

16 A. Yes, it could.

17 Q. In your opinion, would a chip-select signal be  
18 part of a transaction request?

19 A. Yes, it would.

20 Q. In your opinion, is there anything in claim 164  
21 that would limit that claim to use of Rambus' device  
22 identifier feature?

23 A. No.

24 Q. If I could ask you to turn next to claim 151 of  
25 the January 1995 amendment to the '961 application.

1 This can be found I believe at pages 218 and 219 of  
2 CX-1504.

3 Now, did you form any conclusion as to whether  
4 a reasonable engineer could conclude that claim 151  
5 would cover any of the features contained in the JEDEC  
6 SDRAM standard?

7 A. Yes.

8 Q. What was your conclusion?

9 A. This would also cover work within 42.3.

10 Q. And can you please explain to us briefly your  
11 conclusion?

12 A. This is very similar to claim 160 that we just  
13 looked at, the primary difference being that the focus  
14 of this particular claim being a computer system  
15 comprising a bus, a bus master and a -- it's basically  
16 the focus is the computer system whereas in claim 160  
17 the focus is the semiconductor device within that  
18 memory storage system.

19 So claim 151 is the same thing just in a more  
20 broad scope.

21 Q. In other words, claim 151 would cover a  
22 computer system that incorporated the memory storage  
23 system covered in claim 160?

24 A. Yes, it would.

25 Q. If I could ask you to turn next, please, to

1 claim 165. This appears I believe at page 223.

2 Now, did you form any conclusion as to the  
3 scope of coverage of claim 165 of the January 1995  
4 amendment to the '961 application?

5 A. Yes, I did.

6 Q. And what was your conclusion?

7 A. This again is similar. This covers the same  
8 thing as -- well, not the same thing, but this is very  
9 similar in its intent as claim 160 in that it's  
10 describing a -- this type of behavior where the DRAM  
11 was configurable, only the focus here is the method for  
12 configuring the semiconductor device rather than the  
13 mode register.

14 Q. Just to be clear then, did you reach any  
15 conclusion as to whether claim 165 would cover the  
16 method of configuring operation of CAS latency as  
17 described in the JEDEC SDRAM standard?

18 A. Yes. Absolutely.

19 Q. And what was your conclusion?

20 A. It would cover the method of programming CAS  
21 latency.

22 Q. And did you also reach a conclusion as to  
23 whether a reasonable engineer could conclude that  
24 claim 165 would also apply to the method of determining  
25 burst length --

1           A.  Yes.

2           Q.  -- as set forth in the JEDEC SDRAM standard?

3           A.  Yes.

4           Q.  If I could ask you to turn next, please, to  
5   page 258 in CX-1504.

1 that conclusion.

2 A. Well, for this I would like to look at page 3  
3 of DX-99, the claims analysis for claim 183 of  
4 application 08/469,490.

5 So this shows that -- how this particular claim  
6 relates to, for instance, CAS latency -- the CAS  
7 latency of JEDEC SDRAM parts.

8 So we'll take it element by element.

9 The first element describes a computer system  
10 with a semiconductor device and a bus, and the JEDEC  
11 work was clearly focusing on SDRAMs and which operate  
12 in computer systems. And buses are shown within the  
13 standard, for example, on page 164 of JX-56.

14 Element 2 describes the access-time register of  
15 the semiconductor device that contains an access time  
16 for the semiconductor device, and as described earlier  
17 and is shown on DX-100, there is a component within the  
18 SDRAM mode register of JEDEC-compliant DRAMs that  
19 contains CAS latency information and that that CAS  
20 latency information corresponds to an access time. It  
21 tells the DRAM how long to wait before driving data out  
22 onto the bus.

23 So element 3 describes the -- how the memory  
24 controller, a bus master, programs that access-time  
25 register. It says that the bus master should transmit



1 the value -- transmit a value to the semiconductor via  
2 the bus and that the semiconductor device should read  
3 that value off of the bus and store it locally in its  
4 access-time register.

5 And in JX-56, the SDRAM specification, it shows  
6 the power-on configuration sequence where the memory  
7 controller transmits configuration information over the  
8 bus that is read by the DRAM off of the bus and put  
9 directly into this SDRAM mode register, and that's  
10 shown on pages 114, 115 and 116.

11 Element 4 states that the value in the  
12 access-time register should indicate to the DRAM or,  
13 rather, the semiconductor device how long to wait in  
14 response to a request before driving data out onto the  
15 bus, for example, how long to wait before satisfying  
16 that request.

17 And as described, this is exactly what the  
18 programmable CAS latency feature of JEDEC SDRAMs does,  
19 that the programmable CAS latency feature tells the  
20 DRAM how long to wait before driving data out onto the  
21 bus in response to a read request.

22 Q. Now, with respect to the term "transaction  
23 request specifying a semiconductor device," did you  
24 interpret that in the same way that you interpreted  
25 the phrase in connection with the January 1995

1 amendment?

2 A. Yes, I did.

3 Q. If I could ask you to look, please, at  
4 claim 184 of the same amendment. This appears on  
5 page 265.

6 Did you reach any conclusion as to whether a  
7 reasonable engineer might understand that claim 184  
8 applied to a semiconductor device manufactured in  
9 compliance with the JEDEC SDRAM standard?

10 A. Yes, I did.

11 Q. And what was your conclusion?

12 A. That it does relate to JEDEC-compliant SDRAMs  
13 with the programmable CAS latency feature.

14 Q. Could you please explain just very briefly what  
15 the basis of that conclusion is.

16 A. This claim is very similar to claim 183,  
17 whereas claim 183's focus is on a computer system that  
18 includes a bus and a semiconductor device, claim 184 is  
19 focusing on the semiconductor device.

20 Q. If I could direct your attention to claim 185  
21 appearing at pages 265 and 266 of CX-1504.

1           A. That it does cover the JEDEC SDRAMs.

2           Q. Again, can you explain just very briefly the  
3 basis of that conclusion?

4           A. This is similar to claims 183 and 184, except  
5 that the focus of this claim is on the method for  
6 programming the access-time register rather than the  
7 computer system or the semiconductor device.

8           MR. OLIVER: Your Honor, I'd like to move into  
9 evidence CX-1892. This is the report of William Huber  
10 in the Micron versus Rambus matter.

11           JUDGE McGUIRE: Any objection?

12           MR. PERRY: Yes, Your Honor.

13           We had numerous conversations with complaint  
14 counsel on the subject of expert reports from other  
15 cases, and we've always said they shouldn't be in.  
16 They've always been excluded from the stipulations. We  
17 didn't know he was going to offer them in today. We  
18 certainly do object. We'd be happy to brief that or  
19 have a further discussion with you.

20           JUDGE McGUIRE: Mr. Oliver, any response?

21           MR. OLIVER: I apologize. I didn't mean to  
22 take you by surprise.

23           Why don't I withdraw it for the time being.  
24 We'll consult and figure out how to proceed.

25           JUDGE McGUIRE: All right. Very good.

1 BY MR. OLIVER:

2 Q. Professor Jacob, I'd like to turn now to the  
3 topic of on-chip PLL and on-chip DLL.

4 Your Honor, may I approach?

5 JUDGE McGUIRE: Yes.

6 BY MR. OLIVER:

7 Q. Professor Jacob, I've handed you a document  
8 marked as JX-21. This consists of the meeting minutes  
9 of the September 1994 meeting of the JC-42.3  
10 subcommittee in JEDEC.

11 Professor Jacob, did you review JX-21 in the  
12 course of your work on this matter?

13 A. Yes, I did.

14 Q. If I could ask you to turn, please, to page 86  
15 and take a quick look at pages 86 through 92.

16 (Pause in the proceedings.)

17 I'd just like to ask whether you recognize the  
18 presentation that appears at these pages.

19 A. Yes, I do.

20 Q. And if I could ask you to focus in particular  
21 on page 91.

22 And if I could ask you to explain this very  
23 briefly, please, what is depicted on page 91 of JX-21.

24 A. This demonstrates a proposal for the use of a  
25 PLL on a synchronous DRAM and it -- they're showing how

1 PLL can be used to synchronize an external clock and an  
2 internal clock, the external clock being a CLK and the  
3 internal clock being ICLK.

4 MR. OLIVER: May I approach, Your Honor?

5 JUDGE McGUIRE: Yes.

6 MR. OLIVER: By the way, Your Honor, I should  
7 just mention for the sake of updating my earlier time  
8 estimate, unfortunately this is taking longer than I  
9 expected with the demonstratives and documents and the  
10 like, so I do expect that we'll finish today, but I  
11 think it's going to take me longer than originally  
12 estimated.

13 JUDGE McGUIRE: Okay. Go ahead.

14 BY MR. OLIVER:

15 Q. Professor Jacob, I've handed you a document  
16 marked as CX-1502. This is the file wrapper for  
17 U.S. Patent Number 5,657,481.

18 And let me ask you to turn in particular to  
19 page 205 of CX-1502.

20 At page 205 is a document with the caption In  
21 the United States Patent and Trademark Office. There's  
22 a box in the right-hand side with the handwritten date  
23 June 28, 1993. About halfway down the page is the  
24 caption Preliminary Amendment, in the upper left-hand  
25 side in the box Serial Number 07/847,692.

1           Professor Jacob, have you -- or in the course  
2 of your work in this matter, did you review the  
3 preliminary amendment appearing at page 205 of  
4 CX-1502?

5           A. Yes, I did.

6           Q. I'd like to direct your attention in particular  
7 to claim 151, which appears on page 208.

8           Looking at claim 151 appearing at page 208 of  
9 CX-1502, did you reach any conclusion as to whether an  
10 engineer reasonably could construe claim 151 of this  
11 amendment to cover a JEDEC-compliant SDRAM with the  
12 addition of a PLL circuit as set forth in the  
13 September 1994 NEC proposal?

14          A. Yes, I did.

15          Q. And what was your conclusion?

16          A. That it would -- it would cover.

17          Q. I'd like to ask you to explain that  
18 conclusion, please. Before you do, I think that we  
19 have another demonstrative that I'd like to place up  
20 on the easel.

21          A. Yes.

22                 MR. OLIVER: Could I approach, Your Honor?

23                 JUDGE McGUIRE: Yes.

24                 BY MR. OLIVER:

25          Q. I believe you also have a claim chart appearing

1 at page 4 of DX-99?

2 A. Yes, I do.

3 Q. Could you please explain your conclusion with  
4 respect to the scope of coverage of claim 151 of the  
5 amendment to the '692 application using the claim chart  
6 as you wish and also if -- Your Honor, if he could be  
7 permitted to approach the easel?

8 JUDGE McGUIRE: Yes. Go ahead.

9 THE WITNESS: I'm sorry.

10 JUDGE McGUIRE: And while you're up there,  
11 let's mark that as DX-101.

12 MR. DETRE: Your Honor, is it all right if I  
13 just move over here to observe (indicating)?

14 JUDGE McGUIRE: Sure.

15 (DX Exhibit Number 101 was marked for  
16 identification.)

17 THE WITNESS: So we can go through the claim  
18 chart element by element, and again this is the claim  
19 chart on page 4 of DX-99, which gives the text of  
20 claim 151 of application 07/847,692.

21 So element 1 describes a memory device on a  
22 single substrate. That's what DRAMs are, single-chip  
23 memory devices.

24 Element 2 describes a memory array that stores  
25 data at addresses. Well, that would be this. This is

1 your memory array (indicating). This is the box that  
2 is in the figure labeled "memory array." That is for  
3 storing data at addresses. That's sort of the  
4 definition of arrays and memory arrays.

5 Element 3 describes a clock signal receiving  
6 circuit coupled to receive an external clock signal, so  
7 this right here, this sort of right triangle on the  
8 upper left-hand side of the right half of the diagram,  
9 that is -- the triangle is labeled "receiver." This is  
10 the clock signal receiving circuit (indicating).

11 And it is coupled to receive an external clock  
12 signal. This is the external clock signal that is  
13 labeled "CLK" (indicating).

14 And in these diagrams, note that the little  
15 tiny circles are representing pins, so that's something  
16 outside of the little circuit, is meant to be an  
17 external signal, so this CLK is an external signal and  
18 over here, DQ, this represents an external connection  
19 to the data bus, so this is a pin, that is a pin, these  
20 two little circles represent pins (indicating).

21 So we've got a clock signal receiving circuit  
22 coupled to receive an external clock signal for



1 than being outside of the DRAM.

2 So this is my local clock circuit -- my local  
3 clock signal.

4 And element 3 says that the local clock signal  
5 should be performing memory operations with respect to  
6 the memory array. Well, the figure shows the local  
7 clock signal coupled to the memory array through this  
8 output driver that drives data out onto the data bus,  
9 so you know, so this is, you know -- performs read  
10 operations (indicating).

11 As shown in this diagram, the clock is driving  
12 data out onto the bus. It's orchestrating that  
13 timing.

14 So that's the operation with respect to the  
15 memory array that the clock is performing.

16 Element 4 of the claim describes a phase-locked  
17 loop -- I don't need to label that again. That's that  
18 PLL box that's in the middle.

19 The phase-locked loop is coupled to the clock  
20 signal receiving circuit, and as you can see, it's  
21 coupled to the clock signal receiving circuit  
22 (indicating).

23 The element says that it should also be coupled  
24 to the memory array. And we see that it is coupled to  
25 the memory array through this driver circuit

1 (indicating).

2 And the element states that it should provide  
3 a variable delay to the local clock signal such that  
4 the delayed local clock signal is synchronized with  
5 the external clock signal. And that's what is shown  
6 in the bottom half of both of these two diagrams. On  
7 the left we have a system that has no PLL and the  
8 corresponding timing diagram. On the right-hand side  
9 we show the inclusion of the PLL and the resulting  
10 timing diagram.

11 And as you can see, in the left-hand timing  
12 diagram, the external clock signal, this CLK, and the  
13 internal clock signal, ICLK, these two are not in sync  
14 with each other. They're out of sync. But with the  
15 inclusion of the PLL, it now synchronizes the CLK and  
16 ICLK signals so that the timing diagram on the  
17 right-hand side of this illustration, the two are now  
18 in sync.

19 And that's what the PLL is doing. Its job is  
20 to delay this clock so that -- the internal clock, so  
21 that the internal clock becomes in sync with the  
22 external clock.

23 Q. Thank you.

24 A. No problem.

25 Q. Now, if I could ask you to look once again at

1 CX-1502, and if I could ask you to turn, please, to  
2 page 233.

3 This is an amendment of -- that was filed with  
4 the typewritten notation in the box in the upper  
5 right-hand side October 23, 1995. The box in the  
6 upper left-hand side again indicates Serial  
7 Number 07/847,692.

8 Professor Jacob, did you review this document  
9 in connection with the work you did in this case?

10 A. Yes, I did.

11 Q. And if I could ask you to turn, please, to  
12 claim 151, which begins at the bottom of page 233 and  
13 continues over to the top of 234.

14 A. Okay.

15 Q. And did you reach a conclusion as to whether a  
16 reasonable engineer could conclude that claim 151 in  
17 this October 1995 amendment could cover a  
18 JEDEC-compliant SDRAM plus the inclusion of a PLL  
19 circuit as proposed in the NEC proposal of  
20 September 1994?

21 A. Yes, I did.

22 Q. What was your conclusion?

23 A. That an engineer reading this would conclude  
24 that it covers that scenario presented by NEC.

25 Q. Can you please explain briefly the basis for

1 that conclusion?

2 A. Well, this is a rewording of the previous claim  
3 and the wording changes are cosmetic; they don't  
4 actually change the meaning of the claim.

5 Q. So would it be fair to say that the substance  
6 of your prior analysis as set forth on page 4 of DX-99  
7 would also apply to claim 151 in the October 1995  
8 amendment?

9 A. Yes.

10 Q. Professor Jacob, let's turn next to, if we  
11 could, to dual-edged clocking.

12 And have you formed any opinion as to whether  
13 an engineer could reasonably construe any of the claims  
14 that you've reviewed to cover dual-edged clocking as  
15 that technology was proposed for use in the JEDEC  
16 DDR SDRAM standard?

17 A. Yes, I have.

18 Q. And what is your conclusion?

19 A. My conclusion is that an engineer would get  
20 that understanding by reading some claims.

21 MR. OLIVER: May I approach, Your Honor?

22 JUDGE McGUIRE: Go ahead.

23 BY MR. OLIVER:

24 Q. Professor Jacob, I have handed you a document  
25 marked CX-1494, which is the U.S. Patent

1       Number 5,513,327 issued to Rambus with the issue date  
2       of April 30, 1996.

3               Professor Jacob, did you review this patent in  
4       connection with your work on this case?

5               A.   Yes, I did.

6               MR. OLIVER:   May I approach, Your Honor?

1 "dual clock edge"?

2 A. Yes.

3 Q. Now, what is your understanding of how, if at  
4 all, the proposal reflected here relates to dual-edge  
5 clocking?

6 A. This is dual-edged clocking. This proposal  
7 right here proposes dual-edged clocking.

8 MR. OLIVER: May I approach, Your Honor?

9 JUDGE McGUIRE: Yes.

10 BY MR. OLIVER:

11 Q. Professor Jacob, I've handed you a document  
12 marked JX-28. These are the meeting minutes of the  
13 42.3 subcommittee of December 6, 1995.

14 Did you review this document in connection with  
15 your work in this case?

16 A. Yes, I did.

17 Q. And if I could ask you to turn, please, to  
18 page 34. It's the section that begins "Future SDRAM  
19 Features Survey Ballot." Do you see that?

20 A. Yes, I do.

21 Q. And then continuing on to the next page and the  
22 next to last bullet point on that page 35, using both  
23 edges of the clock for sampling inputs. Do you see  
24 that?

25 A. Yes, I do.

1 Q. Now, how, if at all, did that reference relate  
2 to dual-edged clocking?

3 A. That is the definition of -- well, a definition  
4 of dual-edged clocking, using both edges of the clock  
5 to sample inputs.

6 Q. And sampling inputs there would be a write  
7 operation?

8 A. Yes. At the DRAM side, yes.

9 MR. OLIVER: May I approach, Your Honor?

10 JUDGE McGUIRE: Go ahead.

11 BY MR. OLIVER:

12 Q. Professor Jacob, I have handed you a document  
13 marked JX-31. These are the minutes of the JC-42.3  
14 committee meeting of March 1996.

15 Is this a document that you reviewed in  
16 connection with your work in this case?

17 A. Yes, it is.

18 Q. If I could ask you to turn, please, to page 6  
19 of JX-31.

20 There is a presentation there that reads  
21 "Future SDRAM" of Samsung, and within that I'd like to  
22 direct your specific attention to page 71.

23 And underneath the caption Proposed Clocking  
24 Scheme there are -- the fourth bullet point, data in  
25 sampled at both edge of clock into memory, and the last

1 bullet point, use both edge of the strobe clock to  
2 sample the memory data into controller?

3 A. Uh-huh.

4 Q. How, if at all, does this proposal relate to  
5 dual-edged clocking?

6 A. This describes using both edges of the clock to  
7 both read and write data to and from the DRAM, so this  
8 is dual-edged clocking.

9 Q. Now, in your opinion, could an engineer  
10 reasonably construe claim 1 of the '327 patent to cover  
11 a JEDEC-compliant SDRAM that also incorporated the  
12 dual-edged clocking proposals that we've just  
13 discussed?

14 A. Yes, an engineer could.

15 Q. Could you please explain your opinion.

16 A. Yes. Well, we can go element by element  
17 through the claim. I'm going to refer here to page 5  
18 of DX-99 that gives the wording of claim 1 of the  
19 '327 patent.

20 And element 1 describes the DRAM, dynamic  
21 random access memory, with a first circuit for  
22 providing a clock signal. And as you can see, for  
23 example, in the Samsung presentation, specific --  
24 specific mentions of clocks, so -- an SDRAM uses an  
25 external clock signal generating an internal clock



1 signal, so for instance, in the Samsung presentation in  
2 JX-56, page 124.

3 Element 2 describes a conductor pin that  
4 couples the DRAM to a bus and a receiver coupled to the  
5 conductor and the first circuit, and that simply means  
6 the DRAM has a clock pin with a receiver circuit, so,  
7 for example, see pinout diagrams within the spec at  
8 page 106 of JX-56.

9 Element 3 describes that the receiver circuit  
10 should latch -- the receiver circuit should latch  
11 information on a rising edge of the clock and a falling  
12 edge of the clock, and I believe we've got -- well,  
13 this just -- this is just a description of a dual-edged  
14 clock. We've latched data in response to the rising  
15 edge of the clock and the falling edge of the clock,  
16 which is basically what's being said in the Samsung  
17 presentation, data sampled at both edges of the clock,  
18 meaning the rising edge and the falling edge of the  
19 clock.

20 Element 4 describes a specific implementation  
21 of that where you pingpong back and forth between two  
22 input receivers, a first input receiver and a second  
23 input receiver, where one latches information  
24 corresponding to the rising edge of the clock and the  
25 other one latches information in response to the

1 falling edge of the clock, so this is sort of an  
2 implementation detail that's how you would implement  
3 dual-edged clocking because any given latch cannot  
4 operate on both edges of a clock, a latch can only  
5 respond to either of the rising edge or the falling  
6 edge, so the only way to perform this is really to have  
7 two latches, one in response to the rising edge, one in  
8 response to the falling edge.

9 Q. I notice a reference to interleaving on page 5  
10 of DX-99.

11 Now, is that the same interleaving technique  
12 that you referred to this morning when you were  
13 discussing alternatives?

14 A. Oh, no. No. No, it isn't. That is what I'm  
15 describing by saying you would pingpong back and forth  
16 between two latches. That is just a form of  
17 interleaving, but it's very different from what I was  
18 describing this morning where what you interleave  
19 between are two complete banks, which are large  
20 structures on the DRAM. This would be a very small  
21 input receiver that you toggle between an input latch.

22 Q. Now, in your opinion, could an engineer  
23 reasonably construe claim 7 of the '327 patent to cover  
24 a JEDEC-compliant SDRAM that also incorporated the  
25 dual-edged clocking proposals that we discussed a few



1 dual-edged clocking scheme, this is the most reasonable  
2 implementation.

3 Q. By the way, just to be clear, in claim 7 of the  
4 '327 patent, would that apply to a read operation or to  
5 a write operation?

6 A. I'm sorry. I should have been more precise.  
7 Element 3 describes the DRAM driving data out  
8 on both edges of the clock, so that would be a read  
9 operation.

10 Q. Now, with respect to the comparison between the  
11 claim 7 of the '327 application and certain of the  
12 earlier proposals we looked at, specifically the  
13 April 1992 IBM proposal and the survey ballot, would  
14 your analysis differ at all comparing the claim 7 of  
15 the '327 patent to --

16 A. No. No. This describes dual-edged clocking.

17 MR. OLIVER: May I approach, Your Honor?

18 JUDGE McGUIRE: Yes.

19 BY MR. OLIVER:

20 Q. Professor Jacob, I've handed you a document  
21 marked CX-1493, which is the copy of the file wrapper  
22 for U.S. Patent 5,513,327. I'd like you to turn in  
23 particular to page 183 in CX-1493.

24 Page 183 is a document marked Preliminary  
25 Amendment. The box in the right-hand side has a

1 handwritten date of September 6, 1994. The left-hand  
2 side of the box has a caption Serial Number 08/222,646.

3 Professor Jacob, did you review this  
4 preliminary amendment in the course of your work on  
5 this matter?

6 A. Yes, I did.

7 Q. I'd like to direct your attention to claim  
8 number 151 of the '646 amendment. It begins on the  
9 bottom of page 184 and carries over to the top of  
10 page 185.

11 Did you reach any conclusion as to whether  
12 claim 151 in the September 1994 amendment to the  
13 '646 application could be reasonably construed to cover  
14 a JEDEC-compliant SDRAM that also incorporated the  
15 dual-edged clocking proposals that we discussed a few  
16 moments ago?

17 A. Yes, I did.

18 Q. And what was your conclusion?

19 A. That it would.

20 Q. Can you please briefly explain your  
21 conclusion?

22 A. This describes the general concept of  
23 dual-edged clocking, so if you walk throTrlrhhis



1 A. Yes, I did.

2 Q. And what was your conclusion?

3 A. That claim 1 does cover it.

4 Q. Could you please explain how you arrived at  
5 that conclusion.

6 A. I'd like to --

7 MR. OLIVER: I believe we have another  
8 demonstrative, Your Honor.

9 JUDGE McGUIRE: Go ahead.

10 THE WITNESS: May I?

11 JUDGE McGUIRE: Yes.

12 THE WITNESS: Thank you.

13 So I will walk through claim 1 of '327, and if  
14 you want to follow, this is on page 7 of DX-99.

15 So if we go through it element by element,  
16 element 1 describes a dynamic random access memory, a  
17 DRAM, with a first circuit for providing clock signal.  
18 Well, what we're talking about is DRAMS here.

19 Here is the first circuit for providing a clock  
20 signal (indicating). It is this wire in the bottom  
21 right-hand side of this figure, the wire that has a  
22 number of arrows coming out of it, and for instance,  
23 the end of the wire goes into the -- this box labeled  
24 "right FIFO and drivers" and where the wire goes into  
25 that box is labeled "CKN," meaning that this is the --

1 we have a clock input to this component here called  
2 "right FIFO and drivers," so that means that this wire  
3 right here is a clock wire. So this is the first  
4 circuit that provides the clock signal right there  
5 (indicating).

6 Element 2 describes a conductor for coupling  
7 the DRAM to a bus, so we will consider these pins right  
8 here that are labeled DQ 0 through DQ 3, this would be  
9 with the conductor -- conductors for coupling the DRAM  
10 to the bus (indicating).

11 Element 2 continues "a receiver circuit coupled  
12 to the conductor and the first circuit," so that would  
13 be this component that I have circled, which includes  
14 the -- well, actually not those so much but mostly this  
15 box labeled "receivers" and then the bottom two boxes  
16 in this stack that has been labeled "input registers"  
17 in the diagram, so this whole circuit right here is the  
18 receiver circuit (indicating). That is described in  
19 element 2.

20 And as you can see, it is coupled to the  
21 conductor, this conductor, the DQ conductors through  
22 that wire. And it is also coupled to the first circuit  
23 through that wire coming up from underneath.

24 Element 3 describes the general behavior of  
25 this system. It says that the receiver circuit should



1 latch information received from this conductor on both  
2 the rising edge of the clock signal, of this clock  
3 signal which is DQS, and the falling edge of that clock  
4 signal, and as shown on page 32 of JX-57, we have a  
5 timing diagram that illustrates that. I think we'll  
6 pull that up on the screen.

7 So what we have here in the second to bottom  
8 line down here that's labeled "DQ," we have a bunch of  
9 stuff happening there over time. What that shows is  
10 the little sort of -- I don't know -- hexagons that are  
11 filled with white, that's considered valid data.

12 So these are valid data windows over time.  
13 DQ, that means data. And several lines above that is  
14 the timing diagram for DQS, and as we see, the edges  
15 of DQS, where DQS goes from low to high and where DQS  
16 goes from high to low, that corresponds to these valid  
17 data windows on DQ. That means that the data on DQ is  
18 latched in sync with the rising edge and the falling  
19 edge of DQS. That illustrates this behavior. That  
20 says this DQS signal right here that's connected up to  
21 these latches is causing the data coming off of this  
22 pin to be latched on both the rising edge and the  
23 falling edge of that DQS clock signal (indicating).

24 So that's what element 3 is saying.

25 Element 4 says "wherein the receiver circuit

1 comprises a first input receiver coupled to the  
2 conductor and the first circuit," so I'll label this  
3 top box the first input receiver and the bottom box  
4 will be the second input receiver (indicating).

5 So you see two of them stacked on top. One is  
6 the first input receiver; the other is the second input  
7 receiver. And one is going to latch on the rising edge  
8 of the clock and the other is going to latch  
9 corresponding to the falling edge of the clock.

10 And I believe that's it.

11 JUDGE McGUIRE: Then while you're up there,  
12 let's mark that as DX-102.

13 THE WITNESS: Thank you.

14 JUDGE McGUIRE: Thank you.

15 (DX Exhibit Number 102 was marked for  
16 identification.)

17 BY MR. OLIVER:

18 Q. Professor Jacob, at the bottom of what's been  
19 marked as DX-102, there's a notation in note 1 that  
20 this is a functional block diagram.

21 Do you see that?

22 A. Uh-huh. Yes.

23 Q. Now, what's your understanding of that  
24 statement?

25 A. I read that as a disclaimer to indicate to the

1 reader that this is not a fully functional  
2 implementation. This is a simplified version of a real  
3 implementation and it just happens to be missing some  
4 signals to -- basically for clarity. There are places  
5 where, for instance, there should be a clock signal,  
6 but there isn't.

7           So it's just a -- it's meant to convey a  
8 general idea of how the system works but Eyk2t to convey sc2

1 and I think we have one more copy of the same page in  
2 which I'd like to ask you to again point out the  
3 specific elements.

4 Your Honor, may I approach?

5 JUDGE McGUIRE: Yes.

6 THE WITNESS: May I?

7 JUDGE McGUIRE: Go ahead.

8 THE WITNESS: Thank you.

9 And shall I label this?

10 JUDGE McGUIRE: DX-103.

11 (DX Exhibit Number 103 was marked for  
12 identification.)

13 THE WITNESS: So I will be reading through the  
14 claim 7 as part of the claims analysis, the claims  
15 flowchart on page 8 of DX-99.

16 So element 1 describes a DRAM, a DRAM with a  
17 first circuit for providing a clock signal. So for  
18 example, here is a first circuit for providing a clock  
19 signal. This CLK is a clock. And you see several  
20 clocks around the diagram, so there is a clock on the  
21 chip. This happens to be one instance of that clock  
22 (indicating).

23 Number 2 or, rather, element 2 describes a  
24 conductor for coupling the DRAM to the bus. That would  
25 be this little circle off to the right edge that's

1     labeled DQ 0 through DQ 3.  This would be our conductor  
2     (indicating) -- conductors coupling to the bus,  
3     coupling the DRAM to bus.  This is our data bus  
4     connection.

1           The multiplexer having an output, okay, so this  
2           is the wire that exits the box called mux to the right  
3           is the multiplexer's output. The multiplexer has a  
4           first input, and due to space reasons, I'm just going  
5           to label that 1. That will be where the top wire  
6           enters into that box labeled "mux." The wire with the  
7           "/4" through it, where that enters the mux we'll call  
8           that the first input at the bottom of the mux.  
9           Entering from the left-hand side, we'll call that the  
10          mux's second input.

11           So this is how mux have been drawn, two inputs  
12          and one output and a select function.

13           Let's see, where are we?

14           Element 3 further describes a first output  
15          line, so that would be this one, first output line  
16          (indicating). That would be the line with the "/4"  
17          through it that's connecting the read latch to the mux.  
18          The one on top and the line on bottom would be the  
19          second output line.

20           So we have the element describes a first output  
21          line connected to the first input of the multiplexer,  
22          and then further down in the element we have a second  
23          output line connected to the second input of the  
24          multiplexer, and then the second half of each of those  
25          paragraphs or subsections is wherein the multiplexer

1 couples the first output, the first output line to the  
2 output of the multiplexer in response to a rising edge  
3 of the clock and the multiplexer connects the second  
4 output line to the multiplexer output on the falling  
5 edge of the clock.

6 That's what's going on, this select line as it  
7 together goes up and down between zero and one, causes  
8 this multiplexer to alternate between driving this  
9 first output through this circuit, the output label and  
10 then selecting this wire, so it goes back and forth  
11 between selecting these two wires (indicating).

12 The first one selects that one and then that  
13 one and that one. It goes back and forth between the  
14 first output line and the second output line which  
15 corresponds to this read latch, has eight bits of data  
16 in it, so what this multiplexer does is it first grabs  
17 the top four bits and then the bottom four bits and  
18 then the top four bits and then the bottom four bits,  
19 and so forth, so that's what this element states and  
20 that's what's happening in the block diagram.

21 Q. Thank you, Professor Jacob.

22 Your Honor, I'm about to turn now to the last  
23 of the four topics, and first, I apologize. My time  
24 estimate was way off this afternoon. I think we can  
25 finish this in probably 40 to 45 minutes.

1           JUDGE McGUIRE: Okay. I would like to be done  
2 this afternoon if we could by quarter after five at the  
3 latest, you know, if we could be, which should give you  
4 45 minutes.

5           MR. OLIVER: That would be fine, Your Honor.

6           JUDGE McGUIRE: Okay. Go ahead.

7           BY MR. OLIVER:

8           Q. Professor Jacob, we're working you pretty hard.  
9 Do you need a short break?

10          A. No. I'm good.

11          Q. Okay. Professor Jacob, let's turn to the  
12 fourth question that you were asked to address today,  
13 namely, the implications of a redesign today.

14                 I've brought upatsq 5 ns of ahry. rrttN2k ahk4mt7aa

          Q. Okay. Profcanquestfirst please explaindesign today.  
howquestiont about ansionb, w 12 fo?design today.

9           1Well,UIRcaad nume s engat onb, wdocumentsaddress today,



1       implications?

2           A.   Yes.   That would be the following slide I  
3       believe.

4           Q.   We've pulled up a slide entitled DRAM Basics  
5       Graphics Card and we'll label this as DX-105.

6           And Professor Jacob, if you could please  
7       explain briefly what DX-105 shows.

8           A.   This shows a typical desktop system, the  
9       connections that are existent in your desktop system,  
10      and it shows the place of DRAM within that system.

11          So for example, you have a number of DRAM chips  
12      on the module off to the right and you have another  
13      group of DRAM chips that are on the graphics card that  
14      are talking to the CPU, and everywhere that you have  
15      DRAM you have a similar style bus connecting that to  
16      your CPU or controller.

17          Q.   I assume that this is a simplified --

18          A.   Yes.   Yes.   This is rather simplified.

19          Q.   Now, if we could again just very briefly take  
20      the various elements one at a time, starting with the  
21      memory controller.   Could you please remind us just  
22      very briefly of what the memory controller does.

23          A.   The memory controller is the centralized  
24      access point for the DRAM subsystem, so all of the  
25      requests for the DRAM system, whether they come from

1 the CPU or multiple CPUs or the graphics card, all  
2 requests for the DRAM system go through the memory  
3 controller.

4 Q. Now, in general terms, if the specification for  
5 the DRAM were to change, what, if any, would be the  
6 potential redesign implications for the memory  
7 controller?

8 A. Well, it would depend upon the change, but in  
9 general, it could require anything from logic changes,  
10 simple logic changes to the memory controller to pinout  
11 changes, signaling changes. It could require any  
12 number of different changes.

13 Q. Focusing next on the memory module, can you  
14 again remind us briefly of what the memory module does  
15 in a memory system?

16 A. The memory module provides you a convenient  
17 package for DRAM. It's a way to collect a number of  
18 DRAM into a small chunk that can be used rather than  
19 having to deal with individual DRAMs at a time.

20 Q. Again, in general terms, if the specification  
21 for the DRAM were to change, what, if any, would be the  
22 potential redesign implications with respect to the  
23 memory module?

24 A. It could require -- depending upon the types of  
25 changes you make to the DRAM, it could require trivial

1 changes to nontrivial changes like changes of -- add a  
2 number of connectors to the rest of the system or  
3 inclusion of extra chips on the module.

4 Q. Now, Professor Jacob, are you familiar with the  
5 so-called serial presence detect or SPD?

6 A. Yes, I am.

7 Q. What is that?

8 A. That's a chip that's on the module that  
9 identifies to the memory controller the configuration  
10 of the DRAMs that are on that module.

11 Q. Now, in general terms, if the specification for  
12 the DRAM were to change, what, if any, would be the  
13 potential redesign implications with respect to the  
14 serial presence detect?

15 A. It could change trivially or nontrivially.

16 For instance, if you had fixed latency parts,  
17 the serial presence detect would have to identify that  
18 information, that sort of thing.

19 Q. Focusing then on the motherboard, which is not  
20 specifically depicted here but which would be in the  
21 area in blue on which the various bus lines appear, in  
22 general terms, if the specification for DRAM were to  
23 change, what, if any, would be the potential redesign  
24 implications with respect to the motherboard?

25 A. Again, it depends upon the types of changes

1 that would go into the DRAM, but the types of changes  
2 could range from trivial or no changes whatsoever to  
3 nontrivial changes like the addition of more wires, a  
4 lot more wires, termination, that sort of thing.

5 Q. Looking next at the central processing unit or  
6 the CPU, and again in general terms, if the  
7 specification for the DRAM were to change, what, if  
8 any, would be the potential redesign implications for  
9 the CPU?

10 A. Well, the CPU is the originator of most of the  
11 requests in the system. It's the thing that's  
12 generating requests for data that are ultimately turned  
13 into reads and writes. And in most general-purpose  
14 systems like this, the CPU requests data at the  
15 granularity of a cache block size, so if, for example,  
16 you change the block size available from the DRAM, if  
17 you change the burst length to a different value than  
18 the one that the CPU expected, you might want to change  
19 your cache organization.

20 Q. Now, we've also heard discussion of a BIOS.  
21 BIOS is not reflected in this particular diagram here  
22 on DX-105.

23 Can you please briefly what the BIOS is?

24 A. It is a set instructions and information that  
25 helps the memory controller to configure the memory

1 system at start-up, and depending upon how -- depending  
2 upon what types of changes you make to your DRAM, you  
3 would have to rewrite the BIOS.

4 Q. Again -- okay.

5 Let's look for a moment at the graphics card.

6 Can you please explain, again very briefly,  
7 what SGRAM is?

8 A. That is an optimized form of DRAM that's used  
9 in graphics applications.

10 Q. And can you please explain what the CPU on the  
11 graphics card is?

12 A. That would be a graphics coprocessor that would  
13 integrate to processing functions as well as memory  
14 controller, and it would connect directly to the DRAMs  
15 instead of connecting to the DRAMs through a memory  
16 module.

17 Q. Now, in general terms, if the specification for  
18 the SGRAM were to change, what, if any, would be the  
19 potential redesign implications with respect to the  
20 graphics card CPU or the graphics card itself?

21 A. Depending upon the types of changes, it could  
22 be anything from trivial modifications to serious  
23 modifications, nontrivial modifications.

24 Q. Let's reflect back if we could on the various  
25 alternatives that we discussed this morning. Perhaps

1 we can start with the alternatives to programmable CAS  
2 latency.

3 And perhaps we could pull up -- oh, we have  
4 it -- the demonstrative.

5 It's the demonstrative you used this morning  
6 entitled Alternatives to Programmable CAS Latency,  
7 DX-65.

8 Now, with respect to the various alternatives  
9 to programmable CAS latency listed on DX-65, did you  
10 consider the degree of disruption, if any, that would  
11 be caused by these various alternatives?

12 A. Yes, I did.

13 Q. And can you explain in general terms, if the  
14 JEDEC SDRAM or DDR SDRAM standard were to be changed  
15 today, which of the alternatives listed on DX-65 would  
16 be the more disruptive alternatives?

17 A. Well, in general, some alternatives would be  
18 more disruptive than others. Some would cause the DRAM  
19 to be incompatible with existing JEDEC-compliant  
20 systems and others mifi 7 DX-65.



1           A. Yes. If you changed your memory controller to  
2 accommodate systems with different CAS latency and you  
3 changed your serial presence detect chip to notify the  
4 memory controller that this particular part can't  
5 support programmable latency, then you would be able to  
6 support it.

7           Q. Now, with respect to the second alternative,  
8 program CAS latency by blowing fuses on the DRAM, I  
9 believe that you testified this morning that once the  
10 fuses are blown, there's a similarity between the part  
11 with the blown fuse and a part with a fixed latency?

12          A. Yes, I did.

13          Q. Now, your testimony with respect to the  
14 redesign implications of fixed CAS latency, would that  
15 then also apply to parts that were -- in which the CAS  
16 latency was set by blowing a fuse?

17          A. Absolutely. Yes.

18          Q. Now, just in very general terms, again, if a  
19 change in the JEDEC standard would be made today, can  
20 you compare in general terms the redesign implications  
21 for the four alternatives in the red box with the  
22 redesign implications that you've just described for  
23 fixed CAS latency?

24          A. Well, if -- actually, could you repeat the  
25 question.



1 Q. Yes.

2 I was wondering if you could explain in general  
3 terms how a change today in the JEDEC standard to use  
4 one of the alternatives in the red box, namely  
5 alternatives 3, 4, 5 or 6, how the redesign  
6 implications of that type of change would compare with  
7 the redesign implications you have just described with  
8 respect to fixed CAS latency.

9 A. I see. Yes. The redesign implications would  
10 be at least as extensive. You would have to change at  
11 least the memory controller in the scenarios as well as  
12 other things such as the module, potentially the  
13 motherboard, and so forth.

14 Q. Now, Professor Jacob, what, if any, is the  
15 difference between making a change today in how CAS  
16 latency is determined as opposed to having selected a  
17 different method of determining CAS latency in the  
18 early to mid-1990s?

19 A. These would have been very straightforward  
20 designs had they been -- had this been decided the  
21 first time around. If you tried to redesign them  
22 today, that impacts -- this means that for one thing  
23 you throw away design work that has already been done.  
24 It would cause you to slip schedules for existing  
25 designs. Future designs would not be able to use

1 already generated designs or, rather, existing  
2 designs.

3 So this would throw off schedules. It would  
4 cause, you know, wastage of engineering effort. And  
5 if this had been designed in at the beginning, it  
6 would have been as straightforward as the present-day  
7 design.

8 Q. What about a comparison of the time, of the  
9 timing of the design change today versus design  
10 change -- or the selection of alternative in the early  
11 to mid-1990s?

12 A. I'm not sure I understand the question.

13 Q. What, if any, would be the implication with  
14 respect to timing of completion of design of products?

15 Obviously my question is not clear. I'll just  
16 move on then.

17 A. Okay.

18 Q. Thank you.

19 A. Sorry.

20 Q. Let's turn then to the alternatives that you  
21 had identified for programmable burst length.

22 If we could pull up DX-79, which lists the  
23 alternatives that you identified for programmable burst  
24 length.

25 Now, again, did you consider the degree of

1 disruption that the various alternatives listed in  
2 DX-79 would cause if a change were to be made today?

3 A. Yes, I did.

4 Q. If a change were to be made today, which of the  
5 alternatives listed on DX-79 would be among the more  
6 disruptive?

7 A. In general, some would be -- some would cause  
8 more disruption than others, and I believe we have a  
9 demonstrative to indicate which.

10 So for example, the alternatives highlighted in  
11 red would be more disruptive than those that are not  
12 highlighted in red.

13 If one were to build a DRAM using one of the  
14 alternatives highlighted in red, you would produce a  
15 DRAM that's incompatible with present JEDEC-compliant  
16 systems.

17 If one were to use one of the other  
18 alternatives that are not highlighted in red, you would  
19 produce a part that may or may not be compatible with  
20 existing JEDEC-compliant systems, and it would depend  
21 upon the system in question.

22 Q. Let the record reflect that the demonstrative  
23 to which Professor Jacob was referring is DX-107  
24 entitled Alternatives to Programmable Burst Length with  
25 some items placed in red boxes.

1           Looking for a moment at the first alternative,  
2           for example, which is not one of the ones you  
3           identified as more disruptive, using fixed burst length  
4           parts, again in order to try to save time, is there any  
5           significant difference with respect to the redesign  
6           implications today of using fixed burst length parts as  
7           opposed to using fixed CAS latency?

8           A. No. No.

9           Q. So the discussion you provided a moment ago  
10          with respect to design implications of fixed CAS  
11          latency would apply here as well?

12          A. Correct.

13          Q. Now, what, if any, is the difference between  
14          making a change today in how burst length is  
15          determined as opposed to JEDEC having selected a  
16          different method of determining burst length in the  
17          early to mid-1990s?

18          A. Well, again, if one were to create these  
19          designs or introduce these designs into present-day  
20          technology, it means that you would throw away existing  
21          designs. You would have to retest the new parts with  
22          the new designs. This would cause slippage of  
23          schedules. This would cause projected arrival times of  
24          parts to change.

25                 Whereas if this were known -- if this were --

1 if one of these alternatives was chosen in the  
2 early '90s, it would have been a very straightforward  
3 design to accomplish, and you know, it would be just as  
4 easy as the present-day system had they designed it in  
5 from the beginning.

6 Q. Let's turn back now to the alternatives that  
7 you discussed this morning with respect to dual-edged  
8 clocking.

9 If we could perhaps again pull up the  
10 demonstrative, DX-88, that listed the alternatives you  
11 identified to dual-edged clocking.

12 And again with respect to the alternatives  
13 listed -- actually I should specify that I think you  
14 said that number 7, in your opinion, is really not an  
15 alternative, so we'll focus on items 1 through 6.

16 And with respect to items 1 through 6 on DX-88,  
17 did you consider whether some of these alternatives  
18 might be more disruptive than others?

19 A. Yes, I did.

20 Q. And which alternatives did you identify as  
21 being more disruptive?

22 A. And in general, some would be more disruptive  
23 than others, and I believe we have a demonstrative to  
24 show.

25 And in this instance, all of the alternatives

1 would produce parts that would be incompatible with  
2 JEDEC-compliant systems of today. But perhaps the  
3 least disruptive of these would be the number 5,  
4 doubling the clock frequency.

5 Q. Why do you say that that would be the least  
6 disruptive?

7 A. Because it wouldn't require additional number  
8 of pins. It wouldn't require additional hardware or  
9 additional -- or changes to the I/O driver  
10 definitions.

11 Q. What would be the -- or what, if any, would be  
12 the redesign implications of switching to alternative  
13 number 5, doubling the clock frequency, today in place  
14 of use of the dual-edged clock?

15 A. One would need to change the memory  
16 controller.

17 Q. Why is that?

18 A. To use a different clock frequency, to use a  
19 higher clock frequency, as well as using a different  
20 clock chip on the motherboard to provide a higher  
21 rate.

22 Q. In other words, you're saying that the memory  
23 controller and the clock chip today would not function  
24 with a faster single-edged clock?

25 A. Correct.

1           Q. Now, in general terms, how would the redesign  
2 implications of alternatives 1, 2, 3, 4 or 6 of DX-108  
3 compare with the redesign implications of number 5,  
4 doubling the clock frequency?

5           A. They would be at least as extensive changes.  
6 Some would require more pins. It would require changes  
7 to the module. They would require changes to the  
8 motherboard, changes to the driver designs. So the  
9 changes would be at least as extensive.

10          Q. Now, what, if any, would be the difference  
11 between making a change today to replace dual-edged  
12 clocking with one of the alternatives listed in DX-108  
13 as opposed to JEDEC having selected a different method  
14 of clocking before the DDR SDRAM standard method

1 morning.

2 We've pulled up DX-94, listing the five  
3 alternatives that you identified to on-chip DLL.

4 Now, with respect to the five alternatives  
5 listed on DX-94, again, did you consider whether some  
6 of these alternatives would be more disruptive than  
7 others?

8 A. Yes, I did.

9 Q. And could you please identify which  
10 alternatives would be more disruptive.

11 A. And again, some would produce parts that would  
12 be incompatible with JEDEC-compliant systems and some  
13 would produce parts that may or may not be incompatible  
14 with JEDEC-compliant systems, and I believe we have a  
15 demonstrative to show.

16 So those highlighted in red, alternatives 1, 2,  
17 3 and 4, would produce parts that are incompatible with  
18 existing systems, and alternative 5 would produce a  
19 part that may or may not be incompatible with existing  
20 JEDEC-compliant systems, and it would depend upon the  
21 system in question.

22 Q. Let the record reflect that Professor Jacob was  
23 referring to a demonstrative that will be marked as  
24 DX-109 with the caption Alternatives to On-Chip  
25 PLL/DLL --



1 JUDGE McGUIRE: Is it 109 or is it 108?

2 MR. OLIVER: Your Honor, I believe 108 was the  
3 alternatives to dual-edged clocking.

4 JUDGE McGUIRE: Okay. Very good.

5 BY MR. OLIVER:

6 Q. Now, Professor Jacob, perhaps you could explain  
7 in a bit more detail what, if any, would be the  
8 potential redesign implications today of the least  
9 disruptive of the alternatives you have identified,  
10 relying on the DQS data strobe to provide timing.

11 A. What this means is one would disable the DLL  
12 or eliminate the DLL and expect the memory controller  
13 to use DQS to latch the data upon a DRAM read rather  
14 than being able to use the global clock to latch the  
15 data.

16 So in a system that already uses the DQS data  
17 strobe and disables DLL -- for example, many graphics  
18 applications do this -- then this would require no  
19 changes. This would be perfectly compatible. But in  
20 any system that expects the DRAM to be in sync with the  
21 global clock, this would fail to be compatible.

22 Q. Now, in general terms, how would the redesign  
23 implications of the alternatives 1 through 4  
24 highlighted in the red box compare with the redesign  
25 implications of relying on the DQS data strobe to

1 provide timing?

2 A. In general, they would be at least as -- the  
3 changes would be at least as extensive.

4 Q. Now, what, if any, would be the difference  
5 between changing today to one of the alternatives that  
6 you have identified to replace on-chip DLL as opposed  
7 to JEDEC having selected a different method to capture  
8 data at the memory controller before the DDR SDRAM  
9 standard were finalized?

10 A. Again, these are straightforward engineering  
11 techniques, and had they been designed in from the  
12 beginning, it would have been a very straightforward  
13 thing to do as opposed to trying to retrofit them into  
14 existing infrastructure today.

15 Q. Now, we've looked at the redesign implications  
16 with respect to each of the technologies at issue  
17 individually.

18 How would you describe the redesign  
19 implications, if any, if one were to try to replace all  
20 four of these technologies at once?

21 A. Well, as shown, each of the technologies has a  
22 number of alternatives and some of the alternatives  
23 would produce parts that, you know, may or may not be  
24 compatible and some alternatives produce parts that are  
25 clearly incompatible. If one were to replace all of

1 the technologies in dispute with one of the  
2 alternatives, you would produce a DRAM part that would  
3 fail to be compatible with any existing JEDEC-compliant  
4 system.

5 Q. And again, what, if any, would be the  
6 difference between making a change today to replace  
7 all four of the technologies at issue as opposed to  
8 JEDEC having selected different technologies at the  
9 time that JEDEC was forming the SDRAM and DDR SDRAM  
10 standards?

11 A. Again, today the changes would be more  
12 disruptive because it would cause engineers to have to  
13 throw away designs. You wouldn't be able to reuse  
14 existing designs. Future designs would need be to  
15 redesigned from scratch. Designs that are in current  
16 process might have to be restarted and which would  
17 cause slippage of schedules. As opposed to if any of  
18 these had been -- or if all of these technologies had  
19 been replaced with alternatives in the beginning, none  
20 of this would happen.

21 MR. OLIVER: Your Honor, I have no further  
22 questions of the witness at this time.

23 JUDGE McGUIRE: Okay. Thank you very much,  
24 Mr. Oliver.

25 Counsel, it's 5:00, so I suggest we go ahead

1 for the day and break and we'll reconvene here on  
2 Tuesday morning at 9:30. Okay?

3 This hearing is in recess.

4 (DX Exhibit Numbers 95 through 99 and 104  
5 through 109 were marked for identification.)

6 (Time noted: 5:02 p.m.)

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1 C E R T I F I C A T I O N O F R E P O R T E R

2 DOCKET NUMBER: 9302

3 CASE TITLE: RAMBUS, INC.

4 DATE: June 16, 2003

5

6 I HEREBY CERTIFY that the transcript contained  
7 herein is a full and accurate transcript of the notes  
8 taken by me at the hearing on the above cause before  
9 the FEDERAL TRADE COMMISSION to the best of my  
10 knowledge and belief.

11

12 DATED: June 16, 2003

13

14

15

16 JOSETT F. HALL, RMR-CRR

17

18 C E R T I F I C A T I O N O F P R O O F R E A D E R

19

20 I HEREBY CERTIFY that I proofread the  
21 transcript for accuracy in spelling, hyphenation,  
22 punctuation and format.

23

24

25

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