FEDERAL TRADE COMMISSION

I N D E X (PUBLIC RECORD)

UNITED STATES OF AMERICA

FEDERAL TRADE COMMISSION

In the Matter of:	)	
Rambus, Inc.	)	Docket No. 9302
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Monday, July 21, 2003

9:30 a.m.

TRIAL VOLUME 46

PART 1

PUBLIC RECORD

BEFORE THE HONORABLE STEPHEN J. McGUIRE

Chief Administrative Law Judge

Federal Trade Commission

600 Pennsylvania Avenue, N.W.

Washington, D.C.

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P R O C E E D I N G S

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JUDGE McGUIRE: This hearing is now in order.

Counsel, how is everyone doing this morning?

Before we get started, are there any items we need to take up?

MR. PERRY: Yes, Your Honor. We wanted to let you know that we will complete our case next Tuesday afternoon, the 29th.

JUDGE McGUIRE: Okay.

MR. PERRY: And Your Honor, there may well be issues with respect to what they want to do in the rebuttal case as to whether it's fair rebuttal.

JUDGE McGUIRE: Right. I suggest you two, each side confer in the interim on that, and at whatever time that we might engage in that, how much time does complaint counsel anticipate it's going to take to put on their rebuttal case?

MR. OLIVER: Again, I'm not certain at this point, Your Honor, but I think it would be less than a week.

JUDGE McGUIRE: It would be less than a week, okay.

MR. OLIVER: Your Honor, could I have one moment to consult with counsel here?

JUDGE McGUIRE: Yes, go ahead.

(Counsel conferring.)

MR. OLIVER: Your Honor, we also received notice today that Mr. Teece is going to be their witness for Thursday and Friday. I just wanted to mention for Your Honor's information that Mr. Royall was scheduled to handle Mr. Rapp as well as Mr. Teece, and Mr. Royall unfortunately has been ill and was in the hospital yesterday, and I believe that he was planning to try to nevertheless go forward with Mr.

Rapp tomorrow, but in light of his condition, I frankly don't know at this point whether he would be in a position to continue with Mr. Teece later this week. I will speak with him this morning or at the lunch break.

JUDGE McGUIRE: Yeah, I will hold that in abeyance, and I guess -- when you say sometime next week, do you mean sometime before their case in chief being --

MR. OLIVER: No, I simply said because of Mr. Royall's illness and the fact that he was in the hospital yesterday and the fact that I don't know exactly what his condition is today, that we are hoping he would be in condition to go forward with Mr. Rapp tomorrow.

JUDGE McGUIRE: Okay, I got you.

MR. OLIVER: But at this point, we don't know whether he will be able to go forward with Mr. Teece Thursday and Friday.

MR. PERRY: I'm not quite sure what Mr. Oliver is suggesting, whether there would be somebody else to examine the witness or whether we should stop our case at this point, and I don't know that we should do the latter. I know that people have travel plans.

JUDGE McGUIRE: Well, I am not going to stop the case on that.

Do you want to respond to that further, Mr. Oliver? Are you saying if he is not out of the hospital by the time they put on this witness, I guess you should follow up and give us a little more input on what your alternative would be if he's unable to conduct that cross examination.

MR. OLIVER: Well, he is out of the hospital, Your Honor, but I do want to consult with Mr. Royall as well as with the other side to see what arrangement we might be able to make.

JUDGE McGUIRE: And you will do that, what, today?

MR. OLIVER: Yes.

JUDGE McGUIRE: All right, very good.

All right, if there are no other items to come before the Court at this time, the respondent may call its next witness.

MR. DETRE: Thank you, Your Honor. Respondent calls Michael Geilhufe.

JUDGE McGUIRE: Sir, would you please approach the Bench and be sworn in by the court reporter.

Whereupon--

MICHAEL GEILHUFE

a witness, called for examination, having been first duly sworn, was examined and testified as follows:

JUDGE McGUIRE: Have a seat right there, Mr. Geilhufe.

THE WITNESS: Thank you, Your Honor.

DIRECT EXAMINATION

BY MR. DETRE:

Q. Good morning, Mr. Geilhufe.

A. Good morning.

Q. Could you please state your full name for the record?

A. Michael Geilhufe.

Q. And how do you spell that last name?

A. G E I L H U F E.

Q. And where do you live, Mr. Geilhufe?

A. I live in Palo Alto, California.

Q. How long have you lived there?

A. I've lived in Palo Alto for seven years; in the Bay Area for 35 years.

Q. Are you presently employed?

A. I am formally retired. I am very active in private business matters.

Q. What sort of private business matters are you involved in?

A. I'm a serial entrepreneur. I'm an investor in a number of young startup companies. I am involved in funding or identifying funding for young startup

companies. I am on the board of a semiconductor memory company. And I'm on the board of advisers for two other companies.

Q. Prior to this matter, have you ever been an expert witness before?

A. No, I have not.

Q. If we could step back a little bit, could you give a brief summary of your educational background, starting with your undergraduate degree?

A. My Bachelor's Degree in electrical engineering is from the University of California at Berkeley.

Q. What year is that?

A. And that was in the year 1965, a long time ago. And my major was computer science and semiconductor devices.

Q. And did you get any further degrees after that?

A. Yes, I then received a Master's in electrical engineering and semiconductor devices from California State University at Long Beach in 1967.

Q. And did you get any further degrees after that?

A. Yes, I received a Master's of business administration from the University of Santa Clara, specializing in entrepreneurship.

Q. Do you recall what year that was?

A. That was in 1971.

Q. When did you get your first full-time job?
A. In 1965.
Q. Where did you work?
A. I worked for Collins Radio in Newport Beach, California.
Q. And what did you do there?
A. I was a research engineer in the microelectronics research operation for Collins Radio.
Q. And how long were you at Collins?
A. I was there for two years.
Q. What did you do after that?
A. After that, I joined Lockheed Missile and Space Company in Sunnyvale, California.
Q. And what did you do at Lockheed?
A. I worked as a microelectronics research engineer at Lockheed. I worked on some parts for the Poseidon Missile, and I did the first integrated circuit at Lockheed.
Q. And after -- how long were you at Lockheed?
A. Approximately two years.
Q. What did you do after that?
A. After that, I joined a startup company called Advanced Memory Systems in Sunnyvale, California. I was responsible for memory product design.
Q. And how long were you at Advanced Memory

Systems?

A. I was at Advanced Memory Systems approximately four years.

Q. So, during what period of time was that?

A. Approximately 1968 to '72.

Q. And could you give a little bit more detail about what sort of projects you were involved in at Advanced Memory Systems?

A. Yes, Advanced Memory Systems was founded as a semiconductor memory company. It was founded at the same time as Intel, the two companies that had attempted to build semiconductor memories. That technology did not exist before 1968.

Q. And what specific projects were you involved in at Advanced Memory Systems?

A. I designed the first commercial DRAM, a P-channel DRAM. I then designed a number of other products that were successful in the marketplace, DRAM products.

Q. Okay. And what did you do after you left Advanced Memory Systems?

A. I was recruited to Intel in 1972, early '73, to take over the memory development responsibility for Intel Corporation.

Q. And during what period of time were you

employed at Intel?

A. I was employed -- I was formally employed between 1973 to 1988. There was a one-year sabbatical in there.

Q. When you first started with Intel in 1973, what were your job responsibilities?

A. I was -- I was responsible for developing all semiconductor memory products at Intel, specifically the 4K DRAM at that time.

In addition to that, I was responsible for developing DRAM products -- excuse me, SRAM products, bipolar memory products, peripheral products and -- and two years later, nonvolatile memory products.

Q. And at some point did your job responsibilities at Intel change?

A. Yes.

Q. When was that?

A. I was moved to a corporate responsibility in the 1978 time frame, I believe, corporate responsibility for reliability engineering.

JUDGE McGUIRE: Now, let me just inject. I'm hearing what you did, but I haven't heard your titles in these various jobs, sir, if you might just throw that in for the record so I'll know what titles you had during this period.

THE WITNESS: All right, sir, okay.

BY MR. DETRE:

Q. During that first period of time at Intel when you were designing DRAM and memory products, what was your title then?

A. My title was memory development manager, and at Intel, that was the senior development position at that time.

Q. Okay, then I believe you testified that at some point you became responsible for reliability at Intel, and what was your title at that point?

A. That title was director of reliability engineering.

Q. And could you give a little bit of further detail about what your responsibilities entailed in that position?

A. Yes, as -- I was responsible for the design reliability, process reliability and manufacturing reliability of all Intel products at all factories of Intel.

Q. And what sort of products did that involve?

A. That, of course, included DRAMs, SRAMs, EPROMs, microcontrollers, microprocessors, peripheral chips, literally the entire product suite.

Q. And then at some time did you assume another

position at Intel?

A. Yes, I then assumed the position of director of quality -- worldwide quality assurance, and that added to the reliability responsibility the quality assurance responsibility.

Q. When were you in that position?

A. I was in that position in 1980 and '81.

Q. Okay. And did your responsibilities -- how did your responsibilities change when you assumed that position?

A. The staff size grew significantly. At that point I had a 600-person staff around the world, and several manufacturing plants were added to my responsibility.

Q. And what did you do at Intel after 1981?

A. I went on sabbatical. I went on a sailing trip.

Q. How long did your sabbatical last?

A. Approximately 11 months.

Q. And did you then return to Intel?

A. That is correct.

Q. And what was your position when you returned to Intel?

A. I returned to Intel as director of systems quality and reliability.

Q. And were your responsibilities in that position different from your prior responsibilities at Intel?

A. Exactly. My prior responsibilities were components-related responsibilities. The systems responsibilities related to motherboards, memory systems, development systems, systems similar to today's PCs.

Q. Okay. Did those systems involve DRAMs?

A. Of course.

Q. How long were you in that position?

A. Approximately two years.

Q. And what did you -- what position did you assume after that?

A. I was then -- I moved to the position of general manager and director of components contracting.

Q. And during what years were you in that position?

A. Approximately '84 to '87-'88.

Q. And what were your -- what were your responsibilities in that position?

A. My responsibility was to establish, negotiate and manage international manufacturing operations for Intel; that is, manufacturing operations under contract in Japan, in Korea, in the United States and in Taiwan.

Q. What sort of products were being manufactured

for Intel under contract?

A. Generally the low cost products, microcontrollers of memory -- EPROMs and DRAMs.

Q. And could you give some idea of what sort of companies you were interacting with during this period?

A. Yes. In Japan, I worked closely with Mitsubishi, with Sanyo, with OKI -- these are all the semiconductor divisions of those very large companies -- Rohlm. In Korea, I worked very closely with Samsung, and in Taiwan, I worked very closely with TSIC.

Q. And did you then assume some further position at Intel after that?

A. I also handled business development activities towards the end of that particular tenure. One of the businesses I established was a DRAM distribution business.

Q. Okay. And what had -- and erther yDRAM dis1 8Fmem

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A. Yes, I did.

Q. For how long?

A. I worked at Information Storage Devices through 1998.

Q. What sort of technology was Information Storage Devices developing?

A. The company developed a unique multi-level storage technology that is a technology where one memory cell can store more than one bit of information, in our case eight bits.

Q. Did any of your work at Information Storage Devices involve DRAMs?

A. It -- DRAM involvement was -- well, let me back up.

Information Storage Devices was a fabless semiconductor company. As such, we contracted with companies to manufacture our products. Our products were being fabricated in one case in a DRAM fab.

Q. And you became familiar with that DRAM fab?

A. Intimately familiar.

Q. What did you do after your tenure at Information Storage Devices?

A. Information Storage Devices as a public company was sold to Winbond Electronics, a Taiwanese company, and I continued as a vice president for that company,

vice president of -- and general manager of the operation for that company for a year and a half.

Q. I'm sorry, what was that company?

A. Winbond, W I N B O N D.

Q. And what sort of business was Winbond in?

A. Winbond is in the consumer electronics component business. The largest part of its business is DRAMs.

Q. And what did you do after Winbond?

A. After Winbond, I began investing in young startup companies. Specifically, I invested in Advanced Radio Sales, and shortly after I invested, I was asked to become chairman of the company, executive chairman of the company, and I operated in that mode until the company was merged about a month ago.

Q. Okay. Now, over the course of your career, have you --

JUDGE McGUIRE: Be we get started, I want to clarify something. You had introduced him when you called him as doctor, but I don't believe you went into --

THE REPORTER: No, that was my error.

JUDGE McGUIRE: I was going to say, you didn't inquire about his Ph.D. or anything.

MR. DETRE: No, I am not aware that Mr.

Geilhufe has a Ph.D.

proposed or my organization proposed. Certainly during the Intel days, I had to do cost estimation for all the contracts that I negotiated, and these are very, very large contracts. The Samsung contract was greater than a billion dollars. So, we had to do very careful, very thorough cost estimations for those contracts.

We had to do very careful tracking of costs. In other words, we not only estimated the costs, but we were able to then see what the actual costs were during the components contracting operations.

And of course, at ISD, everything continued in the same vein except on a smaller scale.

Q. ISD being Information Storage Devices?

A. Information Storage Devices, yes.

Q. Did any of your experience give you any insight into the cost structures of DRAM manufacturers?

A. Clearly. Not only did I have the experience of Intel's DRAM manufacturing in the very -- in the early years, but as manager of -- as director of components contracting, I had the opportunity to evaluate -- visit, evaluate and gather data at the various DRAM factories that we were using for contract manufacturing.

MR. DETRE: Your Honor, at this time we tender Mr. Geilhufe as an expert in semiconductor design and

manufacturing, including manufacturing costs.

JUDGE McGUIRE: Any objection?

MR. DAVIS: No objection, Your Honor.

JUDGE McGUIRE: All right, so qualified.

MR. DETRE: Thank you.

JUDGE McGUIRE: I just want to get that clear again, he's being offered as an expert in --

MR. DETRE: Semiconductor design and manufacturing, including manufacturing costs.

JUDGE McGUIRE: Okay.

BY MR. DETRE:

Q. Mr. Geilhufe, in this case we've heard a fair amount about four features of DRAM technologies, programmable latency, variable burst length, dual edge clocking and on-chip DLL.

Are you familiar with those technologies?

A. I'm familiar with the terms and the concepts, yes.

Q. Okay, let me show you a document.

May I approach, Your Honor?

JUDGE McGUIRE: Yes.

BY MR. DETRE:

Q. Mr. Geilhufe, I've handed you a document marked as CX-1454.

A. Yes.

Q. Let me just wait for it to come up on the screen. There we go.

Have you seen this document before?

A. Yes, I have.

Q. Have you reviewed it?

A. Yes, I have.

Q. I'll just note for the record that it's a document that we've been identifying in this case as either the PCT or the WIPO application that Rambus filed in 1991.

In your review of the PCT application, Mr. Geilhufe, did you reach an opinion as to whether all four of those features, programmable latency, variable burst length, dual edge clocking and on-chip DLL, are disclosed in this application?

A. I reached an opinion that certainly a -- an experienced designer or an experienced design manager would be concerned that those features are, indeed, described in the PCT application.

Q. And when you say a designer, are you talking about a DRAM designer?

A. Excuse me, a DRAM designer or a DRAM design manager.

Q. Have you reached an opinion as to whether those features, as described in this application, CX-1454,

Q. If you were working on designing an SDRAM incorporating programmable latency and burst length and came across the PCT application, what would you have done?

A. If I were the -- if I were in the role of the experienced designer, first of all, a caution flag would go up. I would -- I would study that topic to some extent, and I would then take my concern that the analysis would raise to my management and my peers for further analysis.

Q. And you've been in the role of a manager also, haven't you, Mr. Geilhufe?

A. Absolutely.

Q. If one of your designers had brought these concerns to you as a manager, what would you have done?

A. As a responsible manager, recognizing that we're dealing with a very, very large economic impact issue -- that is, if a DRAM design infringes a patent or potentially infringes a patent, it could use huge economic losses to the company -- as a responsible manager, I would then gather additional technical analysis from specialis0on 22gato3nalnen e3ehe areable

came back and said the concern has some validity, I would then take the issue to corporate counsel, corporate IP counsel or out-house -- outside IP counsel and get a careful review.

Q. Now, in your opinion, would an experienced DRAM designer reviewing this application, CX-1454, have believed that any IP -- any patent claims Rambus could get from this application would be limited to a particular bus architecture?

A. Not -- not an experienced designer. Experienced designers having some knowledge of intellectual property recognize that a particular -- let's say a circuit in a particular patent cannot be used in some other patents.

A very good example, one of my patents was used in a totally different application and collected huge royalties for that application.

Q. Okay. Well, let me -- we can put this document aside.

These four features that we have now introduced -- and I won't repeat them each time -- in what part of DRAM are these four features implemented?

A. These are control features. They are the peripheral circuitry. They are not the memory part of the circuitry but the peripheral part of the circuitry.

Q. And could you explain in a little bit more detail the difference between the -- what you call the memory part of the circuitry and the peripheral circuitry?

peripheral circuitry?

A. Yes. The memory arrays development includes device and cell development, process development and a lot of equipment development. That is the vast majority of the development cost. Hundreds of millions of dollars can be spent in that particular domain.

The development costs for the peripheral logic can indeed be significantly -- much, much lower, because there is no process development involved whatsoever.

Q. And if you could just briefly describe what you mean by "process development."

A. Process development is the manufacturing process that a silicon wafer undergoes, as many as 400 or 500 steps, distinct steps, including high-temperature processing, photo processing, those -- that is what is called the process, the manufacturing process.

Q. Now, Mr. Geilhufe, have we asked you to estimate the cost impacts of some of the alternatives to these four features we've been discussing that have been proposed by complaint counsel's technical expert, Professor Jacob?

A. Yes, you have.

Q. And have you made those estimates?

A. I have made those estimates, yes.

Q. Now, in making these estimates of the cost

Q. And --

A. And the requirement for that, of course, is to run a 20 million unit volume, you need to be well down the learning curve.

Q. Now, if you had not made this assumption about being well down the learning curve, would your cost estimates have been different?

A. They would have been much, much larger, because the cost -- the base costs would have been much larger.

MR. DETRE: Your Honor, we're going to be using a few demonstratives with Mr. Geilhufe. May I hand a set up?

JUDGE McGUIRE: Yes, you may. Do we have those already marked?

MR. DETRE: Yes, we do. And I'll also hand a set to Mr. Geilhufe.

JUDGE McGUIRE: Go ahead. You have one for opposing counsel, I assume.

MR. DETRE: I do. And we have, as I mentioned, premarked these with DX numbers, and if we could pull up the first one, DX-298, please, starting with the heading Cost Effect of CAS Latency Alternatives.

(DX Exhibit Numbers 298-301 were marked for identification.)

BY MR. DETRE:

Q. Mr. Geilhufe, does this chart summarize your opinions about the cost effects of certain alternatives to programmable CAS latency proposed by Professor Jacob?

A. Yes, it does.

Q. Did you assume any particular time frame when making these estimates?

A. The estimates for this -- excuse me, the time frame for this estimate was in mid-1995.

Q. Okay. And do you have some understanding of what the total unit cost of a DRAM was in that time frame?

A. The mature, first-tier total unit cost was approximately $2, and that is what I used as my model.

Q. Now, if we look at the very top row of this chart, there are a number of headings, Process & Storage Cell/Array, Product Design and so forth.

Do you see that?

A. Yes, I do.

Q. What do these headings represent?

A. Those headings represent cost elements that I looked at in detail that are involved in a DRAM.

Q. And if we look down the very first column where

A. That column lists the five alternatives that I evaluated for CAS latency.

particular alternative, and that's what the "f" means.

Q. Now, over the course of your career, have you had the occasion to make cost estimates involving process and storage cell/array costs?

A. Yes, I have.

Q. Can you explain when that's come up?

A. The last one was at a 64K DRAM in the 1988 time frame.

Q. And if we could move on to the next column, Product Design, could you explain what comes under that heading?

A. Yes, this is the manpower required, the computer time required, the simulations required to go ahead and create a particular alternative.

Q. And there's an "f" after that one also.

A. Right, that is a one-time cost, and it would get amortized over the entire population that gets built.

Q. And again, over the course of your career, have you made cost estimates involving product design costs?

A. Yes. The design estimates I've made throughout my career, the last one I believe was in 1998 or '97.

Q. If we go to the next column, Wafer Plant, could you please explain what wafer plant costs involve?

A. Here I was trying to analyze whether new

equipment was required in the wafer factory to support the alternative.

Q. Okay. And is that a fixed cost also?

A. Exactly. That would be a one-time cost.

Q. Have you made cost estimates involving this cost factor in your career?

A. I have evaluated manufacturing -- excuse me, plant costs throughout the world through the entirety of my career, yes.

Q. The next column is Photo Tooling. Could you please explain that?

A. To process a silicon wafer requires reticles or photo tools, and this is the one-time cost that is required to create the tool for that particular alternative.

Q. Now, you mentioned reticles. In this case we've sometimes heard the term "masks." Is there some relationship between masks and reticles?

A. Yes, the mask term is -- us old guys use mask terms, the term "mask." That's what it was 20 years ago. "Reticle" is the much more refined, much more sophisticated term.

Q. And is that also a fixed cost?

A. That is a one-time cost for the population.

Q. Have you made cost estimates involving this

factor during your career?

A. I have not only made cost estimates, but I've purchased photo tooling throughout my career, and as -- I -- the company on whose board I sit, one of the key elements is photo tool costs for their products.

Q. The next column is Wafer Sort. Could you please explain what you mean by wafer sort?

A. Yes. Once a wafer is processed -- unfortunately, in the semiconductor industry, we don't build good units. We build lots of units, and then we decide a good die or we separate a good die from a bad die.

Wafer sort is the electrical test operation that identifies the good die on a wafer and rejects the bad die on a wafer.

Q. And under -- under Wafer Sort, you have a "v" in parentheses. Could you explain what that means?

A. Yes, that cost is really dependent on the number of units that are being processed. So, it is a per-unit cost as opposed to a fixed cost.

Q. What does "v" stand for?

A. Variable.

Q. Have you made cost estimates involving costs related to wafer sort in the course of your career?

A. Yes, throughout my career.

Q. If we go to the next column, Good Die Yield, could you please explain that?

A. Yes, probably the most important parameter in the life of a semiconductor businessman, it really identifies -- if you build a hundred units, do you get 30 good ones or 90 good ones or 99 good ones? The die yield is the percentage of good die versus die built.

Q. And you've identified that as a variable cost?

A. Again, yes, because that is literally -- it changes on a per-unit basis.

Q. Okay. And have you had the occasion to make cost estimates relating to good die yield over the course of your career?

A. Throughout my entire career, throughout -- all the way through ISD, and I also had the opportunity to work many yield improvement programs over the years, which address exactly this issue.

Q. The next column is headed Packaging. Could you please explain what you mean by packaging?

A. Yes, once we have a die and we decide it's a good die in wafer sort or potentially a good die in wafer sort, we take that die and put it through a manufacturing process that attaches leads to that die so that the -- a package can be put on the circuit board.

What do you include under that heading?

A. There are two elements in inventory. One is the work in process element; that is, in a factory, it may take six weeks or eight weeks to complete all the 400 processing steps to create a finished wafer. That means you have work in process inventory sitting in that factory. If it's six weeks worth, you have six weeks worth of inventory. So, I include work in process inventory in fab, I include work in process inventory in the assembly plants.

And the second element of inventory is the finished product inventory; that is, once a product passes final test and is determined as a good unit, it then goes into finished goods inventory at the manufacturers. It may go into inventory in a distribution channel, and it definitely goes into inventory by the user itself. So, we have a complete food chain, if you will, of inventories. And I've attempted to identify that total cost.

Q. Okay. Have you treated that as a fixed cost or a variable cost?

A. I've treated it as a variable cost.

Q. Okay. Now, the next -- oh, excuse me, I almost forgot one of my questions.

Have you made cost estimates relating to

qualifies the particular line item, the particular product code.

Q. Have you made cost estimates relating to qualification during your career?

A. Of course. I've not only made cost estimates, but I've ran a large number of qualifications when I was responsible for that function.

Q. And then finally, the last factor listed is Board Complexity. Please explain what that means.

A. Yes, we're now out of the realm of the DRAM manufacturer, and we're in the space of the user. So, if we changed a DRAM, for instance, we add more pins to it or something, that may require a larger board area, more real estate on the board, or it may require more traces or some other effect like that, and that is the effect that I was trying to establish with board complexity.

Q. And you've identified that as a variable cost?

A. Yes, that symbol means approximate. Please recognize that this is a model, and all the numbers on the model, by its very nature, have to be approximate.

Q. Now, in making these estimates, have you tried to err on one side or the other?

A. Well, you will find as we go through here that generally I erred on the conservative side; that is, the lower cost increases side.

Q. Okay. So, under Product Design, you have got, "Add approximately 100K --" does K mean thousand?

A. $100,000.

Q. "-- per CAS latency part."

Could you explain why you've assigned $100,000 per CAS latency part under Product Design?

A. Yes, to create a new product requires a number of significant steps during the design effort. The actual design activity may be quite minimal, but it may -- it definitely will require the characterization, simulations work, and a minimum level in my experience in a large company is about $100,000 to do a new line item, new product code.

Q. So, were you assuming that this was going to be a minor design effort or a major design effort or somewhere in between?

A. This is a minor design effort.

Q. If we go to the next non-negligible column under Photo Tooling, you have got, "Add approximately $50,000 per CAS latency part."

Could you explain that?

A. Yes, that is my estimate of the photo tooling cost required.

Q. And what's that estimate based on?

A. That's based on the cost of photo tools today. A photo tool set may cost between a million and a million and a half dollars. This is the time frame

Q. Next, under Good Die Yield, you say, "Reduced yield due to speed distribution."

Could you explain what you mean by "speed distribution"?

A. Yes. The semiconductor manufacturing process produces a distribution of results; that is, for instance, the access time of a hundred chips on a die may vary from 13, 14, 15, 16 nanoseconds. There will be a normal distribution, and that depends on a number of parameters, physical dimensions and what have you.

Q. Now, why would there be a reduced yield due to speed distribution if you went from programmable latency to fixed latency?

A. Pble

the test for the faster part will have some fall-out; that is, there will be die that are functionally working, but they're not fast enough for that particular specification, and they will be rejected.

Q. And what in your estimation would the cost effect be of this reduced yield due to speed distribution?

A. I have estimated that cost to be approximately 3 cents or approximately 1 to lcdlo lcl I havel0vwp dnm4e810ely

Q. Let's move on then to the next row in your chart, CAS latency in Read/Write Command. Could you explain what you mean by that alternative?

A. Yes. There were two versions, I believe, in Dr. -- in Professor Jacob's report, but basically it's to communicate the CAS latency value while the read/write command is issued.

Q. And then under that, you have -- excuse me, the first non-negligible number I see is under Product Design, "Add approximately $100,000."

Could you explain that?

A. That's correct. I assumed a nominal or modest design effort to go ahead and create that product.

Q. And under Packaging, it says, "Negligible or add approximately 1 cent for added pin."

Could you explain that?

A. Yes, again, it's sort of the conservative approach that we have. Professor Jacob suggested one pin could be used for that aspect. In the packaging environment, one can't really add just one pin in a dual inline package; you have to add it in pairs. So, in reality, we should be adding two pins or at least the cost associated with two pins. So, I've added a cost of 1 cent if the pin is used.

Q. Okay. And what was your bottom line using

those numbers then on this alternative?

A. I then concluded that the alternative would increase costs from about one-half a cent to as much as 2 cents.

Q. Let's move on then to your next row, which relates to programming CAS latency with fuses.

Do you see that?

A. Yes.

Q. And under Process & Storage Cell/Array, you have, "None if use existing fuse technology."

Can you explain what you mean by that?

A. Yes. Fuse technology is very important in the manufacture of DRAMs, certainly in the '95 time frame and still today. It's a critical element that is used to repair defective parts of the memory array.

In the '95 time frame, the dominant fuse technology used for that purpose -- and by "dominant," I believe all the majors used it at that time -- is laser fuse technology, but I'm assuming here for this analysis is that if a fuse is used, it's a laser fuse, laser-blown fuse.

Q. What other fuse technologies are there other than laser fuses?

developing some products in that space which were discontinued at Intel for reliability reasons, and it's a very simple mechanism. You blow a fuse open, and over time and over operation, it has a tendency to migrate back together. So, it's not quite -- quite satisfactory.

In addition to that, there are anti-fuse technologies, both amorphous and dielectric, also with some fairly peculiar reliability concerns.

Q. What is your understanding of whether such anti-fuse technology was being used in DRAMs in the time frame mid-1990s when you were making these estimates?

A. For the mid-1990s time frame, I believe the major manufacturers were using laser fuses.

Q. Okay. And what is that belief based on?

A. My own personal experience with several of the Japanese and Korean manufacturers. I do not have any personal experience with Micron.

Q. Now, here you say under Process & Storage Cell/Array, "None if use existing fuse technology."

Do you have an opinion about whether there would be a cost associated with the process and storage cell/array factor if a manufacturer that was not using anti-fuses then were to begin using anti-fuse

technology for its fuses?

A. Yes, I do.

Q. What's that opinion?

A. Anti-fuse technology is not generally available in the DRAM process. It requires what's called a metal insulator or metal structure that is not generally available --

JUDGE McGUIRE: Can we go back, and before you go into that, could you explain to the Court what you mean by "anti-fuse technology"?

THE WITNESS: Yes. Fuse technology -- fuse technology is you take a conductor, and just like a fuse at home, you blow it open, and in theory, it stays open. In reality, on an integrated circuit, it has a tendency to try to grow back together at some level.

Anti-fuse technology is the two -- the conductor is isolated, that is, there is no connection, and once you blow that fuse electrically, you create a connection. So, it is the inverse of a fuse.

JUDGE McGUIRE: All right, Mr. Detre.

BY MR. DETRE:

Q. Now, the laser fuses that you were talking about earlier, can you use those either before or after packaging?

A. The laser fuses can only be used at wafer sort,

before packaging.

Q. Okay. And how about anti-fuses?

A. Anti-fuses could potentially -- if they were the right anti-fuses can potentially be blown after packaging.

Q. Okay. And you were I believe explaining what sort of costs might be involved in adding anti-fuse technology if a DRAM manufacturer did not have that available.

A. Yes. If the anti-fuse technology module does not exist in the DRAM process, adding that could be a significant cost, and by "significant," the development of that would be several million dollars in my opinion.

Q. Okay. Now, under the next column, Product Design, with respect to the fuse alternative, you have, "Add approximately $100,000."

Could you explain that?

A. Yes, one would need a new mask set if one wanted to use fuse technology for programming.

Q. Now -- and does that relate to product design?

A. I'm sorry?

Q. I was asking you about the $100,000 figure under Product Design.

A. That is correct.

Q. So, that's designing with the mask set?

A. No, it -- I apologize. I was getting in front of myself.

No, this is purely the design effort to go ahead and provide for the fuses. That's all.

Q. Okay. Now, under Wafer Plant and Photo Tooling, you have, "None if use existing fuse technology."

Q. And why is that?

A. Because again, once the fuse is blown, you have a fixed CAS latency part.

Q. Okay. And could -- and -- excuse me.

What is your opinion of how much cost that would add due to the reduced yield?

A. Approximately 3 cents.

Q. Three cents per unit?

A. Per unit, excuse me, yes.

Q. The next non-negligible cost you had was under Inventory, "Three parts add approximately 2 cents per unit."

Could you explain that?

A. Again, it's identical to a fixed CAS latency. At this point, we have fixed CAS latency parts, so it is the same as -- inventory cost as if we had built fixed CAS latency parts from scratch.

Q. Now, if I could stop here at inventory for a second, you have estimated approximately 2 cents per unit. Do you know of any actual cases involving inventory problems and associated costs?

A. Well, the DRAM industry is an interesting industry because of the cost reductions that take place in the industry over a relatively short time period. A 64-meg DRAM in 1994 may be $40 or $50 in cost, and 12

Q. This Apple loss of $27 million, do you know how that relates to -- if we were looking at that on the per-unit basis, how that relates to your estimate here of approximately 2 cents per unit?

A. Well, for Apple, it was probably a $5 or $6 per unit loss.

Q. Are you familiar, Mr. Geilhufe, with the term "speed binning"?

A. Of course.

Q. Could you explain what you understand that to mean?

A. Again, the manufacturing process turns out a distribution of performance; that is, access time of various levels. Speed binning is the testing process that says, yes, my part is faster than 15 nanoseconds, that's maybe bin one; my part is faster than 18 nanoseconds, between 15 and 18, that's a bin two; and an 18 to 25, that's a bin three. That's what I understand to be speed binning.

Q. Okay. And that's something that DRAM manufacturers do?

A. Absolutely.

Q. Now, does the fact that DRAM manufacturers do this sort of speed binning, does that have any effect on inventory costs and having multiple parts?

A. Not -- not really. Consider that the slower part gets sold for a much lower price than the faster part, so the faster part carries a large premium over the slower part. So, I did not estimate or I did not include speed binning as an alternative, because it's too minor of a factor.

Q. Okay. Now, the next non-negligible item under Program CAS Latency With Fuses is under Qualification, you have, "Add approximately $250,000 per CAS latency part."

Could you explain that?

A. Yeah, again, at this stage, we have fixed CAS latency parts. Each part needs to be qualified.

Q. And could you then tell me what your bottom line is on what the cost effect would be of going to the programmable CAS latency with fuses alternative?

A. The alternative I modeled here is approximately 7 cents cost increase.

Q. And that, again, combines the variable costs with the fixed costs the way you described before?

A. That is correct.

Q. Okay. If we go to the next alternative, CAS Latency Via Pins, do you see that?

A. Yes, I do.

Q. What's your understanding of that alternative?

A. The alternative is CAS latency is programmed with three bits in the program register, so we would have to provide three pins -- excuse me -- yes, we would have to provide three pins. Pins are added in a dual inline package in pairs of two. So, to add three pins would in reality require four pins.

Q. Okay. And then the first non-negligible entry you have there is under Packaging. Could you explain what your opinion is about how much this alternative would add to the packaging costs?

A. If we were to add four pins to the package, I modeled that as an increase of 4 cents. Again, one should recognize that that's a very conservative estimate. If we look at the JEDEC spec, the JEDEC spec generates -- moves from a 44-pin package, not to a 46 or 48 for its next generation, but to a 54-pin package. So, in other words, the JEDEC spec goes and adds ten pins for the next generation. And then it actually moves to a 66-pin package, adding 12 pins. So, it adds it in larger increments. I modeled just adding the four pins here.

Q. Okay. And then under Board Complexity, you say, "May need different connector."

What do you mean by a connector?

A. If we put four more pins on the memory and the

memory is on a DIMM, then now we need those four lines to go from the DIMM to the motherboard. If those four pins are no longer available on the connector, we may need a larger connector there, and that may increase that cost somewhat.

Q. Okay. Are there any other changes to the system that you would need in order to -- if you added four pins to the DRAM?

A. Of course. The controller would have to be modified, and I did not model that cost.

Q. Would you need more pins on the controller?

A. Of -- you would need more pins, and you would need a change in functionality.

Q. Okay. And would you need any other changes to the board?

A. And the board would have to -- the bus on the board would have to be increased by at least four.

Q. And so without adding any additional costs, then, that might have come from the controller or the board, what is your bottom line there on the

Q. Okay. Then if we could go to the last line on this chart, No CAS Latency Asynchronous DRAM, can you explain what you understand by that alternative?

A. Yes. Certainly in the early nineties, asynchronous DRAM was the standard way of producing DRAM, EDO DRAM, what have you, and if no CAS latency -- no programmable CAS latency is required, we would reduce the test time, and that would be the only effect.

Q. And how much do you think the test time would be reduced?

A. I believe the test time would be reduced by approximately -- would -- the cost for test time would go down by approximately 1 cent.

Q. Okay. So, what then is your bottom line on that alternative of asynchronous DRAM?

(A brief recess was taken.)

JUDGE McGUIRE: You may proceed at this time, Mr. Detre.

MR. DETRE: Thank you, Your Honor.

BY MR. DETRE:

Q. Could we pull up DX-299?

Mr. Geilhufe, does this chart summarize your opinions about the cost effect of certain of the alternatives to programmable burst length proposed by Professor Jacob?

A. Yes, it does.

Q. Okay. Now, I -- did you assume any particular time frame when making these cost effect estimates?

A. Yes, I assumed the mid-1990s time frame, 1995 approximately.

Q. Now, I will note that there are fewer factors listed on the top row of this chart than on the previous chart going to programmable CAS latency. Could you explain why that is?

A. Yeah, for clarity, we -- I removed the columns that were negligible through all the alternatives so that we would have a somewhat simpler chart here, still fairly complicated though.

Q. Okay. If we could go to the first row, then, relating to the fixed burst length alternative, could

you explain what you understand by that alternative?

A. Yes, that is -- the read command would ask for a fixed burst length as opposed to a programmable burst length.

Q. And if we look, then, at the first non-negligible entry under Product Design, "Add approximately $100,000 per burst length part," could you explain that?

A. Certainly. You will find that fixed burst length is identical to fixed CAS latency. It has exactly the same characteristics. So, the $100,000 is a design effort for each part type.

Q. Okay. And then the next entry under Photo Tooling, "Add approximately $50,000 per burst length part," could you explain that?

A. Since the parts are different, each part needs a photo tool.

Q. And then under Wafer Sort, "Decreased test time," could you explain why there would be decreased test time?

A. Very much the same as for CAS latency; that is, if you only need to test for a -- for one burst length, that shortens the test time, and I assumed that would improve the cost by a penny, approximately a penny.

Q. And the next, under Inventory, you say, "Four

parts."

Why have you assumed that there were four parts?

A. The JEDEC spec calls for four parts.

Q. And what's your cost estimate of how much having four parts would add to inventory costs?

A. Inventory costs increase by the number of parts, and I modeled this particular level of inventory -- excuse me, line item increases increase the inventory costs, and I modeled for four different

before, by averaging the fixed costs over 20 million parts?

A. Over 20 million units, that is correct.

Q. If we could go then to the next row, Burst

if use existing fuse technology."

Could you explain that?

A. Again, just as for the CAS latency alternative, this assumes using laser-blown fuses.

corresponding number for CAS latency?

A. It is.

Q. What, then, is your bottom line for the alternative of programmable burst length with fuses?

A. I modeled this as a cost increase of approximately 5 cents.

Q. If we could then move to the next alternative, Fixing Burst Length With Terminate Command, do you see that?

A. I do.

Q. What is your understanding of that alternative?

A. It's -- I apologize. That is to program or -- excuse me, to supply the -- to not have any burst length command at all, but to terminate the burst operation with a burst terminate command.

Q. Okay. And you have under Product Design, "Add approximately $200,000."

Could you explain that?

A. Yes, I considered that the design effort would be considerably more complicated, and quite frankly, it may not even be possible to do a burst length of one with a terminate command, is just not possible.

Q. Could you explain why not?

A. Because a read command is issued or a write command, it takes one cycle to execute before a burst

terminate command could be encountered, and at that point, you already have two bits of data coming out.

Q. What, then, in terms of cost anyway, if it were technically feasible, what would the cost increase be of this alternative?

A. I modeled this cost increase purely as a design cost increase at approximately 1 cent.

Q. If we could go then to the next alternative, Burst Length Via Pins, is -- is your understanding of how this alternative works similar to your understanding of how you would set CAS latency via pins?

A. That is correct. Again, we would need three bits of information.

Q. Okay. Under Packaging, you say, "Add approximately 2 cents per unit."

Could you explain how you arrived at that figure?

A. Yeah, again, I used a conservative approach to modeling. Since we had a pin left over -- let me stop.

My assumption is that if pins are being used to program burst length, then they would also be used for programming CAS latency. We've already used four pins for CAS latency, so I only need two more pins to support the burst length. If the burst length were all

by itself, it would be four pins.

Q. And then under Board Complexity, is your opinion about the changes to the board and controller that would be required similar to your opinion about the corresponding alternative for CAS latency?

A. It is identical, yes.

Q. What, then, is your bottom line on the alternative of setting burst length using pins?

A. I modeled this cost as an increase of approximately 2 cents.

Q. If we could look then at the last row on this chart, Burst-EDO Style Protocol, what's your understanding of that alternative?

A. It's exactly the same as burst asynchronous DRAM in the CAS latency alternative. It's basically -- I apologize. I'm getting in front of myself.

It is to use the asynchronous EDO-style memory.

Q. Okay. And is your opinion about the 1 cent cost decrease in that case similar to your opinion about the alternative of using asynchronous DRAM in the CAS latency alternative?

A. It is the same.

Q. Okay. If I could go back for just one second to the -- we are going to stay on this chart, but if I could go back to the top row, the fixed burst length

alternative, for one second, you had -- you had assumed four parts there, Mr. Geilhufe?

A. That's correct.

Q. And for fixed CAS latency, you had assumed three parts. Is that right?

A. Three parts for the SDRAM.

Q. If you were to go with the fixed CAS latency alternative instead of programmable CAS latency and the fixed burst length alternative instead of programmable burst length and you wanted to allow for all of the possible combinations of CAS latency and burst length allowed for in the JEDEC SDRAM specification, how many total parts would you need?

A. For the SDRAM, you would need 12 parts; that is, three times four. For the DDR RAM, you would need 15 parts. The DDR RAM provides for five CAS latencies.

Q. How would that affect your cost estimates relating to fixed burst length and fixed CAS latency?

A. It would increase the -- well, first -- it would increase the inventory costs dramatically.

Q. Let's then go to DX-300, a chart headed Cost Effect of Dual-Edged Clock Alternatives. Does this chart, Mr. Geilhufe, summarize your opinion as to the

A. It does.

Q. And did you use any particular time frame in making these estimates?

A. Yes, for -- since this is through the DDR RAM, I used the late nineties time frame.

Q. Now, this chart has even fewer cost elements along the top. Could you explain why?

A. Again, the cost elements that were negligible for each of these alternatives were removed, were analyzed but were removed from the chart.

Q. Now, if we could look, then, at the first alternative, Interleave on-chip Memory Banks, two clocks, if -- if JEDEC had chosen this alternative instead of dual edged clocking, what's your opinion of how much that would have added to product design costs?

A. In my opinion, that is a more significant product design effort of the peripheral circuitry, and it would add approximately $250,000 to implement that solution.

Q. Okay. And why is it a -- do you think it's a more sophisticated effort with respect to the peripheral circuitry?

A. Well, let's say the design effort is only in the peripheral circuitry, and it's a more sophisticated design effort compared to, let's say, a fuse, which is

a very simple design effort.

Q. Okay. Now, if we look under Good Die Yield, you say, "Reduced due to additional critical die area."

Do you see that?

A. Yes.

Q. What do you mean by "critical die area"?

A. As I described earlier, the memory component is about -- the active area is about 90 percent memory array. We have a unique technology called redundancy technology that can repair defective portions in the memory array. It's a very important part of the manufacture of DRAMs. And the way that works is the tester identifies a defective row or column or sector and replaces that with a spare sector that is functional. So, in essence, this large part of the die has some repairability associated with it, and a defect occurring there may not cause die failure.

The periphery does not have any redundancy capability. So, a defect in the periphery I call the critical die area, because a defect there will cause die failure.

Q. And why would this alternative reduce -- sorry.

Why would this alternative result in additional critical die area?

A. Because we are now taking two banks of data and

combining them. That's going to require some circuitry, some multiplexing circuitry, some timing circuitry, which is critical in nature.

Q. Okay. And what -- what is your opinion as to the cost effect of going with this alternative instead of dual edged clocking?

A. I reduced the die yield by approximately 2 percent for this particular solution.

Q. Okay, and what --

A. And it costs -- and that costs approximately 3 cents.

Q. Okay. If we could go, then, to the next non-negligible number under Final Test & Good Unit Yield, you say, "Increased Complexity testing."

Could you explain what you mean by that?

A. Yes, we now need to activate two banks, add some clocking circuitry. It may not be possible to test that as efficiently at wafer sort as if that circuitry were not there, and therefore, at final test, we have a slightly higher fall-out.

Q. Okay. And what would the cost effect of that higher fall-out be?

A. And I modeled that at a 2 cents cost effect increase.

Q. So, what, then, is your bottom line as to what

the estimated cost increase or decrease would have been if JEDEC had chosen this alternative instead of dual edged clocking?

A. I estimated the cost increase to be approximately 6 cents a unit.

Q. If we could go then to the next row, Interleave Memory Banks on DIMM, what's a DIMM, Mr. Geilhufe?

A. It's a dual inline memory module, a small circuit board that has 16 or 30 -- 16, 18 or 36 -- 32 or 3 -- I can't -- 16 or 18 DRAMs on it.

Q. Sixteen or 18?

A. Yes.

Q. Are you sure it's not eight or 16?

A. Sixteen or 18.

Q. Sixteen or 18?

A. Yeah, the IBM versions, remember? A parity bit adds a memory.

Q. Oh, okay, got you.

Under Board Complexity, which is the only apparently relevant entry here, you say, "Add multiplex and driver circuits."

Could you explain why this alternative would require the addition of multiplex and driver circuits?

A. Clearly this alternative requires no change to the DRAM itself at all. It is only a requirement at

the DIMM level, where you now take two DRAMs and merge the data of the two DRAMs at the DIMM level together, and that requires multiplexing circuitry, similar to the circuitry that the first alternative has on board, but here it is a set of separate components and may require clock drivers also.

Q. And what in your opinion would adding that multiplexer and driver circuitry cost?

A. I estimated that cost to be approximately $4 for multiplexers and clock drivers.

Q. And how do you get from that to a per-unit cost?

A. Again, we used a 20 million unit --

Q. This is on the DIMM, right?

A. On the -- oh, thank you.

Q. No problem.

A. This -- since we're now on a DIMM, the one-time cost gets amortized over 16 memory components, which is the smallest number of units -- memory components on the DIMM, and that's how we arrive -- I arrived at the 25 cent increase in cost.

Q. $4 divided by 16?

A. That is correct.

Q. If we could go then to the next row, the Double DRAM Data Width from x16 to x32, do you see that?

A. Yes.
Q. What's your understanding of that alternative?
A. My understanding is we would take a DRAM that has 16 I/O pins or a bus of 16 I/Os and add an additional 16, in other words, double the data width.
Q. So, under Product Design, you have, "Add $250,000."
Could you explain that?
A. Yes, this now requires significant redo of the peripheral circuitry, adding 16 I/O drivers and the necessary timing and multiplexing associated with that.
Q. And then under Good Die Yield, you have, "Reduced due to additional critical die area."
Could you explain what that means?
A. Yes, to add the additional I/O circuitry takes a considerable amount of critical die area, and I modeled that amount of die area to be -- to cost about 5 cents.
Q. Okay. Then if we go on to the Packaging column, you say, "Use BGA."
What does BGA mean?
A. If we add 16 I/Os to the package -- I'm sorry, I'm not answering your question. BGA means ball grid array package.
Q. And what is that?

A. That is a type of package that can have many more pins than the dual inline or JEDEC TSOP package.

Q. And why in your opinion would you have to use that type of packaging?

A. The largest TSOP package that JEDEC specified was 66 as a standard industry standard package. To add 16 pins, one -- it is my belief that one would have to go to a ball grid array package.

Q. And how much would that cost?

A. And I modeled that cost at 25 cents.

Q. So, then, in your opinion, if JEDEC had chosen this doubling DRAM data width alternative instead of dual edged clocking, what would the bottom line cost effect have been?

A. The bottom line cost effect would have been a 31 cent increase, approximately, per unit.

Q. Let's move on then to the next row, Double Clock Frequency. Could you explain what you understand by that alternative?

A. My understanding is instead of using, let's say, a 200-megahertz clock, use a 400-megahertz clock.

receding circuitry, so there's a nominal design change that has to take place.

Q. Under Final Test & Good Unit Yield, you have, "Higher speed testing."

Could you explain what higher speed testing would be required?

A. Yes, because we are operating the clock at twice the speed than current technology, that is a significant step up in testing, and the test equipment changes significantly. Test equipment changes and yield changes would result.

Q. And what would the cost effect of that higher speed testing be?

A. The higher speed testing would result in approximately a 4 cent increase in yield and test costs.

Q. And then under Board Complexity, you have, "On-DIMM clock required."

Could you explain what you mean by that?

A. Yes. To distribute this much higher frequency signal on -- the double frequency signal on the DIMM would require a -- an on-DIMM clock circuitry, possibly on-DIMM PLL/DLL.

Q. And how much would that add to the cost?

A. I estimated that cost based on product

availability from various manufacturers at approximately the $3.80. That cost is a very strong factor of frequency. Some of these parts can cost as much as $7 or $8 at high frequencies and can be less than this at low frequencies.

Q. And then what is your bottom line about what the cost effect would have been if JEDEC had chosen to double the clock frequency instead of using dual edged clocking?

A. I estimated the cost increase to be 28 cents approximately.

Q. A 28 cent increase?

A. A 28 cent increase, approximately.

Q. And then if we go to the last row on this chart, Asynchronous Toggle Mode, do you see that?

A. Yes.

Q. What is your understanding of the asynchronous toggle mode alternative?

A. That is basically to stay with the mid-'95 technology of asynchronous DRAMs. Of course, the general wisdom at the time was that that was not feasible, but I made a real attempt to see if it could be designed, and it -- I made some very basic assumptions as to how much work it would take to design it.

Q. Okay. And under Product Design, you have, "Add approximately $250,000."

Could you explain that figure?

A. Yes, this -- again, it's similar to the Double DRAM Data Width column -- excuse me, row. It's a significant design task.

Q. Under Good Die Yield, you say that would be reduced due to additional critical die area. Could you explain why that additional critical die area would be required?

A. We'd have considerable additional critical die area, and I modeled this as a 10 cent increase.

Q. Okay. And under Packaging, you say, "Additional pin."

Why would an additional pin be required?

A. Professor Jacob suggested that in his solution, and I modeled that.

Q. Okay.

A. Notice I modeled it only as a single pin, not the two pins that would likely be required in a TSOP package.

Q. Okay. And then what, then, is your bottom line conclusion about what the cost effect would have been if JEDEC had gone with asynchronous toggle mode instead of using dual edged clocking?

A. I estimated that cost increase to be approximately 12 cents.

Q. Let's move on then to the next chart, DX-301, and does this chart summarize your opinion, Mr. Geilhufe, about the cost effect of certain of Professor Jacob's alternatives to using an on-chip PLL or DLL?

A. Yes, it does.

Q. Okay. The first row, Double DRAM Data Width, is that essentially the same as the double DRAM data width alternative that you discussed with respect to dual edged clocking?

A. Exactly. It is exactly the same.

Q. And what is your conclusion then about how much that alternative would cost?

A. That alternative would increase the cost by approximately 31 cents.

Q. Let's move on, then, to the second row on this chart, Move DLL to DIMM. Could you explain what you understand that alternative to mean?

A. To take the DLL circuit block and remove it from the DRAM and add a set of circuits that carry the same functionality at the DIMM level.

Q. Okay. Now, under Wafer Sort, you say that test time would be decreased. Why is that?

A. Well, we remove a fairly sensitive circuit

block, the DLL on chip. That takes time to test. We reduce that -- we remove that test time.

Q. What would the cost effect --

A. And that would decrease the cost by 2 cents in my opinion.

Q. Okay. Under Good Die Yield, you say that there would be a slight yield increase. Can you explain that?

A. Again, the DLL is -- would be a critical die area, and I would assume that would increase the sort yield somewhat and would improve the cost by approximately 1 cent.

Q. Okay. And then finally, under Board Complexity -- should that be red under Board Complexity?

A. Yes, I apologize. We got the color wrong.

Q. Well, I am not sure that you were responsible for the colors, but in any case, why would an on-DIMM DLL be required here?

A. That, of course, is the alternative that Professor Jacob offers here.

Q. Okay. And how much would that cost?

A. And the on-DIMM DLL, again, would cost approximately $3.80 on -- for the DIMM and would be then a function of the frequencies that were supported.

Q. Okay. And then how would you translate that into a per-unit cost?

A. I would divide the $3.80 by 16, that is, amortize it over 16 DRAMs, and then, of course, reduce that number by the improved test time and yield numbers.

Q. Okay. And then once you've done that, then, what is your bottom line about what the cost effect would have been if JEDEC had chosen to go with a DLL on the DIMM instead of an on-chip PLL or DLL?

A. I modeled that cost as a cost increase of approximately 21 cents, approximately.

Q. Now, Mr. Geilhufe, if you were going to implement one of the alternatives for on-chip DLL and another alternative for dual edged clocking that we've discussed and yet some other alternatives for programmable latency and burst, how would you calculate the total cost effects?

A. The cost effects would all be additive.

Q. Now, have you reached any opinions about the difficulty or ease of actually implementing the alternatives that you considered, assuming that they were technically feasible?

A. Yes, I considered that in the design phase of

analysis.

Q. Okay. When could these alternatives be most easily implemented if you were going to try to implement them?

A. In DRAM manufacturing, there is a routine improvement -- the way costs are improved is by making changes to the product and the process on an as-needed basis, and that can happen as often as every six months or six to twelve or six to eighteen months. Every time one of these changes for either yield or process reasons are implemented, many of these if not all of these alternatives could possibly be implemented if they're technically feasible.

Q. Okay.

Thank you, Mr. Geilhufe, that's all I have.

JUDGE McGUIRE: Thank you, Mr. Detre.

At this time, we will hear the cross examination by complaint counsel. Mr. Davis?

MR. DAVIS: Let me try to operate the ELMO for a second, because I have a question about the slides. If I could have a minute or two just to learn how to do that.

(Pause in the proceedings.)

CROSS EXAMINATION

BY MR. DAVIS:

Q. Just a quick question about the slides, I didn't quite understand. Well, that's actually good enough for my purposes, because I just need to ask you about the colors.

I understand the red, that's -- you think the cost goes up, so that's red.

A. Yes.

Q. And green, you think the cost goes down, so that's green.

A. That's right.

Q. I'm a little confused about the yellow and the gray, however. What does the yellow refer to?

A. It's just to help us delineate one row from the next. It has no significance.

Q. Okay. So, the gray is to delineate from the yellow, okay. I will take that off for now.

Now, prior to your report in this case, Mr.

Exhibit B of your report prior to writing your report?

A. Yes, I did.

Q. And those references listed in Exhibit B, those are the documents that you relied on in putting together your opinions, in addition to your experience?

A. I primarily relied on my experience and my knowledge, industry knowledge.

Q. Okay. Your opinions didn't depend on any communications you had with Rambus attorneys?

A. They did not depend on any communication with Rambus attorneys.

Q. And they didn't depend on any communications you had with Rambus employees?

A. They did not depend on any communications with Rambus employees.

Q. And your opinions didn't depend on any communications you had with any other experts in the case?

A. They did not -- they did not depend on them, no.

Q. There were no documents that you wanted to see that you didn't get a chance to see prior to submitting your report?

A. I would have wanted to see cost documents from a number of companies, but no documents that were

MR. DAVIS: If he wasn't going to say it, I wasn't going to bring it up.

JUDGE McGUIRE: Okay.

BY MR. DAVIS:

Q. You also reviewed the Jacob rebuttal report prior?

A. Yes, I did.

Q. YoD(Tsa A. w0 .rQ. rort)TjTě Ja9

before your own deposition, made you think you needed to do any more work to confirm your conclusions in your report?

A. That is correct, nothing.

Q. Okay. And nothing you read in Dr. Peisl's deposition made you think you needed to do any more work to confirm your conclusions?

A. That is correct.

Q. Now, after your deposition but prior to your testimony here today --

A. Yes.

Q. -- have you read any additional deposition transcripts other than your own?

A. I've reviewed a whole series of documents, and quite frankly, I don't remember what they all are. I'm not very good at names.

Q. I think most of the engineers we've had so far haven't been so good with the names.

A. I'm one of them.

Q. Do you recall any additional deposition transcripts that you did review?

A. Let's see, there were various ones, and I just don't recall the specifics right now.

Q. You don't recall any names?

A. I think the -- the -- the Becker one -- yeah,

Becker, the deposition of the fellow from Siemens -- from Infineon.

Q. The DRAM fabrication plant manager is who you're referring to?

A. Yes.

Q. Have you been reading the trial transcript?

A. I'm sorry, I -- I believe it was the trial transcript of Dr. -- of Mr. Becker, not the deposition.

JUDGE McGUIRE: Now, let's be clear here for the record. You're talking about the trial in Infineon or the trial here at -- the FTC proceeding?

MR. DAVIS: Well, I'll clarify that.

BY MR. DAVIS:

Q. When you're saying you read the trial transcript of Mr. Becker, you are referring to the trial transcript in this case?

A. I believe that was it. I -- I'm not well versed in all the labels, but I believe that was it.

Q. I think that's the best we are going to be able to do.

Now, have any other facts or have any facts come to your attention that made you think you needed to do any additional work to confirm your conclusions in this case?

A. No.

Q. Now, what did you do to ensure that the analysis that you did was the type of analysis that's done at JEDEC?

A. I did not do anything. I did my analysis which has proven to be quite successful over the years.

Q. You never reviewed any JEDEC meeting minutes?

A. I did not.

Q. You never reviewed any JEDEC policy manuals?

A. I did not.

Q. You never spoke to any JEDEC employees to

Q. Well, there's both JEDEC employees, Mr. Geilhufe, and JEDEC members.

A. Oh, I see. I spoke neither to JEDEC employees nor JEDEC members.

Q. I was just about to make that clarification myself.

A. Thank you.

Q. And you never spoke with Rambus' JEDEC representative?

A. I did not.

Q. Did you ever ask to speak with Rambus' JEDEC representative?

A. No, I did not.

Q. Okay.

A. I felt I could give a much better opinion without hearing what someone who has a strong opinion feels.

Q. Now, have you ever been to JEDEC yourself?

A. I -- yes, I attended a -- one JEDEC meeting a long time ago.

Q. Now, I'm not sure -- are you confusing a JEDEC meeting with an IEEE meeting?

A. I believe I attended a JEDEC meeting once.

Q. Because when I asked you that question at your deposition, you said that you had never attended any

responsible for memory development.

Q. Now, when I asked you that question in your deposition, you told me that you had never supervised anybody who had --

A. I didn't, but there was someone in my organization, not someone I supervised.

Q. Okay.

JUDGE McGUIRE: You're talking about the organization at Intel?

THE WITNESS: At Intel, yes.

BY MR. DAVIS:

Q. Now, the only person you remember supervising whose job responsibility included attending standard-setting organization meetings was an employee of Intel who briefly reported to you in this time frame, sometime in 1975?

A. Oh, I think you're referring to Dick Pashley and the nonvolatile activity, yes. Thank you for reminding me.

Q. I want to go back to your background a little bit. So I understand, and I want to make sure I've got my notes right, the last time you contributed to a DRAM design was sometime in the mid to late 1980s. Is that right?

A. It depends on what you mean by "contribute." I

other companies' products to build them, brand them

factories and the skills of the people.

Q. Now, you were saying that a DRAM manufacturer can only use their factory for a relatively short time period for DRAM, something like one, two, three years. Is that right?

A. Yeah, not one year. It's longer than one year, but it's a finite life, and the life is shorter than the life of the -- clearly the building or the equipment.

Q. So, they use -- they use that same factory for other products?

A. Exactly.

Q. The fabrication plant that you were referring to in your work with ISD, you said you worked with a DRAM fab?

A. Um-hum, yes.

Q. That was the Kihun 1 fab. Is that it?

A. Yeah, Kihun 1 was a fab that went through that transition, and I also went through that transition on Kihun 2.

Q. And those were the fabs you were talking about when you said you had experience with DRAM fabrication plants when you were at ISD. Is that right?

A. That is correct.

Q. And the Kihun 2 fab -- am I pronouncing that

right, "Kihun"?

A. "Kihun" is close.

Q. That's as close as I can get.

Kihun 2, that was put together -- that was constructed, I'm sorry, in 1985. Is that right?

A. '85 or '86, that was definitely in that time frame.

Q. And the Kihun 1 fab was --

A. Was earlier, it was before that.

Q. Kihun 1 was built before?

A. Yes.

Q. Was it like 1982-1983, something like that?

A. Let's see, my first visit to that fab was somewhere in '84, somewhere in that time period.

Q. So, before '84?

A. Yes.

Q. Now, one of your opinions in this case that you gave this morning involved an analysis of the Rambus patent application along with the JEDEC standard. Do you remember that from this morning?

A. Analysis of the PCT application.

Q. Yes, that's what I was referring to.

A. Okay.

Q. I actually wrote '898 on my notes.

Going to the conclusions you reached on the

patent application, you read that patent application along with the JEDEC standard. Is that right?

A. That is correct. I only reviewed those two documents.

Q. And the conclusions you reached that -- I'm sorry, strike that.

The conclusions you reached were that some of the technologies described in the JEDEC standard are similar in form and function to some of the technologies described in the Rambus patent application?

A. That's correct, that's what I -- yes.

Q. And by "similar in form," you mean either an architectural characteristic or physical characteristic is similar between the JEDEC standard and the patent application?

A. Architectural context, application context or circuit context.

Q. When you said "application context," what did you mean by that?

A. For instance, a mode register, the concept of

A. And -- of course, they are.

Q. So, by "similar in function," you mean that if someone -- if something does one thing in the patent application, the PCT application, and it does the same thing in the standard, that the functions are similar?

A. I'm sorry, I don't think I understand.

Q. Okay, I'll say it -- I'll ask the question again.

By -- you found that -- you believed that the functions in the patent application, the PCT application, and the standard were similar in form and function, and I'm trying to understand what you mean by "form" and what you mean by "function."

So, I'm asking you by "function" --

A. Yes.

Q. -- do you mean that -- do you mean that if something does one thing in the patent application and it does the same thing in the standard, that the functions are similar?

A. That is correct. I -- yes.

Q. Now, you thought that it was irrelevant that the engineers who might have read the patent application --

THE REPORTER: I'm sorry, I didn't hear the end of that.

BY MR. DAVIS:

Q. I'll reread the question.

You thought that it was irrelevant that the engineers who might have read the patent application were at JEDEC. You didn't consider that as part of your conclusions.

A. That has no bearing on my analysis. My analysis was to review the documents.

Q. So, you didn't consider what effects the JEDEC patent disclosure rule would have had on the analysis done by the JEDEC representatives?

A. I did not.

Q. And you didn't consider the effects of what the good faith obligations on JEDEC members had on the expectations of its members?

A. I did not. I only considered what a designer or a design manager would do by being confronted by the two documents.

Q. You didn't consider the effects of Rambus' behavior at JEDEC on the analysis done by the JEDEC representatives?

MR. DETRE: Objection, Your Honor. The witness has asked and answered. The witness already answered what he did, that he did not consider any JEDEC stuff.

MR. DAVIS: I'm asking specific --

JUDGE McGUIRE: Well, this is another question, so I'll entertain this new question. Overruled.

BY MR. DAVIS:

Q. You didn't consider the effects of Rambus' behavior at JEDEC on the analysis done by the JEDEC representatives?

A. I did not consider it, and I have no knowledge of their behavior.

Q. And you didn't consider the potential impact of other information that the engineers at JEDEC might have had about Rambus?

A. Of course not. I only compared two documents.

Q. Okay. Now, I'd like to show you a document that's been marked as CX-1309, which is a Rambus technology and applications overview.

May I approach, Your Honor?

JUDGE McGUIRE: Yes.

THE WITNESS: Oh, boy.

BY MR. DAVIS:

Q. You won't be going through all those pages.

Could you turn to page 28 of CX-1309? Now, what you are looking for in terms of the page numbers are on the corner, do you see the page numbers there? It says CX-1309-028?

A. There we go, got it. Twenty-eight.

Q. Twenty-eight.

A. Okay.

Q. And do you see that there's a diagram on the left --

JUDGE McGUIRE: All right, now, before we get into that, I am going to need to know exactly what this document is for the record, Mr. Davis, so could you lay a foundation?

BY MR. DAVIS:

Q. Okay, this is a -- as I understand it, a Rambus technology and applications overview. I mean, we have seen documents like this.

A. Excuse me, sir, I didn't understand the answer.

JUDGE McGUIRE: Could you restate what this document is for the witness?

MR. DAVIS: Sure.

BY MR. DAVIS:

Q. This is a Rambus technology and applications overview, a description of the Rambus technology, and on page 28, do you see that there's a diagram on the left-hand side that's labeled SDRAM?

A. Yes.

Q. And a diagram on the right labeled RDRAM?

22 A. Yes.

Waldorfcorarylft-on?

diagrams like it on the question of how an experienced engineer at JEDEC would view the Rambus patent?

A. Of course not. As I indicated earlier, I only considered the JEDEC specification, JC-21, and the PCT application.

Q. Had you ever seen a diagram like this before?

A. I've seen thousands of diagrams.

Q. Do you recall seeing a diagram like this before?

A. I have never seen this diagram, no.

Q. Okay. Now, could you turn to page 212 of CX-1309? Again, it's the same page numbering.

A. Bear with me.

Q. Sure.

A. I've got it.

Q. Do you see there's a column on the left-hand side describing RDRAMs and a column on the right-hand side describing SDRAMs?

A. Yes, I do.

Q. Did you consider the effects of this table or tables like this on the question of how an experienced engineer would read the Rambus patent?

A. As I said, I have only reviewed the JEDEC document and the PCT application.

Q. Okay, you can put that aside.

application, you were able to identify the four features that you were asked to identify in that patent application?

A. As I indicated in my report, yes, I was able to identify that an experienced DRAM designer should -- would show concern and would evaluate very carefully whether he could go ahead with some of these features.

Q. I'd like to talk a little bit about your conclusions regarding programmable burst length.

A. Okay.

Q. In your testimony, you stated that an experienced DRAM designer would find commonality between the variable block size of the PCT and the programmable burst length of the mode register. Is that accurate?

A. That's correct.

Q. And by "programmable burst length of the mode register," you were referring to the mode register that's described in JEDEC's standard 21-C, Release 9?

A. That is correct.

Q. And part of that standard is actually referenced, isn't it, in your Appendix B to your report? It's one of the documents you relied on.

A. That is correct.

Q. And by "variable block size," you're referring

to a particular bit of language from the PCT application. Is that right?

Let me read to you something from your -- from your report that --

A. Please.

Q. -- related to that same opinion, and it's going to be complicated because it's patent language, so we are going to have a lot of open parens and stuff. I'll try to be clear.

A. Can I have a copy of my report, please?

Q. Absolutely, absolutely.

A. Thank you.

Q. I should have done that first, I'm sorry.

A. Thank you.

MR. DAVIS: May I approach, Your Honor?

JUDGE McGUIRE: Go ahead.

THE WITNESS: Thanks.

BY MR. DAVIS:

Q. And in fact, for your reference, I'm referring to something that's on page 6 of your report.

A. Thank you.

Q. Paragraph 17.

Your Honor, we don't have this in the database, I don't think, so may I approach?

JUDGE McGUIRE: Yes, okay, that will be fine.

BY MR. DAVIS:

Q. Okay, "Page 27, (23) block size [0:3] Specifies the size of the data block transfer," and you have three dots, "if block size one is zero, then the remaining bits give a block size to the power of two."

Now, actually, in your deposition, you have a slight correction to the report language, right, which was that "block size one is zero" should actually read "block size zero is one." Is that right?

A. That's correct.

Q. But with that correction, your report describes your opinion in this area?

A. That is correct.

Q. Now, in your analysis, you identified three factors that were relevant to your opinion that an experienced DRAM engineer would find commonality between the variable block size in the PCT and the programmable burst length of the mode register. Is that right?

A. Yes, I did.

Q. And those three factors were the diagram in one document looks like the diagram in the other, the two documents use the same word, and they describe the

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so I can't vouch for it, but it sounds right.

Q. Okay. Well, why don't I give you a copy --

JUDGE McGUIRE: Mr. Detre?

MR. DETRE: Your Honor, I just object generally to the use of this expert report. It is not evidence. It can be used to impeach, but that's not how Mr. Davis is using it.

JUDGE McGUIRE: Mr. Davis, that's correct, so how do you intend to proceed in this matter?

MR. DAVIS: Well, Mr. Geilhufe described his conclusions in this matter regarding the patent application, but he didn't describe the basis in his testimony. He did describe the basis for that testimony in his report.

JUDGE McGUIRE: Then to that extent you can inquire.

MR. DAVIS: Thank you, Your Honor.

BY MR. DAVIS:

Q. Actually, I think I should give you a copy of your deposition as well on this.

A. Thank you.

MR. DAVIS: May I approach?

JUDGE McGUIRE: Yes.

BY MR. DAVIS:

Q. Now, the two documents use different words to

describe this concept, correct? I mean, one uses "programmable burst length," the other one uses "variable block size," so they're different terms.

A. Different terms describing the exact same function.

Q. Now, I'd also like to show you document CX-234,

A. There's something out of whack on mine. I have a 146 and then a 176. The 150 doesn't seem to be there.

Q. Why don't I give you this copy. This copy has it.

May I approach?

JUDGE McGUIRE: Go ahead.

THE WITNESS: A bigger copy. Thank you.

BY MR. DAVIS:

Q. We're looking at page 150.

A. I have 150.

Q. You have 150 in front of you now?

A. Yes.

Q. This is the diagram of the mode register that you were referring to, is it not?

A. That's correct.

Q. Now, I'm going to give you another document, and I have to apologize for it, because you already have the document in another form, but it's RX-185, which is the PCT again. My references on my outline are to that.

A. Is there some question on the JEDEC document?

Q. There is no question yet.

A. Oh.

MR. DAVIS: May I approach?

JUDGE McGUIRE: Yes.

BY MR. DAVIS:

Q. Now, could you turn to page 29 of RX-185, and by 29, I'm referring to the exhibit page numbers.

A. The exhibit page number is 29 and the document number is 27?

Q. I believe that's right.

A. Okay.

Q. Now, could you focus on line 23 and the language that is quoted -- I'm sorry, could you focus on line 23 of that? That's the language that's quoted in your report. Is that right?

A. Okay.

Q. Now, the reference to block size there is a reference to a part of a request packet. Is that right?

A. I don't see the reference to a request packet.

Q. Okay. Could you turn to page 21 of the PCT, which is page 23 of the exhibit, and look at the paragraph that starts on line 21?

A. Okay, I'm on page 21.

Q. And you're looking at line 21, the paragraph that starts on line 21? Are you there?

A. There's no paragraph that starts there. It looks different. My 21 looks different from the one on

the screen.

MR. DAVIS: May I approach?

JUDGE McGUIRE: Go ahead.

THE WITNESS: What page?

BY MR. DAVIS:

Q. Twenty-one.

A. Ah, thank you.

Q. There you are.

A. There we go. Thank you for your help.

Q. Now, the first sentence of that paragraph states, "In a preferred implementation of this invention shown in Figure 4, a request packet contains 6 bytes of data -- 4.5 address bytes and 1.5 control bytes."

Do you see that?

A. Yes.

Q. And then the paragraph continues onto the next page, correct?

A. Yes.

Q. Why don't you turn to the next page.

A. Okay.

Q. So, if you look at the last sentence of that same paragraph, it states that, "The last byte contains address valid --" I'm sorry, "AddrValid (the invalidation switch) and the remaining address bits,

address (36:39), and block size (0:3)," then it says "control information" in parentheses.

Do you see that?

A. Yes.

Q. Does that indicate to you that block size is part of a request packet in the language that you quoted?

A. In this description, it could very well be.

Q. Could you turn to page 129 of the exhibit?

A. Page 129?

Q. This is the patent application. Are you on page 129?

A. Yes, I am.

Q. You see a diagram at the top labeled Figure 4, correct?

A. Yes.

Q. At the bottom of that figure, you see block size 0:3. Do you see that?

A. Yes, I do.

Q. Now, is Figure 4 the diagram in the PCT application that you believe looks like the diagram in the JEDEC standard?

A. Not at all.

Q. Could you leaf through that -- and if you look at the last pages of the PCT application, you'll see

JUDGE McGUIRE: Well, then, I'm unclear then as to what -- if the question is inaccurate regarding your prior testimony, then what other diagram had you referred to?

THE WITNESS: I referred --

JUDGE McGUIRE: And we're assuming that this -- that what he just said is true.

THE WITNESS: And I may have misspoken.

JUDGE McGUIRE: All right, that's why I'm asking you this so we can clarify it.

THE WITNESS: Clearly -- and I appreciate the opportunity to clarify. Clearly block size, the technical concept of block size and the technical concept of burst length to me, as an -- as an engineer, have great similarity, and I drew that conclusion. They were not the same words, but they have -- they are the same function.

JUDGE McGUIRE: All right, Mr. Davis.

BY MR. DAVIS:

Q. Is that because you believe they're implemented in the same way in the patent application and in the JEDEC standard?

that right?

A. They generate the same result in terms of the number of bits that get either written or read.

Q. Now, I asked if you believed that they're implemented in the same way in the patent application and the JEDEC standard. I'm not sure you answered the question.

Do you believe they're implemented in the same way in the patent application and in the JEDEC standard?

A. Please note, the JEDEC standard is a specification. It does not require implementation. How something gets implemented is up to the manufacturer or the designer.

MR. DAVIS: I move to strike, Your Honor. It's not responsive.

JUDGE McGUIRE: Well, I'm not going to strike that one. I do think it does to some extent answer your question. It may not be quite the way you had hoped, but you know, I'm going to leave it in. And I'm still somewhat unclear as to what's on the table in terms of the pending question, so you may want to go back.

MR. DAVIS: Well, there is no pending question at this point.

JUDGE McGUIRE: Well, I meant the prior question. He's answered it to the extent that you weren't pleased with it, so maybe we can go back into that if you care to do so.

MR. DAVIS: I might after a break. I want to make sure I think it through.

JUDGE McGUIRE: Okay, all right.

BY MR. DAVIS:

Q. Now, let's move on to the -- to another topic here. You also testified regarding the DLL on the DRAM, that an experienced DRAM designer would find commonality between the JEDEC on-chip DLL and the on-chip DLL that you believe was disclosed in the PCT application. Is that right?

A. That is correct.

Q. Now, you have the JEDEC standard in front of you, don't you?

A. That's correct.

Q. Could you show me where in the JEDEC standard you have in front of you there's a diagram that's the same as that in the PCT application?

A. Again, the JEDEC standard is a specification that does not require -- define specific implementations.

Q. So, if you --

A. Excuse me, let me finish, please.

Q. I'm sorry.

A. I will -- I will look for the -- for the specific reference for you, though, if -- and maybe someone can help me. We're looking for the extended DDR mode register --

Q. We're looking for -- well, I'm not sure what you're looking for at this point.

A. To try to answer your question, you asked where in that specification. I can reference this, and I was trying to do that for you.

Q. Let me see if I can short-circuit it.

A. All right.

Q. There is no figure in that standard that describes any DLL circuitry. Is that right?

A. Again, a standard is not supposed to --

JUDGE McGUIRE: Okay, you have answered that already, sir. Maybe you can just answer the question.

THE WITNESS: I'm sorry.

JUDGE McGUIRE: Does that exist in the JEDEC standard?

THE WITNESS: It does not exist in the JEDEC standard.

JUDGE McGUIRE: Okay, thank you.

BY MR. DAVIS:

Q. Now, in your deposition, you stated that if the block diagram and the language is the same, that would raise a serious question for an experienced DRAM designer. Is that right?

A. Or if -- yes, I believe that's what I said, but certainly if the language is similar or the block diagram is similar, any one of those things will raise that question for me.

Q. And you referred to pages 56 to 59 of the PCT as describing the DLL that's in the application. Is that right?

MR. DETRE: I'll object again to the use of the deposition this way. There's no --

JUDGE McGUIRE: Sustained. That's not how we use depositions, Mr. Davis.

BY MR. DAVIS:

Q. Well, you believe that the -- if the block diagram and the language is the same, that would raise a serious question for an experienced DRAM designer?

A. My testimony is that if a block diagram or language is similar, it will raise that concern.

Q. Okay. And that's --

A. N us Rc 2 if how sam" th,"t

today?

A. That is correct.

Q. Could you show me where in the portion of the patent application that you believe refers to the DLL that that l,

A. That's right. And that figure is referenced in the body.

Q. Okay, well, let's stick with 139 for a second so that I can get on the same page as you.

A. All right, okay.

Q. Were you referring to Figure 12?

A. I'm -- I apologize, page 135 of 139.

Q. You were referring to -- you said 139. You're referring to the last --

A. I apologize.

Q. That's okay, no, understandable.

And you're referring to Figure 12 that's listed there. Is that right?

A. Yes.

Q. And you were going to look for the part of the patent application that references that figure for the DLL language?

A. That's correct, and I believe that is somewhere in the pages that I cited where the patent application discusses clock circuitry. Let's see, you will have to bear with me, because it may take a bit.

Q. Sure.

A. (Document review.) In glancing at it right now, I can't find it.

Q. Are you looking at pages 56 to 59 of the PCT?

A. I believe so. Yes. (Further document review.) I cannot find the reference right now.

Q. Well, perhaps after lunch --

A. I can take a look at it at lunch.

Q. -- if you find the reference to DLL, you can point that out. I'd appreciate it.

A. Yes.

Q. Now, we have Figure 12 up on the screen, and I will ask you a few questions about that. There is no mention of the DLL there on that screen, correct?

A. That's correct.

Q. Your contention is that the circuitry itself is a DLL?

A. Yes, I -- I would suspect a second-year engineering student, electrical engineering student would recognize this as a DLL.

Q. That that's a DLL?

A. Yes, um-hum, potentially a DLL.

Q. Okay. Now, this is the figure that's similar in function to the DLL that's specified in the JEDEC DDR standard?

A. That's described in the -- in the DDR standard.

Q. See, I tried to use the word "specified" so you wouldn't have a problem with it, but that's what I meant. We already established that there is no DLL

figure in there.

A. That's correct.

Q. Okay. And the function of the DLL in the DDR standard is that it aligns the clock that's internal to the DRAM with the system clock?

A. In a general sense, yes.

Q. And this is --

A. It aligns one clock with another clock -- with another clock, one signal with another clock.

Q. But in the DDR standard, the clock that's being aligned is the internal DRAM clock --

A. Yes.

Q. -- and that's being aligned with the system clock. Is that correct?

A. Yes, I believe so.

Q. The DLL delays the clock that's internal to the DRAM so that it lines up with the system clock?

A. I believe so.

Q. And this is the circuit that you believe aligns the -- when I say "this," I mean Figure 12 -- this is the circuit that you believe aligns the clock that's internal to the DRAM with the system clock?

A. No, this is a circuit that aligns one clock with another clock.

Q. And what clock is being aligned here with what

clock?

A. My --

Q. There's two clocks being aligned. What's being aligned with what in Figure 12?

A. Depending on the delay lines and the values in the delay lines, we can't tell from this circuitry. It's -- excuse me, from this block diagram, we cannot tell which is aligned which way.

Q. Okay.

Your Honor, this is a good breaking point for me.

JUDGE McGUIRE: Okay, it's 12:30. Why don't we break for lunch and reconvene at 1:45. The hearing is in recess.

(Whereupon, at 12:30 p.m., a lunch recess was taken.)

and then I'll give their side an opportunity to respond either in writing or orally on that regard, and we're going to have to tie this up in pretty short order.

Could I inquire of I guess complaint counsel, do you have some idea at this point who you intend to offer in rebuttal?

before they conclude their case in chief on Tuesday.

MR. OLIVER: That would be fine, Your Honor. If I could simply ask if there is any unexpected testimony after Thursday, would we be able to augment if necessary? I don't anticipate that, but if necessary.

JUDGE McGUIRE: Well, we will take that up at the time, but we'll see.

MR. OLIVER: Thank you, Your Honor.

JUDGE McGUIRE: Did you have anything else, Mr. Perry, you wanted to add to this discussion?

MR. PERRY: No, Your Honor.

JUDGE McGUIRE: Okay, good.

Let's go back -- sir, you can take the stand again, and you are still under oath from this morning. Thank you.

Mr. Davis, you can proceed with your cross examination.

MR. DAVIS: Thank you, Your Honor.

BY MR. DAVIS:

Q. Actually, I have a few questions, Mr. Geilhufe, on your background --

JUDGE McGUIRE: You know, just again, let me just say, I'm probably going to issue just a short order tomorrow, if I can, just to give you the scope of

what I intend to see on rebuttal just so we're clear. It's going to be a very short order, just something to give you all some guideline on where I want to see this to go, and then we can do what we said we're going to do.

Okay, Mr. Davis, go ahead.

BY MR. DAVIS:

Q. Do you recall this morning you testified that you had four patents in the DRAM design area?

A. That's correct.

Q. When was the last DRAM design patent issued?

A. I don't recall. Probably in the early eighties.

Q. In the early eighties? When was the one before that?

A. I really don't recall. It's a long time ago.

Q. Okay, I thought I had one more background question. Maybe I didn't.

Now, there was a question from this morning that you were going to look at over lunchtime, which was where in the PCT application DLLs are mentioned. Did you have a chance to look at that over lunch?

A. I think I stated that the PCT application referenced Figure 12 in the document itself, and you asked me to identify where that reference was.

Q. No, I asked you to identify where DLLs were mentioned in the patent application.

MR. DETRE: I think that misstates Mr. Geilhufe's prior testimony. He never said DLLs were specifically mentioned. He said there was a reference to Figure 12 that shows a DLL.

MR. DAVIS: I wasn't actually referencing, Your Honor, any prior testimony. I was referencing my prior question to Mr. Geilhufe, which was where DLL was mentioned --

JUDGE McGUIRE: I'll entertain the question.

BY MR. DAVIS:

Q. Did you have a chance to look for the mention of DLLs in the patent application over lunch?

A. It is not mentioned in the patent application --

Q. Okay.

A. -- that particular word, just a DLL circuit is in the patent application.

Q. And that's Figure 12?

A. That is correct.

Q. Now, I would like to ask a few questions about the tables that you presented this morning. As introduction, I'll have some clarification questions, and let me make sure I find the right one.

Are you able to see the screen -- actually, you probably have your own copy of that.

Actually, yeah, I don't have an electronic copy of this. Would you -- is it possible for you to put this up --

MR. DETRE: Sure, if you could change -- switch over the computer to that.

MR. DAVIS: To counsel computer?

MR. DETRE: Yeah. DX-298, is that --

MR. DAVIS: Is that the CAS latency?

MR. DETRE: Yes, DX-298.

MR. DAVIS: Great.

BY MR. DAVIS:

Q. Now, if you look at the CAS latency -- let me see -- I'm sorry, it's DX-299 that I have. That's the effect of the burst length alternatives.

A. Yes.

Q. Look under Burst Length in Read/Write Command, under the Estimated Cost Increase or Decrease, it says 0.005 cents to 0.2 cents?

A. That's correct.

Q. Are you saying there's a half a cent to a 20 cent increase in price per unit?

A. No, it's 2 cents. I see it's a typo. I apologize for that. It should be 0.02. Thank you for

correcting it.

Q. All right. Now, when you presented your testimony today regarding the DRAM costs, what you were presenting wasn't actual DRAM costs but a model of DRAM costs based on your experience?

A. As I testified, I modeled these alternatives, that is correct.

Q. Okay. As a result of the fact that you were using a model, all of the information presented in your testimony was approximate?

A. That is -- that is correct. All the information is estimated.

Q. In fact, you believe that the margin of error for each of the cost elements described in your presentation is 25 percent. Is that right?

A. At -- at worst. I suspect it's less than 25 percent.

Q. And you base that margin of error on your experience?

A. Yes, as I made many -- more and more and more cost estimates over my career, they tended to get better.

Q. And you didn't test your projections in this case to any actual results to see if the results actually were within 25 percent of the actual numbers,

did you?

A. Well, since the vast majority of these never got implemented, it was not possible to test them.

Q. So, the answer is no, you didn't test?

A. I did not.

Q. And the only way that you can think of for anyone else to verify or validate the cost numbers that you arrived at is to ask a DRAM manufacturer, particularly a firm like Infineon?

A. I know I stated something to that effect in my deposition. I need to clarify that comment. Since it never got implemented, many of these alternates never got implemented at a DRAM manufacturer, it would be impossible for a DRAM manufacturer to verify many of these alternatives.

Q. But to the extent that they were implemented in some fashion, that would be how I would validate them?

A. That would be one possible way, if they were indeed implemented.

Q. And you never did that; you never attempted to verify the numbers you came up with with the DRAM manufacturers.

A. Mr. Davis, please recognize, cost information is the most carefully held, confidential information in the corporation and is not available to someone who's

not in the corporation.

Q. You didn't ask Rambus to conduct discovery on that question, did you?

A. I did not.

Q. And you didn't actually review any documents relating to the manufacturing costs of DRAM manufacturers in this period?

A. I -- there are a series of estimates by industry analysts that suggest my cost numbers, certainly the total cost numbers, seem to be correct. I did over the years review and I'm aware of what analysts said about costs.

Q. Were those estimates by industry analysts included in the documents you relied on, you attached to Exhibit B to your report?

A. No, they were not.

Q. Now, since the numbers that you gave us are based on your own experience, you can't speak for any of the DRAM manufacturers in the relevant time period in terms of what their costs actually were, can you?

A. Clearly -- as I stated, cost information is highly confidential, and I cannot speak for the actual costs at a DRAM manufacturer. I can only speak for the model that I feel is a credible model that I used.

Q. You did read a deposition of an employee of a

current DRAM manufacturer regarding what the -- what he thought the actual DRAM manufacturing costs would be, didn't you?

A. I -- can you be more specific? I'm -- it's too general.

Q. You read the deposition of Dr. Peisl, didn't you?

A. Yes, I did.

Q. And Dr. Peisl's a current employee of Infineon, correct?

A. I believe so.

Q. And you might recall that Dr. Peisl either designed or managed the design -- design team for a number of DRAMs. Do you remember reading that?

A. I understand that, yes.

Q. Dr. Peisl was involved in the design of EDO in 1994. Do you remember reading that?

A. Right, I recall that.

Q. And Dr. Peisl managed a team designing the SDR and DDR combination part that Infineon made?

A. I recall that.

Q. I think they called it Cronus, do you remember that name?

A. Something to that effect.

Q. And Dr. Peisl also managed the design of the

256-megabit DDR SDRAM part called Orion. Do you recall that?

A. Correct. He testified to that as I recall.

Q. So, Dr. Peisl was either designing DRAMs or managing the design of DRAMs during the relevant period, to your understanding?

A. To my understanding.

Q. And in the deposition that you read by Dr. Peisl, he talked about what he believed to be the cost impact of some of the alternatives based on his own DRAM design experience. Do you remember reading that?

A. I don't recall the specifics. Maybe you can refresh my memory.

Q. I think I will in due course.

Dr. Peisl also testified that there's an entire organization at Infineon that does an analysis of the cost of manufacturing DRAM. Do you remember reading that?

A. I recall something to that effect. It's very common in DRAM manufacturing organizations.

Q. Dr. Peisl himself could only take an educated guess at the actual cost of alternatives but only after reviewing a million Excel spreadsheets?

A. I don't remember reading that exact comment, but if you can read it for me.

Q. Okay. The Peisl deposition?

May I approach, Your Honor?

JUDGE McGUIRE: Go ahead.

MR. DETRE: Your Honor, this is not a proper use of the deposition testimony of Dr. Peisl. This is not evidence that's in the record here at this trial. Dr. Peisl testified at trial. I don't think it's appropriate to try to get his deposition testimony in in this manner.

MR. DAVIS: I'm not trying to get the deposition testimony in at all. Dr. -- I'm sorry, Mr. Geilhufe read this testimony. It was part of the information that he reviewed prior to his deposition at least, and the question is how did the use of this information affect his opinions?

JUDGE McGUIRE: I will hear it on that basis.

BY MR. DAVIS:

Q. Now, if you turn to page 193, starting at line 20, and I'll read the lines and then ask you if that comports with your reading.

"QUESTION: You asked me the question as to did or could -- could you provide a total cost estimate for these two alternatives?

"MR. WILKINS: Right now he is just asking yes or no.

"THE WITNESS: Yes."

"QUESTION: Okay. Could you do that sitting here?

"ANSWER: No.

"QUESTION: What would you have to do to make that cost estimate?

"ANSWER: To go through a million Excel files.

"QUESTION: To go through a million Excel files?

"ANSWER: Excel files."

Then he goes on to describe what he means by that.

Do you remember reading that?

A. I just read it again. I now recall reading it.

Q. But that didn't make you think that you needed to get more data before deciding what the cost of the alternatives would be, did it?

A. Well, it suggests the answer that Mr. Peisl gave was a somewhat incredulous answer. No one reads a million Excel files, at least not a human being that I know of.

Q. You didn't take his answer to mean that it would require a lot of work to --

A. I took it literally.

Q. Let me finish my question.

A. Certainly.

Q. You didn't take his answer to mean that it would require a lot of work to come up with the actual cost estimates?

A. I took his answer as a nonanswer. Anyone who suggests the reading of a million Excel files suggests something that's incredulous.

Q. So, the next question and answer states:

"QUESTION: What do you mean by that?

"ANSWER: My company in Munich, this is done by people in headquarters, has very accurate cost estimation --"

A. Excuse me, would you tell me what line, please, again?

Q. Starting on line 9.

A. Page?

Q. Page 194, just continuing.

A. One minute.

Q. "ANSWER: My company in Munich, this is done by people in headquarters, has very accurate cost estimations and cost projections of essentially whatever it takes to produce a manufacturer test, so I would have it to look at this in detail to come up with an educated guess."

Does that still make you think that he was

stating that -- that he was giving a nonanswer?

A. If an executive in a billion dollar business gives these kinds of answers, it suggests that he really doesn't understand what he's answering or that he really doesn't know an answer. This is -- you know, if someone gave me that answer when I -- if I would have asked the question during a business review, that individual would go back to work and get much, much better answers.

Q. And Dr. Peisl himself was unwilling to give any specific numbers for the costs of alternatives without doing the actual circuit designs that were required to determine what was being estimated. Do you recall reading that?

A. I think that is a much, much more appropriate answer.

Q. You didn't do any circuit design for this case, did you?

A. Since the alternatives that I was asked to look at did not include circuit design, that suggests already that they were poorly thought out alternatives. They were not detailed enough to do any circuit design. If the alternatives that Dr. Jacob had offered included circuit design, we would have been able to -- I would have been able to do that analysis, of course.

Q. But you didn't do any circuit design in this case, did you?

A. I could not do any circuit design.

Q. So, you didn't?

A. I did not.

Q. Now, you're not offering an opinion in this matter that the method that you followed in this case is the same method used by JEDEC representatives, right?

A. I am only offering the -- my model as my method, as a method that has been proven over a long period of time to be reasonably successful.

JUDGE McGUIRE: Well, I'm not sure that answers his question. It either did comport with what the JEDEC --

THE WITNESS: I have no --

JUDGE McGUIRE: And if you don't know, you don't know.

THE WITNESS: I have no knowledge of how JEDEC folks did their analysis or if they did an analysis, Your Honor.

BY MR. DAVIS:

Q. Now, you stated earlier today that each of the alternatives that you reviewed could have been implemented in a six to twelve-month time frame. Is

that accurate?

A. It is my belief that that could happen.

Q. But in making that determination, you didn't include any consideration of how long it would take JEDEC to determine which alternatives to put in the standard, did you?

A. Of course not. That wasn't -- just not.

Q. And your determination of six to twelve months was based on your own experience?

A. It's based on the industry experience of how often a DRAM normally gets revised during its manufacturing cycle. So, it would literally -- I estimated that this would be a piggyback on existing revisions that were going on.

Q. But how long would it take to actually do the design and implement those designs, you thought that would take six to twelve months from when one decided to do it, right?

A. That is correct.

Q. So, that part of the question, you thought it would take six to twelve months to implement these standards which was based in part on your industry -- your own experience of how long it would take to implement those?

A. That's correct.

Q. And you didn't review any evidence that might tell you how long it would take to change the DRAM designs?

A. I certainly understand how long it takes or has taken at Winbond recently. I certainly understand or one can interpolate from Samsung's product codes, which identify the revision codes in the product code, approximately how often they change their redesign or change their product.

Q. But I'm asking you how long it would take a DRAM designer to do the design, not how often they revise the designs.

A. Excuse me, that's not the question you asked before. You asked design and implement. If we're just talking about design, that's a different issue.

Q. Okay. You didn't review any evidence that might tell you how long it would take to design -- I'm so 18 17 ntMw metMwom

and 2000?

A. Yes. Recall, ISD and Winbond were partners before that, and then I became part of Winbond.

Q. And this was when you had testified that you didn't have any DRAM manufacturing -- let me get back to the actual testimony that you gave.

Now, this is where you said that your manufacturing experience was limited to being aware of the volumes and types of DRAMs that were being manufactured and the profitability of the DRAMs?

A. Right, so I was aware of the revisions of the DRAMs.

JUDGE McGUIRE: Let him finish, and then I'll ask you to file your objection. Go ahead.

MR. DETRE: When --

JUDGE McGUIRE: No, I am going to let him answer the question.

Well, if you don't remember it, now, what's your objection?

MR. DETRE: I don't -- Mr. Davis said "you said." I don't know if he's looking at trial testimony or deposition testimony or what. If it's the latter, he hasn't properly impeached the witness with it.

JUDGE McGUIRE: Could you clarify, Mr. Davis?

MR. DAVIS: I just reread a question that I had

read this morning that he answered "yes" to.

JUDGE McGUIRE: Does that satisfy you, Mr. Detre?

MR. DETRE: I'm not sure if Mr. Davis is characterizing the record correctly or not, frankly. He's citing his own notes apparently.

JUDGE McGUIRE: I am going to assume that he has, and if he hasn't, n't, frankly.

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11 I'm not suBYure ifAVIS: Detre?
1UIRE: DoQ. Lets ago through so ofor nocost elem s k Detre?
1 discusse answered "yes Detre?

A. And my experience in -- in many other products that I've done over my career.

Q. You reviewed no evidence relating -- in this case relating to the costs of DRAM manufacturers for this element from the relevant period other than the Peisl deposition. Is that right?

A. That's correct, and the Peisl deposition suggests my numbers seem to make sense.

Q. So, your recollection from reading the Peisl deposition was that he agreed with your design costs?

A. He suggested the size of the design teams that were required were consistent with what my understanding of the industry is.

Q. Well, I'd like to focus your attention on the Peisl deposition, in particular --

Did I give you a copy of that, Your Honor?

JUDGE McGUIRE: No, I don't -- well, I'm sorry, which one is that?

MR. DAVIS: That's the Peisl deposition.

JUDGE McGUIRE: No, I've just got his deposition.

MR. DAVIS: May I approach?

JUDGE McGUIRE: Yes.

MR. DAVIS: I had an extra copy and I wasn't sure why. Sorry.

BY MR. DAVIS:

Q. If you would turn to page 74 and focus in particular on line 15, and I'll read it and ask you if I'm reading it correctly.

"QUESTION: Okay, well, let's go through them. What do you understand product design to be?

"ANSWER: Product design is the cost involved for engineers for designing of parts.

"QUESTION: Would designing fixed CAS latency parts be more expensive than designing a part that had programmable latency?

"ANSWER: No."

Do you recall reading that?

A. Yes.

MR. DETRE: Objection, Your Honor. Again, we object to getting the Peisl deposition testimony into evidence, if that's what Mr. Davis is attempting to do.

MR. DAVIS: I'm not. I'm asking what the effect of that -- of reading that portion of the deposition had on his opinion that there would be higher design costs.

JUDGE McGUIRE: I indicated earlier that on those grounds, I would hear the question, and it's going to be to that extent only.

MR. DETRE: Thank you, Your Honor.

MR. DAVIS: And in fact, I can stipulate that any time I read from the Peisl deposition, it's solely for that purpose.

JUDGE McGUIRE: Okay, thank you, Mr. Davis.

MR. DETRE: Thank you.

BY MR. DAVIS:

Q. Dr. Peisl thought that the design of -- that -- I'm sorry.

Did Peisl thought that the design of the alternative that we were discussing in that deposition, which is fixed CAS latency, was less expensive than what was in the current standard. Is that right?

A. Would you read that for me? I don't see that.

Q. I'm sorry, he said that designing the fixed CAS latency wouldn't be more expensive than programmable CAS latency, correct?

A. That's what he states here, and of course, he's wrong, as he knows himself. If you want to do another product, it takes a design cycle. If you --

Q. But he's not talking about doing another product, is he? You were -- your estimates were of doing a product instead of doing the JEDEC standard product. Isn't that right?

A. My estimates are of doing several products instead of the JEDEC product.

Q. Well --

A. And I estimated a cost for each one of those.

Q. So, then, did you deduct the cost of doing the JEDEC standard product from your estimate of doing the fixed CAS latency?

A. Of course, the design of the base product is a $10-$20 million effort. To do this derivative -- for instance, the first design of a 256-meg product is a very, very expensive effort. So, to do these derivative products is only a small design effort.

Q. No, I asked you, did you deduct the cost of doing the JEDEC standard product from your estimates for fixed CAS latency?

A. And I just answered it. If I had not deducted it, the cost would be $10 or $15 million.

Q. Okay, let me focus your attention on page 138.

MR. DETRE: Of Peisl's deposition?

MR. DAVIS: Yes, I'm sorry.

BY MR. DAVIS:

Q. Now, I'll focus your attention on the question starting on line 6.

"QUESTION: If you look at Table 2, which is Exhibit 2, you look at the first column, which discusses fixed burst length rather than programmable burst length, okay?"

Then I am going to skip the parenthetical.

"QUESTION: Looking at the costs that are listed in this column as well as the total costs, are there costs in there that you would agree with or disagree with?"

There are some objections, and the witness answers:

"ANSWER: I would disagree with the same issues I mentioned before. The product design is no add-on," and there's a number of others.

Dr. Peisl disagreed with you on every alternative for design costs, didn't he?

A. I don't know that.

Q. You don't recall?

A. I don't know that. You just specified -- specifically talked about a burst length design alternative here.

Q. Now, Dr. Peisl supervised design teams designing the 256-megabit SDRAM and DDR SDRAM parts in the mid-1990s. Do you remember reading that in his deposition?

MR. DETRE: Objection, Your Honor. There is no foundation for the --

JUDGE McGUIRE: Sustained.

MR. DAVIS: Mr. Geilhufe already stated that he

understood that from the deposition. I was just establishing a foundation for the next question.

JUDGE McGUIRE: Well, I don't know. I don't know what he said. I've sustained the objection.

BY MR. DAVIS:

Q. Now, part of Dr. Peisl's job had been to estimate the design costs for the DRAMs. Do you recall reading that?

MR. DETRE: Objection, Your Honor. Mr. Geilhufe has no foundation to say what Dr. Peisl's job was or wasn't.

MR. DAVIS: I'm asking if he recalls reading that in his deposition, not if he knows Dr. Peisl's job.

JUDGE McGUIRE: I will hear it on that very tight basis, then.

THE WITNESS: I do not -- it's a large document. I do not recall reading that.

BY MR. DAVIS:

Q. Let me direct your attention to page 41 and line 22.

"QUESTION: During your --" and I'm reading from line 22 on page 41.

A. Um-hum.

Q. "QUESTION: During your tenure at Infineon,

have you had to make estimates of manufacturing costs for any products that you were involved in?

"ANSWER: I did once estimate for design effort, meaning we had head count, for the 16-megabit

A. Just like I did.

Q. -- and that's what he did as part of his job as well?

A. That's what he says, and it's interesting, only for one product. I find that a very unusual statement.

Q. Actually, he said that for a number of products.

A. Oh, good.

Q. But you didn't see a need -- I mean, you and Dr. Peisl disagreed on what the design costs were, didn't you?

A. I don't know what Dr. Peisl estimated for a design cost for what element.

Q. Well, we can go through all the other ones I guess. So, we did fixed CAS latency and fixed burst length. We read Dr. Peisl's testimony on those two, correct? Just a few minutes ago.

A. We only read it for one alternative, I believe.

Q. No, we read it for two. Let me try it again. If you go to 74, page 74, line 15.

A. Um-hum.

Q. He's talking about the design costs for a fixed CAS latency part, correct?

A. Correct.

Q. If you go to page 138, line 6, he's talking

about a fixed burst length part?

A. Right.

Q. Well, let's go to page 105, line 2. Are you there?

A. Bear with me, I apologize. There we go.

Q. "Would designing --" I'm sorry, "Would using -- would designing a product with electrical fuses add to your design costs versus just using laser-blown fuses?

"ANSWER: No."

So, there's another example where Peisl disagrees with --

A. That's now a third example, yes, we now have three.

Q. Would you go to page 159?

A. Yes.

Q. Starting at line 22:

"QUESTION: Do you have any idea based on your experience how much it would cost to double the data width on an SDRAM in 1998?"

There were some objections.

"ANSWER: If I go through the rows again for the product design, I would maintain that there was zero add-on. With a good die yield, I would agree that there was some critical die area," and I could keep on reading, but we're talking about design.

So, that's another area where he disagreed with you on the DRAM design?

A. That's correct. That's his testimony.

Q. If you would go to page 154, starting on line 9, "If you look at the first column in Exhibit 3, there's a number of costs -- a number of costs for implementing that particular alternative. Assuming costs in the mid-1990s of volume product, and that alternative was implemented for SDRAM at the time the JEDEC specification was set, do you have an opinion one way or the other as to whether these cost increases are accurate?

"ANSWER: Based on my experience, the product design add-on would be zero."

Now, for that alternative, if you turn to the previous page, 153, you'll see that he's talking about interleaving on chip memory banks.

A. Excuse me?

Q. If you turn to page 153 --

A. Yes.

Q. -- at the very bottom --

A. Um-hum.

Q. -- he says, "Had you --" you can see that the question was related to on-chip memory banks and using two blocks as an alternative to dual edge clocking

technology.

A. Oh, that is a very surprising statement for someone knowledgeable in design. If you're adding a clock, you better do some design.

Q. So, he disagreed with your -- with your conclusions, so you're just saying that he's wrong. Is that right?

A. I disagree with his conclusions.

Q. Now, you don't have any -- excuse me.

Now, we were talking about fixed CAS latency and fixed burst length a minute ago. You don't have any negative figures for the design costs for any of the alternatives, correct?

A. That is correct.

Q. That means you thought that none of the alternatives that were proposed by Professor Jacob were cheaper to design than the alternatives in the JEDEC standard?

A. That was my estimate, yes.

Q. And you thought that fixed CAS latency and fixed burst length was more expensive to design than programmable CAS latency and burst length?

A. Because there were different parts that needed to be aligned, it is more expensive in total.

Q. At the time you reached your conclusions, were

you aware that the proponents of SDRAM-Lite at JEDEC were thinking of using a fixed CAS latency of three as late as January of 1996?

A. That's outside the scope of my analysis. I -- I don't see what bearing that has on my cost analysis.

Q. Were you aware that the JEDEC members themselves believed that eliminating the ability to set the latency and burst length would reduce design costs?

A. Please --

MR. DETRE: Objection, Your Honor, misstates the record.

BY MR. DAVIS:

Q. Are you aware that -- withdrawn.

JUDGE McGUIRE: Well, sustained.

BY MR. DAVIS:

Q. Are you aware that Terry Lee testified based on his understanding at the time that the use of fixed CAS latency and fixed burst length would reduce design costs?

A. I am not aware of that.

MR. DAVIS: One second, please.

(Counsel conferring.)

JUDGE McGUIRE: And Mr. Davis, I'm having -- there's often times during this hearing I have trouble hearing people that aren't right up to the podium or at

their table, so you tend to go back and forth, which is okay, but just make sure that I hear you when you do so.

MR. DAVIS: Yes, Your Honor. Unfortunately, I had caffeine this morning or this afternoon, so it makes me move around too much.

JUDGE McGUIRE: All right.

BY MR. DAVIS:

Q. Now, looking at the product design costs for the use of the burst terminate command, you thought that was a fairly complex design change from the current standard? If you want to refer to your tables, that might refresh your recollection.

A. Thank you. (Document review.) Yes, I felt it was somewhat more complex than a simple design change, like implementing fuses.

Q. Did you make any assumptions about the burst length that would be required for use for the burst terminate -- if there was a burst terminate command? For example, did you assume -- let me withdraw that question and ask another one.

Did you assume that the burst terminate command would be required to accommodate a burst interrupt of one?

A. Of course. If you don't have a burst length

register, you would have to interrupt a single data bit, which, of course, is not possible.

Q. And you thought that there would be required to be a burst interrupt to interrupt the burst at a one because it was in the current JEDEC standard?

A. A -- it is a requirement for any DRAM to be able to output a single bit at a time.

Q. I'd like to turn to wafer sort. Now, this element depends on the amount of test time required to test the alternative over the time required to test the current standard. Is that right?

A. That is correct.

Q. And your basis -- I'm sorry, the basis for your opinions for this element was your experience in the DRAM industry?

A. It's -- it's my experience in wafer sort testing for DRAMs and for flash memories, for SRAMs and

Q. You say you were aware. When were you aware?
A. At this time frame.
Q. And that was because of work that you did with the DRAM manufacturers?
A. That is correct.
Q. And that was work that you did with the DRAM manufacturers that I asked you about at your deposition? Do you remember that?
A. I don't remember which DRAM manufacturers you asked me about.
Q. Well, I -- can I have the deposition? Oh, I have it.
Is this confidential information, Mr. Geilhufe?
A. Of course.
Q. It is confidential information?
A. Yes.
Q. So, when I asked you about it -- if I had asked you about it at the deposition, you wouldn't have told me what those would have been, would you?
A. No.
Q. I couldn't have found out what those numbers were from you?
A. It is confidential information that I obtained under confidentiality agreements which I'm bound by.
Q. But other than the confidential information

that I wasn't able to get information about from you, you reviewed no evidence in this case about this cost element?

A. Well, actual data is pretty solid information. So, beyond the actual data, I did not review anything else.

Q. When you read the deposition of Dr. Peisl, he thought that in order to come up with a number for the test costs, you'd have to write up a set of test programs to see for sure whether there would be any change in test costs. Do you recall reading that?

A. I don't recall reading that.

Q. If I could refer you to page 77, line 9.

"QUESTION: Okay, wafer sort, what do you understand that to be?

"ANSWER: Wafer sort is the sorting of good dies -- sorting out the good dies from the bad dies of the wafer according to the test program.

"QUESTION: Do you see here that it says using fixed CAS latency parts would decrease your test time?

"ANSWER: This is what I believe I said five minutes ago, no.

"QUESTION: So, you don't believe there would be any decreased test time for using fixed CAS latency parts --" I'm sorry, it doesn't say fixed, but --

"ANSWER: I have not written a test program in order to assess the differences quantitatively. My feeling would be that it would be absolutely close to zero, because from my experience, tests like CAS latency are built into other tests in parallel. We usually test two or three things in parallel with the same test. So, just waiving this particular CAS latency test would not necessarily change the duration of the test program."

Do you remember reading that?

A. I -- I recall -- I see it reading it now.

Q. You didn't write up any test programs to see whether changing the test time at wafer sort would change for any of the alternatives, did you?

A. No, I did not write any test program.

Q. I'd like to turn to good die yield. Now, to figure out the effect on good die yield of some of the alternatives that you analyzed, you knew that you had to look at some of the changes in circuitry that would be required to implement the alternative as compared to the current standard, correct?

A. I had to make some very rough estimates at that, yes.

Q. But as you testified earlier, you never actually did a detailed design of the circuitry that

would be required to implement it.

A. That's correct, there was no circuit design and no layout done.

Q. And you never really looked at the circuitry that you could remove from the DRAM after omitting the standard feature, did you?

A. I estimated if some circuitry could be removed or some circuitry had to be added.

Q. But you never really looked at the circuitry that you could remove, specific circuitry, did you?

A. Of course. For instance, for the DLL option, I looked at the -- removing the DLL from the -- from the chip.

Q. Did you look at removing the circuitry for the dual edged clocking alternative?

A. I did not.

Q. Once you made the determination that the circuit size would be larger for the alternative than for the original, you assumed that the increase in circuit size would lead to a reduction in yield?

A. Yes, I did.

Q. And in making this determination, you were estimating that what you generally believed to be -- what you -- I'm sorry, strike that.

In making this determination, you're estimating

Peisl's testimony. We would have to go element by element by element.

Q. Do you recall Dr. Peisl disagreeing with your estimates of changes in good die yield for any of the alternatives?

A. Say that again, please.

Q. Do you recall Dr. Peisl disagreeing with your estimates for changes in the good die yield for any of the alternatives?

A. Not specifically, no, I do not.

MR. DETRE: Your Honor, I'm going to object on relevance grounds. We've heard so much from Dr. Peisl's deposition at this point. Mr. Geilhufe has his opinion, and apparently Dr. Peisl had a different one in his deposition. I'm not sure what the relevance is of reading all these in.

MR. DAVIS: Again, the relevance --

JUDGE McGUIRE: Mr. Davis, I will give you a chance to respond to that.

MR. DAVIS: The relevance is that Dr. -- Mr. Geilhufe read Dr. Peisl's deposition prior to testifying here today and giving his opinion. Dr. Peisl is a current practitioner in this same area that Mr. Geilhufe --

JUDGE McGUIRE: Well, so ultimately you're

showing that they don't agree, so they don't agree, and that's in the record. Maybe you could expedite this and ask him if there are some areas in the Peisl testimony that he does disagree with and not have to go through each and every one of them.

MR. DAVIS: I tried that, Your Honor, and --

JUDGE McGUIRE: It is not aiding this Court to understand that they disagree.

MR. DAVIS: The purpose of the cross isn't to show that they disagree, but it's to show that Mr. Geilhufe saw that there was another person who disagreed with him and he didn't do anything to check his estimates, even though he only based them on his experience.

MR. DETRE: I think Mr. Davis has now established that at least half a dozen times. He could ask one question and ask after reviewing the Peisl deposition, did you do any further work based on it, and we could be done with it.

JUDGE McGUIRE: Okay, that's what I'm going to suggest we do at this point, Mr. Davis. We can expedite this if we can clarify your inquiry.

MR. DAVIS: Let me just see the question that Mr. Detre asked.

BY MR. DAVIS:

Q. Now, after seeing the -- after reading the deposition of Dr. Peisl where he disagreed with you in certain parts, did you do any further work based on it?

A. I did not.

JUDGE McGUIRE: See how easy that was?

THE WITNESS: Saved all of us a half an hour.

BY MR. DAVIS:

Q. Now, regarding the possibility of reduced good die yield due to speed distribution for --

A. Yes.

Q. -- for using fixed CAS latency, you said that you thought that there would be some die yield loss for a DRAM manufacturer who made a DRAM with fixed CAS latency of two. Is that right?

A. With any fixed CAS latency.

Q. If he fixed -- if the DRAM manufacturer fixed the CAS latency at the highest CAS latency available, would there be that -- would there have been that good die yield loss?

A. No, at that point, there would not have.

Q. Did you make an assumption of what CAS latency the DRAM manufacturer would be fixing at to arrive at your cost for good die yield?

A. Yes, I used the JEDEC spec CAS latencies for the SDRAM and the DDR RAM.

Q. I think I'm a little confused. With respect to fixed CAS latency, you say that there is going to be three parts manufactured. That's part of your assumption?

A. Yes, I -- my prior answer is confusing indeed. I looked at what the impact would be on the DDR RAM, but for table one, I only looked at the SDRAM and calculated the costs only for the SDRAM.

Q. Well, actually, what I was confused about was something a little different. You said that there's -- for fixed CAS latency, you thought that they'd be making three parts.

A. The JEDEC spec calls out three parts.

Q. Three parts. Now, for the good die yield, you thought the good die yield would be reduced through speed distribution, even though they were making all three parts. Is that right?

A. That's correct.

Q. Could you explain to me how there would be a reduction in good die yield if they're already making all three parts that they would have been making anyway?

A. Very simple. You create a distribution of access times. If you have a programmable CAS latency, the entire distribution can become a product, in other

words, does not get rejected for speed. If you make CAS latency of three, you may use the entire distribution. If you make a CAS latency of three and two, you may not use the entire distribution, because two will have speed fall-out.

Q. So, the good die yield is based on your assumption that the JEDEC standard would be using all three -- I'm sorry, that the alternative would involve all three fixed latencies that are set out in the JEDEC standard?

A. That's generally -- yes.

Q. You also thought that a DRAM manufacturer wouldn't manufacture only a CAS latency three part, even though it might eliminate good die yield reductions, because of all of the extra money that you thought the manufacturer would get from selling the part with a CAS latency of two, for example, rather than three?

A. You're characterizing I believe my testimony accurately.

Q. Okay. And that's because the part with a CAS latency of two is faster than a part with a CAS latency of three?

A. It has greater value to the end customer, and the end customer pays more money for it.

Q. Did you do anything to determine how much of a performance gain there would have been for a CAS latency two device over a CAS latency three device?

A. I estimated the cost differences, and depending on where you are in the manufacturing cycle, early on, those differences are huge, because it's very difficult to make the faster parts, and later on in the cycle, it becomes less.

Q. But I think I asked a different question. Did you do anything to determine how much of a performance gain there would have been for a CAS latency two device over a CAS latency three device in any application?

A. Performance gain? No, I did not do performance evaluations at systems level.

Q. Did you do anything to determine how much more consumers would be willing to pay for a CAS latency two device over a CAS latency three device?

A. I am roughly familiar with what -- with the premiums that can be achieved there.

Q. You are roughly familiar. You didn't do anything to determine what that premium would be, though?

A. I did not specifically identify a given manufacturer, a given part and a given time period.

Q. Now, I'd like to talk about final test and good

existing fuse technology as that fuse technology.

Q. So, would your answer be yes to that question?

Let me ask the question again. That's not a -- it -- you know it's a yes, but it's not good for the record.

You assume that the fuses would have to be burned prior to packaging. Is that right?

A. That is correct.

Q. Now, you have reviewed no evidence related to the cost to DRAM manufacturers for this element for the relevant period, did you, other than the Peisl deposition?

A. I was aware of the equipment and staffing requirements that were in place at final test at one of the major manufacturers, one of the first-tier manufacturers during this time period.

Q. And this is another set of costs that were confidential?

A. That's correct.

Q. And I couldn't have found out about those costs from you at the deposition?

A. That's correct.

Q. Now, I want to talk about inventory costs. You based your inventory cost estimate on your assumption that the number of new part numbers -- of the number of

new part numbers that would be required for a fixed CAS latency and a fixed burst length from the JEDEC standard. Is that right?

A. That's correct.

Q. And after multiplying it all out, you determined that you thought there would be 12 based -- 12 different parts for SDRAM and 15 different parts for DDR SDRAM based on what's in the JEDEC standards?

A. My model for CAS latency only assumed three -- let me make sure I get this right. I assumed only three part numbers, and my model for burst length assumed four part numbers, as the JEDEC spec includes. I did not go to the next extreme, which is the logical extreme of combining or, if you will, multiplying those numbers to a point where, of course, it would be absurd.

Q. So, you did testify this morning that if you did multiply them, there would be 12 and that the cost would be much higher.

A. Exactly.

Q. Now, you never looked at the market today to see how many of those different types of parts are sold, are you -- did you?

A. I did not look in detail at the market today.

Q. And you never saw any evidence from JEDEC

regarding how many different types of DRAMs would have been sold had there been a fixed CAS latency and a fixed burst length?

A. I did not receive any information from JEDEC.

Q. And you never read any testimony, either from deposition or at trial, from a current industry participant regarding how many different types of DRAMs would have been sold had there been a fixed CAS latency and a fixed burst length?

A. I don't recall any specific testimony.

Q. Now, would you have considered it relevant to your opinion if it turned out that only two CAS latency values and two burst length values are used today?

A. If the spec were only two and two, that would be relevant. If the spec is three and four and the usage is different, that would be less relevant, because you'd still have to support all of the part numbers.

Q. So, just so I have an understanding of the answer to my question, you would not have considered it relevant if it turned out that there are only two CAS latency values and two burst length values used generally today?

MR. DETRE: I think that's the same question, Your Honor, and it's been asked and answered.

is in the -- in the spec.

Q. Well, then, my question is, would you have considered it relevant?

A. Of course, if the spec would have been reduced to two CAS latencies, it would have affected the inventory, increased inventory costs.

Q. And if the testimony were that it would be just a single CAS latency or single burst length, would that have been relevant to your costs?

A. If the spec was a single CAS latency and a single burst length, it would have reduced the costs.

Q. I'll take that as a yes.

I want to talk about board complexity. Now, this element is a little different from the other elements that you described today, isn't it?

A. That is correct. It's -- it is not in the area of DRAM component manufacturing. It's in the area of DRAM usage.

Q. It's also different in that you weren't able to come up with a cost number based solely on your own experience.

A. The experience I relied on was my experience as reliability and quality director responsible for a number of manufacturing -- manufacturing plants at Intel while --

Q. But you were -- I'm sorry, I didn't mean to cut you off.

But you needed to go to various web pages to determine which product you thought was going to be necessary to implement the alternative in order to come up with a number for board complexity. Is that right?

A. I needed to -- to develop cost estimates, for instance, for clock circuitry and for multiplexer circuitry to complete the model.

Q. And to develop those cost estimates, you went to the web pages of various companies to figure out which parts would fit in?

A. Yes, and -- yes.

Q. And then you had to determine what the price would be for that component?

A. I tried to establish high-volume pricing if at all possible.

Q. But this is one basis for your opinions that you didn't state in your report, isn't it?

A. I don't understand.

Q. You didn't state the basis for this -- the opinions regarding the cost of these components in your report?

A. I don't believe I specifically stated that I used web pages.

Q. You didn't state that you went to the web pages?

A. I -- I believe you read my report correctly. I

of the components that you estimated for --

A. I do not recall those --

Q. You have got to let me finish my question, Mr. Geilhufe.

You don't remember the part numbers for any of the components that you put in for the board complexity aspect of your -- of your opinions?

A. I -- not off the top of my head. Part numbers are six, seven, eight digit long things, and I do not recall that.

Q. And you had those part numbers in your notes, didn't you?

A. Somewhere, yes.

Q. But you didn't bring your notes with you to the deposition, did you?

A. No.

Q. So, you couldn't tell me from your notes what the part numbers were?

A. No.

Q. You also didn't recall for sure which companies made the products that you were -- that you were using, did you?

A. When?

Q. At the deposition.

A. Oh, at the deposition? I believe I specified

one or two companies, and others I didn't recall.

Q. You thought that Arrow might have been one of the companies you contacted as a distributor?

A. That is correct.

Q. But you didn't remember who you spoke to at any of the companies?

A. No.

Q. Now, in your direct, you didn't mention the part numbers that you got the prices for, did you?

A. No, I did not.

Q. Have you -- and you don't recall what the price numbers -- I'm sorry, what the part numbers are sitting here today?

A. No, I do not.

Q. Did you bring your notes with you today so that you could tell me what part numbers you got the prices for?

A. I do not -- I did not.

Q. So, if I wanted to check on whether the part numbers that you identified were the appropriate part numbers to solve the problems that you identified or that Dr. Jacob identified, I wouldn't be able to do that from the information you provided me, would I?

A. I -- since I did not provide --

JUDGE McGUIRE: I think he's answered that now

about five times, Mr. Davis. Let's get off the part numbers.

MR. DAVIS: Okay.

BY MR. DAVIS:

Q. In your analysis of Professor Jacob's double clock frequency alternative for dual edge clocking, you testified that you thought that an on-DIMM clock would be required to adequately -- I'm sorry, accurately position the clock. Isn't that right?

A. That is correct.

Q. And you were referring to an on-DIMM PLL or DLL?

A. On-DIMM PLL or DLL clock circuit, maybe more than a PLL/DLL.

Q. You didn't do any timing analysis to ensure that you were correct in your assertion that an on-DIMM clock or an on-DIMM DLL would be required, did you?

A. I made hopefully the good technical assumption if we're removing a DLL from the chip, and we certainly would need some -- a DLL on the DIMM, but I did not make the timing -- detailed timing analysis.

Q. And just so we're clear, for this alternative, I was -- I wasn't talking about removing the DLL. I was talking about doubling the clock frequency.

A. I apologize for the wrong answer.

Q. But that doesn't change your answer, does it?

A. No, it doesn't.

Q. Now, in coming up with your cost for the clock PLL or PLL or DLL, you didn't look to see what the cost of similar components were for either register DIMMs or for the Kentron's QBM DIMMs?

A. I made an attempt to identify the cost for the Kentron DIMMs, and interestingly enough, the high-speed DIMMs are not available, and information about them was only available via nondisclosure agreement, which suggests that the product is not yet commercially available.

Q. The cost for the PLL is not -- I was talking about the cost for the PLL, and that's not available you're saying?

A. The Kentron solution. You asked specifically about the Kentron solution, and that's the answer I'm giving.

MR. DAVIS: Can I have one second, Your Honor?

JUDGE McGUIRE: All right.

(Counsel conferring.)

BY MR. DAVIS:

Q. I'd like to show you what's been marked for identification as CX-2613.

May I approach, Your Honor?

A. May I put my glasses on?

Q. You can look at the screen, actually. I think it's on there.

A. Okay. So, that's -- that puts us in September of 2002.

Q. Now, this is the QBM Kentron DIMM that you were referring to earlier in your answer just a minute ago.

A. That is -- that is correct.

Q. Now, could you turn to page 7 of the exhibit, and the top slide there, do you see a table?

A. Yes.

Q. Refer to the first column, which says QBM533.

A. Correct.

Q. And focus on the third row from the bottom. Do you see it says, "PLL," and the cost is $2?

A. Right.

Q. Did you see this document prior to putting together your opinion in this case?

A. I believe I saw this document, yes.

Q. Okay. And you didn't include this as a -- did you consider this as part of the cost of PLL?

A. Of course. I actually tried to establish what the PLL cost at Kentron is, and the response was I needed to sign a nondisclosure agreement to get that -- access to that information.

Q. So, it wasn't good enough to see the $2 in the presentation; you wanted to get what they considered confidential information on what the PLL cost was?

A. Mr. Davis, I have generated hundreds of marketing presentations, and I've seen thousands, and just because a number is on a slide does not mean it is either available or it's -- actually a transaction has taken place at that price.

Q. So, you didn't believe that $2 price?

A. I have no judgment. I could not confirm it.

Q. And did you consider the cost for PLLs for registry DIMMs?

A. I did not review specifically the costs for register DIMMs.

Q. Now, with your -- I'm sorry, with your cost estimate for the clock/PLL that we were talking about, the -- you think the double clock frequency alternative would cost about 28 cents more than the dual edge clocking alternative?

A. That is correct, that's what I projected in my model.

Q. And 24 cents of that 28 cents comes from that PLL?

A. Approximately 24 cents.

Q. Now, I'd like to talk about a few of the actual

technology alternatives themselves.

Now, let's look at some of the -- some of your overall conclusions regarding the costs of some of these alternatives. You think that a fixed CAS latency and fixed burst length would increase costs by 6 cents and 4 cents, respectively, over the JEDEC standard, the current JEDEC standard technology?

A. That is correct. That's what I've shown on the table.

Q. Now, you'll recall earlier we talked about SDRAM-Lite a little bit?

A. I don't believe SDRAM-Lite -- yes, you asked questions about it.

Q. Did you know that in 19 -- that there's testimony to the effect that in 1995, fixed CAS latency and fixed burst length parts were being proposed as part of the SDRAM-Lite standard to lower costs relative to the current standard?

A. I'm not aware of that, and of course, SD-Lite is not a significant DRAM product, so history or the actual marketplace has decided that that's -- was probably incorrect.

Q. You didn't review the SDRAM-Lite proposals?

A. I did not.

Q. And you didn't talk to anybody who was at JEDEC

who reviewed those proposals?

A. I did not talk to anyone at JEDEC. You don't need to ask that question again.

Q. Now, let's talk about voltage levels via pin to set CAS latency and burst length. Is it accurate for me to say that virtually all of the costs for this alternative are based on your assumption that additional pins would be needed to implement this alternative?

A. My analysis and testimony did not address voltage levels of the pins.

Q. I see what you're saying. You're looking at voltage level, multiple voltage levels.

A. That is correct, yes.

Q. I'm referring to the analysis that you did of burst length via pins and CAS latency via pins.

A. Okay, that has nothing to do with voltage levels, just the pin.

Q. Two voltage levels, right?

A. Right.

Q. It's fair to say that virtually all of the costs -- in fact, all of the costs for this alternative are based on the assumption that additional pins would be required to implement this alternative. Is that right?

A. That is correct.

Q. And you base that assumption that more pins would be required on your reading of Professor Jacob's report?

A. Professor -- Professor Jacob suggested using additional pins, and I identified how many pins would be required to support the three bits for CAS latency and three bits for burst length.

Q. But you didn't do anything to ensure that it was the case that you actually did need more pins to -- to use this alternative, did you?

A. Professor Jacob did not suggest any other -- excuse me. No, I did not.

JUDGE McGUIRE: Thank you.

BY MR. DAVIS:

Q. You didn't look at any JEDEC -- I'm sorry, at the JEDEC standard to see if there were standard packages that had no-connects that could have been used?

A. Of course, I did.

Q. And you found that there were packages that had multiple no-connect pins when you did that, correct?

A. I found as part of the JEDEC standards that all the standards used either at the 44 or the 54 or the 66 pin level, they used up all the pins in the highest

density cases. So, the standard used up all the pins in the highest density cases.

Q. Well, I'm not sure I understand that answer. Let's look at CX-234, which is the JEDEC standard, you should have it in front of you still, and I'm talking about page 83.

A. What's the page number?

Q. Page 83.

A. Um-hum.

Q. And this is a -- are you at that point, page 83?

A. I'm on page 83.

Q. And this is a schematic or a drawing of the pin-out for the 16, 32 and 64-meg x4 SDRAM in TSOP-2. Is that right?

A. That's correct.

Q. And if you look at that picture, there are open or no-connect pins at 17, 25, 43 and 53. Is that right?

A. That's correct.

Q. So, there are four open pins; there are four no-connect pins in this particular pin-out.

A. On this particular version.

Q. So, there would be 16 options, is that right, 16 options for CAS latency and burst length using this

particular -- this particular pin-out?

A. Only for this configuration of DRAM. The standard provides for all configurations of DRAM, and other configurations, of course, don't have any -- have four -- do not have four pins available.

Q. Could you turn to page 80?

A. Eighty, yes.

Q. And this is a two-meg x4.

A. Yes, much smaller SDRAM.

Q. And this is an SDRAM rather than a DDR SDRAM, right?

A. That's correct.

Q. And there are open pins for or no-connect pins on 30 and 34 there, correct?

A. Correct.

Q. So, that's four options, not as many as the first time, but --

A. Right, but again, the SDRAM spec does not confine itself to a 16-meg x4. It covers the range of densities, so we have to look at the worst case packaging situation.

Q. But this SDRAM spec was put together along with the assumption that there would be a mode register. Isn't that right?

A. Correct.

Q. Now, with respect to your table -- you can take that off -- with respect to your tables describing fixed costs, those are one-time costs. Is that right?

A. That's correct, one-time costs per product type.

Q. Per product type?

A. Per product part number, if you will.

Q. So, you'd only -- for example, for the design, you would spend the money for the design, and then you'd have the design.

A. That -- that is the model there.

Q. You wouldn't be spending another $250,000 or $100,000 next year to do the same design; you've already got that. Is that right?

A. That is why this es pr ght? pr castsnservatin; you've D o esThat iighpr castsnservatin; yolYou' ca(eT(s place(D o es

that right?

A. That's correct.

Q. Is it 20 million units of output of DRAM, is that what you were referring to?

A. 20 million DRAMs.

Q. Is that 20 million DRAMs per year?

A. That's 20 million DRAMs for that particular iteration.

Q. 20 million -- oh, that's what I didn't understand. So, it's 20 million DRAMs for the entire iteration; for the life of that product, there would be 20 million DRAM.

A. For that iteration; that is, if you did a shrink, it would be a separate iteration.

Q. But I thought that this was a -- based on a mature product, that there weren't going to be any more shrinks after --

A. It's possible that there are further shrinks, but I -- I assumed that 20 million units could be built off that one design effort.

Q. So, there could be further shrinks off of the design that you talked about?

A. Potentially.

Q. Okay. Going back to the double clock frequency for a second?

A. Yes.

Q. If you want to take a sip of coffee, go ahead.

A. I appreciate it.

Q. You said that you thought a DLL or PLL type chip would be required on the module to distribute the clock. That's why you added that component to the DIMM.

A. That is -- that is correct.

Q. What clock frequencies were you assuming would be used?

A. 200 megahertz.

Q. 200 megahertz. Did you look at the DDR 400 modules currently on the market to see if they used PLLs or clock chips or DLL-type chips on the module?

A. I think I already testified that I did not look at the register modules.

Q. Well, no, I'm not talking about the register modules. I'm talking about the unbuffered, unregistered modules, DDR 400. Did you look at those modules?

A. I did not -- I looked at a whole series of Samsung -- I may have looked at them. I don't recall.

Q. Those modules, the clock speed for those modules is 200 megahertz, right?

A. Right, but doubling the 200 megahertz goes to

400 megahertz. We're now operating at twice that speed.

Q. Right. So, it's -- the clock speed for that module is 200 megahertz?

A. The -- let's be very precise. We're doubling clock speed here. 200 megahertz clock speeds, it now needs to operate at 400 megahertz, and I believe that requires an on-DIMM clock generator.

Q. So, you were assuming a 400-megahertz clock when you put together this table or a 200-megahertz clock when you were putting together this table?

A. The dual edge clock alternative operating at 200 megahertz requires a 400-megahertz clock in this alternative.

Q. Yeah, I'm just asking what you assumed when you were putting together your table. Were you assuming the clock would be going at 200 megahertz or were you assuming it would be going at 100 megahertz or were you assuming that it would go at 400 megahertz? I just want to know how fast the clock was going.

A. Okay, the actual clock was going at 400 megahertz, and I looked at a range.

Q. 400 megahertz for the clock alternative?

A. Yeah.

Q. Now, did you know that Mark Kellogg of IBM

testified that they expect to be able to run a clock at two and a half gigahertz in the near future?

A. I -- I read all kinds of good things in the literature and people tell me all kinds of good things. I wouldn't be surprised if somebody said that today. This is 2003.

Q. Did you talk to Mark Kellogg or anyone else about whether PLL would be required on the DIMM in order to implement that?

A. In the 1999 time frame, I did not.

Q. In any time frame?

A. I did not.

Q. Now, one of the things you mentioned early today when I first started asking you questions was that you had read some documents -- you recalled reading some documents and you might have read some testimony, but you weren't able to recall who. Do you remember that testimony?

A. That's correct.

Q. I just want to give you some names and ask you if you recall reading testimony of these people.

Do you remember reading the testimony of Desi Rhoden?

A. I may have seen it, a piece of it or -- I don't -- I certainly don't remember reading the whole

thing.

Q. Do you recall reading any of it?

A. How do you spell the last name?

Q. R H O D E N.

A. I believe -- I may have seen a piece of it.

Q. You don't have any specific recollection of the piece, but you think you might have read it?

A. No, I do not.

Q. I understand. Do you recall reading any testimony of Howard Sussman?

A. I don't recall.

Q. Do you recall reading any testimony from Mark Kellogg?

A. I may have seen some piece of testimony of his.

Q. Okay, but you don't recall specifically?

A. I don't recall specifics, no.

Q. Did you read the testimony of Terry Lee?

A. I don't recall.

Q. Did you read the testimony of Joe Macri?

A. I don't recall.

Q. And did you read the testimony of Andy Bechtolshein?

A. I did not. That one I didn't.

Q. You would have remembered his name?

A. I'd remember that.

Q. Did you read the testimony of Kevin Ryan?
A. I did not.
JUDGE McGUIRE: All right, it would be a lot easier if we just asked him what he did read.
MR. DAVIS: I asked him, and he didn't remember.
JUDGE McGUIRE: Okay, then he's answered it.
MR. DAVIS: Actually, I just finished the last one.
JUDGE McGUIRE: Lucky for you.
BY MR. DAVIS:
Q. Now, each of the alternatives to dual edge clocking that Dr. Jacob proposed --
A. Yes.
Q. -- none of those alternatives would end up using both edges of a clock, right, that you evaluated? So, you might want to just look at that --
A. Oh, I would totally disagree with that. You can't utilize two banks without using both edges of the clock.
Q. Okay. So, other than that first alternative, the on-chip memory banks, the remaining alternatives didn't use both edges of the clock. Is that accurate?
A. In one form or another. The precise timing of bringing data out, with the exception of doubling the

data with going around, it would require bringing data out on the two edges of the clock.

Q. Okay.

I may be very nearly done, Your Honor.

Now, the last alternative that I think I want to talk about, and I want to make sure that it's the last one, but I believe it is, is -- is the programming the values for CAS latency and burst length of fuses, one we were talking about this morning.

A. Okay.

Q. Now, with respect to the alternative of programming CAS latency in fuses, you assume that the alternative involved was to use laser-blown fuses to set the --

A. That's correct, because that's existing technology at that time.

Q. And you didn't think any other type of fuse technology was feasible for DRAMs?

A. At -- at the time frame of 1995, I believed -- yes, I did not believe there was any other technology that was feasible.

Q. In fact, you thought that anti-fuse technology wasn't even feasible today. Isn't that accurate?

A. Anti-fuse technology is less reliable than laser-blown fuse technology, and it carries with it a

risk.

Q. So, you thought that anti-fuse technology has a reliability factor which is inconsistent with the cost objectives with something as complicated and expensive as DRAM manufacture. Is that right?

A. Yes, that is my belief.

Q. And you also thought that the need for an additional application module also meant that DRAM manufacturers wouldn't use the technology on DRAMs, correct?

A. If the anti-fuse technology module is not available in the DRAM process, then I would think a manufacturer would resist or not implement it, because it would add cost.

Q. You don't think they would add the module, in other words.

A. Just for fusing, because the DRAM manufacturers already have laser-blown fuse technology in place. Unless there is a compelling cost or reliability or performance improvement, one wouldn't implement it.

Q. You didn't review any evidence in this case regarding whether DRAM manufacturers actually used anti-fuses to set -- to do their redundancy work that you were referring to?

A. I became aware of testimony on Friday that

Micron currently is using some anti-fuse technology.

Q. And this was something that you didn't know when you were -- when you were writing your opinion?

A. No, I was aware that Micron was using anti-fuse technology for some parts, but not in the 1995 time frame.

Q. Did you know when they were using it?

A. I estimated it to be somewhere in the '98, '97-'98 time frame.

Q. Okay, but you said in your deposition that you thought that anti-fuses were -- first of all, that you -- you said that they had a reliability factor which is inconsistent with the cost objectives of something as complicated and expensive as DRAM manufacturer, in your deposition you said that, right?

A. Right.

Q. But you knew at the time you said that that Micron was actually using fuses for that purpose?

A. Oh, and it is still my belief that that may, indeed, be a special skill either that Micron has or a special yield loss that Micron deals with.

MR. DAVIS: Your Honor, could I take a five-minute break to make sure? I think I may be done.

JUDGE McGUIRE: Okay, good enough. Three minutes.

(Pause in the proceedings.)

JUDGE McGUIRE: Mr. Davis, any further cross?

MR. DAVIS: No more questions.

JUDGE McGUIRE: All right, thank you very much.

Did you want to follow up, Mr. Detre, redirect?

MR. DETRE: Yes, Your Honor, just a few questions.

JUDGE McGUIRE: Okay.

REDIRECT EXAMINATION

BY MR. DETRE:

Q. Mr. Geilhufe, do you recall Mr. Davis asked you about the margin of error in connection with some of your estimates?

A. Yes, I do.

Q. Now, when you were making your estimates in this case, were you trying to be -- were you trying to err on one side or the other?

A. I -- I attempted to be as realistic as possible but err on the serve of conservatism.

Q. Okay. Is that the practice you generally followed when you were making these estimates in the industry?

A. Clearly those of us who have to take responsibility for building stuff that we project have to be fairly conservative in our estimates.

Q. Some of your cost estimates involved estimating the costs of a pin in the 1995 time frame, correct?

A. That is correct.

Q. What -- and you estimated that at about a penny a pin. Is that right?

A. That is correct.

Q. What would you say the margin of error is with respect to those pin estimates specifically?

A. Those were quite accurate since those were industry standard numbers at that time period, so certainly within 10 percent.

Q. Now, Mr. Davis asked you some questions about whether you could, in connection with some of your alternatives, remove circuitry from a DRAM. Do you recall those questions?

A. Yes.

Q. And you testified you took that into account?

A. Yes, I did.

Q. Now, specifically, or let's go to fixed CAS latency, if we went to fixed CAS latency, could you remove all or --

A. One second.

Q. I'll let you get there.

With respect to fixed CAS latency, could you remove all or any part of the mode register if you

employed that alternative?

A. Of course not. The mode register serves a series of purposes, not only CAS latency. It serves the purpose of CAS latency, burst length, burst type, test mode. In the SDRAM, it's a 22-bit long register.

Q. Now -- so, you couldn't remove the whole thing, but could you remove the bits that are specific to CAS latency?

A. Indeed, you certainly could remove -- if you go to a fixed CAS latency, you could take the 22-pin -- bit register and lower it to 19 bits.

Q. What --

A. Which --

Q. -- what would the cost savings be in removing three bits from the mode register?

A. Totally negligible. It would probably include removal of 36 to 40 transistors on a chip that has 10 million transistors. It's a completely negligible effect.

Q. Now, you mentioned that it was a requirement that every DRAM be able to output a single data bit. Do you recall that testimony?

A. That's correct.

Q. Why is that?

A. Single word addressing is a requirement of some

applications. Some other applications take data streams and bursts; other applications require a great deal of random access memory. Let's recall what we're dealing with. We're dealing with a random access memory, which suggests you can get to any word independently.

Q. How does that apply to, say, DDR SDRAM?

A. In the DDR SDRAM, of course, because it clocks out two bits in a single clock cycle, it brings out two words at the same time. That's its minimum increment.

Q. If -- could we put up DX-298, please?

With respect to programming CAS latency with fuses, you testified that there would be reduced yield due to speed distribution. Do you recall that testimony?

A. That's correct.

that was what was in the JEDEC spec. Do you recall that?

A. That's correct.

Q. Did you think that it was appropriate to look at what was in the JEDEC spec as opposed to what parts are in use today?

A. Of course. The JEDEC spec determined the requirements that the industry and the DRAM manufacturers, the DRAM consumers, the software writers, what have you, felt was necessary to go forward. The JEDEC spec is a document that addresses several generations of product. It addresses a lengthy time period. And at that time, there was no information whatsoever as to which one of the CAS latencies would be prevalent or if only a few would be prevalent.

JUDGE McGUIRE: Mr. Davis?

MR. DAVIS: Your Honor, move to strike everything after "of course," Mr. -- for foundation. Mr. Geilhufe stated he didn't know anything about JEDEC, didn't interview anybody about JEDEC, didn't review any documents about JEDEC.

JUDGE McGUIRE: I'll let you answer, but I'm inclined to --

MR. DETRE: Mr. Geilhufe did say he looked at

the JEDEC spec. He didn't say he looked at other JEDEC documents, but he did say he looked at the JEDEC spec, and this only goes to why he used that spec in a certain way.

JUDGE McGUIRE: Is that your understanding of his testimony, Mr. Davis?

MR. DAVIS: If that is his understanding of his testimony, he can talk about what was in the spec, but that's not what his answer gave.

MR. DETRE: Well, what was in the spec was three latency values, and --

JUDGE McGUIRE: It's the question that I was looking at, not what was in the spec. I will hear it on that basis, only what was in the spec and what he had reviewed in the spec.

BY MR. DETRE:

Q. You'll recall, Mr. Geilhufe, that Mr. Davis was asking you some questions about anti-fuse technology.

A. That's correct.

Q. Do you know whether there were DRAM manufacturers in the 1995 to 2000 time frame who did not have anti-fuse technology available?

A. I'm aware of one major one that definitely did not, and I -- it's -- I believe several other ones did not.

Q. Okay. Which one are you aware of that definitely did not?

A. At that time, Samsung definitely did not.

Q. That's based on your own personal experience with Samsung?

A. Yes, and this is public information. This is not confidential information.

Q. Okay. Now, if you've got CX-234 in front of you, Mr. Geilhufe, that's the JEDEC spec, Release 9. Could you pull that up?

A. Yes.

Q. I'll just wait for it to come up on the screen, CX-234.

Could you turn to page 84 of that document, 84 of the exhibit?

A. Yes.

Q. There are certain SDRAM configurations shown on this page. Do you see that?

A. Yes, I do.

Q. And there is in particular a -- the outer ring of this diagram shows a particular SDRAM configuration?

A. That is correct.

Q. Could you check whether there are any no-connect pins available there?

A. That configuration does not have any

no-connects.

MR. DETRE: No further questions.

JUDGE McGUIRE: Okay, Mr. Davis, any recross?

MR. DAVIS: Thank you, Your Honor.

RECROSS EXAMINATION

BY MR. DAVIS:

Q. Mr. Geilhufe, you -- in response to questions from Mr. Detre, you talked about the practice in the industry to be conservative in estimates regarding cost. Do you remember that?

A. Yes.

Q. And that was as a customer, you were in a sense buying DRAM from people who were manufacturing it for you, where you were in control of the plants or whatever, but you were talking about the costs of those products. Is that correct?

A. I'll give a broader answer. I view that both as a manufacturer for cost analysis in an internal fab factory and for contract acquisition of manufacturing capacity where you're purchasing the capacity from the outside. So, it's both conservative on the high end and low side.

Q. Conservative on the high end, okay.

Now, if you -- I'd like to refer you to the mode register page on the JEDEC standard, Release 9.

A. What page is that, please?

Q. Which I believe it's on page 150 of CX-234, and that's the SDRAM and SGRAM mode register?

A. That's correct.

Q. And in fact, it also has the DDR CAS latency values there as well. Is that right?

A. That is correct.

Q. And the DDR burst length values are there as well, correct?

A. That is correct.

Q. Okay. Now, if you removed as an alternative the burst length and the CAS latency from the mode register, what would be left -- you would be left with is the BT register, I guess, which is number three there, is that right, bit number three? That's all that would be left.

A. Okay.

Q. Now, one of the things that you said in your redirect was that you had to have a burst length of one, right, that was a requirement for DRAMs?

A. Yes, random access.

Q. Could you show me where on this, on this mode register, a burst length of one is specified in the mode register?

A. Yes, 000.

Q. 000 for both SDRAM and DDR SDRAM establishes a burst length of one. Is that accurate?

A. It -- this only specifies it for SDR RAM.

Q. So, for DDR SDRAM, 000 in those bits actually is reserved?

A. It's reserved, yes, for something else.

Q. And 001 for DDR and for SDR is a burst length of two. Is that right?

A. That is correct.

Q. So, DDR doesn't even have a burst length of one specified in that -- in the mode register.

A. Of course, double data rate suggests you get two bits or a nibble per access.

Q. And if you look at the SDRAM, the SDRAM part of the mode register for burst length, do you see the one there is in parentheses?

A. Yes.

Q. Do you know what that means?

A. According to the -- no, I don't. I don't recall.

Q. Okay. If you look at the very bottom, and actually, for some reason it's covered up, at the bottom of the table, at the bottom of the bottom table -- yes, highlight that, please.

A. Yes, as a matter of fact, I apologize. Of

course, they're options.

Q. It's optional?

A. Yes. It's getting late in the afternoon, Mr. Davis.

MR. DAVIS: No more questions, Your Honor.

JUDGE McGUIRE: Okay, very good, sir. Thank you for your testimony --

MR. DETRE: Your Honor, I have one follow-up question, just one.

JUDGE McGUIRE: You better ask the Court, then, because I haven't gone two rounds.

MR. DETRE: Well, Your Honor, may I ask one follow-up question just to clarify something?

JUDGE McGUIRE: Yes.

FURTHER REDIRECT EXAMINATION

BY MR. DETRE:

Q. Mr. Geilhufe, in response to Mr. Davis' questions, you were talking about how when you were taking cost estimates in the industry, you would be conservative on the high end and the low end. Do you recall that?

A. That is right.

Q. Now, for purposes --

MR. DAVIS: I'm sorry, objection, that misrepresents his testimony, I believe.

JUDGE McGUIRE: I can't even see what you said.

Then restate, Mr. Detre. See, your one question, you messed it up. So, I could ask you to sit down right now.

MR. DETRE: I'll try to do better, Your Honor. I'll withdraw that question, if I may, and ask a different question.

BY MR. DETRE:

Q. For purposes of this case, Mr. Geilhufe, were

morning we will call Mr. Richard Rapp, an economic expert. We are pretty sure it will take the whole day.

JUDGE McGUIRE: Okay, very good. I have got some hard copy up here. We will see you in the morning at 9:30. Hearing in recess.

(Whereupon, at 3:50 p.m., the hearing was adjourned.)

C E R T I F I C A T I O N O F R E P O R T E R

DOCKET NUMBER: 9302

CASE TITLE: RAMBUS, INC.

DATE: JULY 21, 2003

I HEREBY CERTIFY that the transcript contained herein is a full and accurate transcript of the notes taken by me at the hearing on the above cause before the FEDERAL TRADE COMMISSION to the best of my knowledge and belief.

DATED: 7/22/03

SUSANNE BERGLING, RMR

C E R T I F I C A T I O N O F P R O O F R E A D E R

I HEREBY CERTIFY that I proofread the transcript for accuracy in spelling, hyphenation, punctuation and format.

SARA J. VANCE