Annex to the summons to attend oral proceedings

Communication
of the Technical Board of Appeal 3.5.1
pursuant to Article 11 (1) of the rules
of procedure of the Boards of Appeal

[redacted]

1. The Board has made a preliminary study of the present appeal. The f[illegible]

[redacted]

2. The following abbreviations will be used:

O1: Micron Europe Ltd; Micron Technology Italia S.R.L.

O2: Infineon Technologies AG

5. In the following issues are indicated which are expected to be addressed at the

oral proceedings.

The patent proprietor's main request

6. Added subject-matter (Art. 100(c) EPC)

6.1. The opposition division decided that claim 1 as granted contravened Art. 123(2) EPC (cf Art. 100(c) EPC). The discussion has concentrated on the issue of whether all the features of claim 103 as originally filed should be included in the claim. It has been argued that features 2a, 2b, M1, M2, 3 and 3a (cf the feature listing annexed to the present communication) should be present in claim 1. Th

7.2. In the appeal proceedings the opponents have concentrated on two newly filed documents, D29 and D30.

7.3. D29

Reference is here made to the arguments by the patent proprietor in the letter dated 25/9/2003, p.15 onwards. The following questions have been raised among others:

a) Does the expression "a semiconductor memory device" in claim 1 cover

separate chips, and in particular four "64 K RAM parts" and an MCU (D29, col. 4, l. 10-16)?

Even if claim 1 did not cover this, it is not clear to the Board why it would be

The connection means seems to be present in D29 and D30 as well.

The patent proprietor's second auxiliary request

11. Additional subject-matter

[redacted]

See above under main request.

12. Inventive step

12.1. Compared with D29

Claim 1 specifies that the value in the access-time register is established by data

[redacted]

sent over the external bus. If this bus is taken to correspond to the MACD bus in

[redacted]

13. Additional subject-matter

It is noted that claim 1 of request IV and claim 1 of request VI both relate to subject-matter very similar to that of original claim 103.

14. Inventive step

The additional features in these requests primarily specify the bus to which the semiconductor memory device is connected. Since D29 describes a bus to which a plurality of semiconductor devices are connected in parallel, the bus having a plurality of bus lines for carrying substantially all address, data and control information, there being substantially fewer bus lines than the number of bits in a single address, these additional features are not expected to add anything new

Claim 103 of WO (as annexed to the minutes of the oral proceedings before the opposition division):

1 A semiconductor device,

2 capable of use in a semiconductor bus architecture including

2a a plurality of semiconductor devices

2b connected in parallel to a bus

[redacted]

substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to the bus,

M2 and has substantially fewer bus lines than the number of bits in a single address,

[redacted]