UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

IN THE MATTER OF

RAMBUS INCORPORATED.

DOCKET NO. 9302

**BRIEF OF AMICI CURIAE
MICRON TECHNOLOGY, INC.,
HYNIX SEMICONDUCTOR, INC.,
AND INFINEON TECHNOLOGIES AG**

[PUBLIC]

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MISCELLANEOUS

Based on requests by Complaint Counsel and by Rambus, Amici devoted substantial resources to this proceeding. In response to subpoenas for documents and

members to opt for other, non-proprietary technologies in JEDEC's standards (*i.e.*, to "design-around" the patent rights) or, at the very least, negotiate the best royalty rate they can *before* incorporating the technology into a standard. CCPFF 2101.

This is the way all three Amici understood the JEDEC policy. CCPFF 319, 324, 330, 358-418; CX 42A. This is the way JEDEC officials understood the policy. CCPFF 324, 358-418. This is the way that all the fact witnesses who testified before the ALJ -- including Rambus itself -- understood the policy. CCPFF 357-418, 820. *See also* Rambus Mem. In Support of Its Renewed Motion for Judgment as a Matter of Law at 10 (May 31, 2001) (attached hereto as Exhibit A). ("Rambus acknowledges it had a duty to disclose … all of its actual patents relating to SDRAM to JEDEC . . . "). And this is the way the Federal Circuit understood the policy. *Rambus, Inc.*, 318 F.3d at 1098 ("this court likewise treats this language [of the JEDEC patent policy] as imposing a disclosure duty."). Only the ALJ -- and now, conveniently, Rambus's counsel – understand it differently.

Rambus is a monopolist - this even the ALJ concedes. Initial Decision ¶ 1018. Rambus gained this monopoly by knowingly breaching its duty of disclosure and engaging in exclusionary conduct. Rambus went to JEDEC meetings as a member, learned what was being considered by fellow members, and then secretly wrote and filed patent claims that attempted to "read on" the standards under consideration. CCPFF 822-48, 867-70, 1125-1237. Rambus *intended* to "mire" the industry "in a big intellectual property trap." Crisp, Tr. 3531. It did so by lulling JEDEC members into a false belief that they were adopting standards on which Rambus would *not* have any claims. In fact, Rambus withdrew from JEDEC to avoid disclosing that it had pending patent rights that

it believed were relevant to

2101-464. Cost-effective, technically viable alternatives were available. *Id.* Through Rambus's conduct, however, Amici and JEDEC were denied this opportunity.

Amici -- and the customers and consumers they serve -- stand to lose mightily if Rambus's scheme succeeds. Collectively, Amici manufacture nearly half of all DRAMs sold worldwide. CCPFF 80. Billions of dollars have been invested in "fab" plants that principally produce JEDEC standardized DRAM products using technology Rambus now claims to own. Rambus has threatened not to license Amici under its patent rights at all if it wins, and at the very least plans to charge Amici far higher royalty rates than the rest of the industry. If Rambus restricts the output of DRAM technology in this way, competition will be sharply curtailed and prices will certainly rise to the detriment of customers and millions of consumers.

The harm from Rambus's behavior reaches far beyond JEDEC and DRAM technology. When SSOs in any industry enjoy the good faith of their participants, their activities have pro-competitive outcomes. Rewarding Rambus's subversion of the standards-setting process can undermine future participation in SSOs, as Joseph Simons, former Director of the FTC Bureau of Competition, noted when the FTC's complaint was filed:

> The conduct at issue here . . . threatens to undermine participation in
> industry standard-setting activities more generally . . . By issuing this
> complaint, the Commission is sending a signal not only to Rambus but
> also to other companies. The message is this: If you are going to take part
> in a standards process, be mindful to abide by the ground rules and to
> participate in good faith.

Amici depend upon the good faith participation of fellow JEDEC members as standards are being adopted. Rambus blatantly violated the rules of fair play in JEDEC, and its actions harmed – and are continuing to injure – Amici, customers, and consumers. The ALJ ignored or did not appreciate the substantial weight of the evidence that supports the FTC's antitrust claim. Numerous JEDEC participants testified at length about JEDEC's patent policy and the expectations of JEDEC members. Numerous industry members testified about alternatives to Rambus's claimed technology, about how the industry is locked-in to the current standards, about the industry's adoption of those standards without disclosure from Rambus that it believed it had patent rights covering the standards, and about how the industry would not have adopted the current standards had Rambus made the disclosures that were required and expected of JEDEC members. In his decision, the ALJ did not comment on much of this evidence. Indeed, the ALJ appears to have ignored the testimony of industry members. Nowhere in the initial decision does the ALJ weigh the evidence or explain why he did not accept it.

When the full record, including industry testimony, is considered, Rambus's scheme and its anticompetitive consequences are manifest. Amici respectfully request that the Commission consider the evidence and overturn the ALJ's initial decision.

BACKGROUND

A.   JEDEC

JEDEC is a voluntary standard-setting body that sets standards for the semiconductor industry. CCPFF 200-05. This case concerns JEDEC's JC 42.3 committee, which develops standards for DRAM. CCPFF 10-11, 234. Each amicus was

a member of JEDEC and participated in the JC 42.3 committee throughout the time period relevant to this case.

46410. Internal Rambus emails in 1993 described filed patent claims as expressly "directed against SDRAMs." CX 1959 at R 202996. Rambus closely tracked the work of JEDEC and aggressively sought to amend its pending patent applications to target the emerging SDRAM standard. CCPFF 800-1121.

From the outset, Rambus's outside patent counsel warned Rambus of a "potential equitable estoppel problem" arising from Rambus's disclosure duty as a member of JEDEC. CCPFF 422, 821, 850-51. Rambus's outside counsel emphasized to Rambus that it "cannot mislead JEDEC into thinking that Rambus will not enforce its patent." CCPFF 889. Rambus's counsel also advised the company that even if it did nothing but remain silent at JEDEC meetings, it ran a risk that its patents would be unenforceable. CCPFF 889.

Rambus said nothing to JEDEC about its pending patent applications or its belief that its patent rights covered SDRAM. Instead, Rambus concealed its patent rights while the JC 42.3 committee proceeded to agree on and publish an SDRAM standard in 1993. JEDEC's SDRAM standard included numerous features that Rambus believed were covered by its patent rights. CCPFF 917-18, 926. At the same time, Rambus affirmatively misled JEDEC about its patent rights. In May 1992, the Chairman of JC 42.3 asked Rambus's JEDEC representative, Richard Crisp, to comment on whether Rambus patent rights covered the two-bank design of the SDRAM standard. Rather than give a straight answer, or state that Rambus's patent rights covered SDRAM (as Rambus believed), Mr. Crisp declined to comment on the matter one way or the other. In September 1993, Mr. Crisp disclosed a recently issued Rambus patent, U.S. Patent No. 5,243,703, to the Committee. CCPFF 971-73. Rambus made this disclosure even though

the '703 patent was unrelated to the work of JEDEC. CCPFF 971-73. This disclosure was misleading, because it gave JEDEC the false impression that Rambus intended to comply with JEDEC's patent disclosure rules – an intention Rambus never had.

D.   Rambus Plots to Capture JEDEC's Next Generation SDRAM Standard

In the late 1980's and early 1990's, IBM made a proposal to JEDEC that involved doubling the data rate of a DRAM. Kelley, Tr. 2584-85. Rather than adopt this feature at that time, JEDEC reserved it for future discussion.

E. Rambus Leaves JEDEC

As the next generation SDRAM standards took shape in 1995, Rambus understood that JEDEC's rules would require it to disclose its pending patent applications that related to features being proposed for the new standards. CX 2088 at 174. At the same time, Rambus's outside counsel held a series of meetings with Rambus executives in late 1995 and early 1996. CCPFF 1083-85. Rambus's outside counsel's notes from the time period state: "No further participation in any standards body . . . – do not even get close!!" CCPFF 1086.

Rambus concluded that it would leave JEDEC rather than disclose that it had patent applications relating to the work of JEDEC. CX 2088 at 174 ("one of the reasons . . . why Rambus left JEDEC was that it did not want to disclose its pending patent applications . . . ."); CX 2074 at 465 (Rambus CEO Geoff Tate: "Q: Was the -- was your awareness of JEDEC's policy requiring disclosure of patents and patent applications a factor in Rambus's decision to withdraw from JEDEC? A: Yes."). An email from Mr. Crisp to Rambus CEO Geoff Tate and others at Rambus in late January 1996 stated: "So, in the future, the current plan is to go to no more JEDEC meetings due to fear that we have exposure in some possible future litigation." CX 858 at R 234663; Crisp, Tr. 3358.

On June 17, 1996, Rambus sent JEDEC a withdrawal letter. The letter advised that "Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus," which "may not be consistent with the terms set by standards bodies, including JEDEC." CX 888 at R 157080. And while drafts of the letter stated that Rambus was providing a list of "all issued US patents" held by Rambus, *see* CX 873, 874, 876, 880 (emphasis added), the final version of the letter

stated merely that it enclosed "a list of Rambus U.S. and foreign patents." CX 888. In fact, the list omitted a Rambus patent -- the '327 patent. At the time Rambus withdrew, *this was the only issued patent of Rambus that had claims targeting the next generation SDRAM standards.* CCPFF 1114, 1216-37.

Rambus today argues that the omission of the '327 patent was an oversight. However, this explanation does not add up. First, unbeknownst to JEDEC, Rambus edited the withdrawal letter in ways that show it was concealing information about its patent rights. The phrase "in the interest of full disclosure" was also removed from the final version of the letter. The phrase "[i]n addition, there are numerous pending applications relating to high bandwidth memory and signaling technology" was replaced with "Rambus has also applied for a number of additional patents in order to protect Rambus technology." CX 880, CX 887; Crisp, Tr. 3386-87. Second, on the very same day that Rambus sent its withdrawal letter to JEDEC with a list of patents that omitted the critical 16-37.

NOT tell customers/partners that we feel DDR may infringe – *our leverage is better to wait*." CX 919 (emphasis added). Rambus understood that its leverage in eventual royalty negotiations would depend on the ability of its targets to adopt alternative technologies. Thus, Rambus made the calculated decision to wait to assert its patent claims against the standards until after JEDEC had adopted the new DDR SDRAM standard and the industry had irreversibly committed to DDR SDRAM as the next generation of computer memory.

Finally, in late 1999 or early 2000, Rambus for the first time told a DRAM manufacturer that Rambus believed its intellectual property claims covered SDRAM (or DDR SDRAM). CCPFF 1241. At that point, the industry was no longer able to adopt alternatives to the SDRAM and DDR SDRAM features over which Rambus claimed patent rights. As explained below, the industry had numerous alternatives to these features available to it early in the standardization process, permitting viable design-arounds at that time. But by the time Rambus finally revealed the scope of its intellectual property claim in late 1999 or 2000, the industry was locked in to using these features and could not change them. After JEDEC looked into whether it would be feasible to change the SDRAM and DDR SDRAM standards, and after determining that it would not be, the industry was left with only two options: capitulate to Rambus's royalty demands

ARGUMENT

I. **The Evidence, Including Rambus's Own Admissions, Overwhelmingly Contradicts the ALJ's Position that Rambus Had No Obligation to Disclose its Relevant Patent Rights.**

The ALJ's tortured construction of the JEDEC patent policies is contradicted by

2. Every JEDEC Participant to Testify Understood that the Disclosure Rules were Mandatory, Not Voluntary.

The trial of this proceeding lasted 54 days, including live testimony by 44 witnesses and deposition testimony by many others. A large number of JEDEC participants testified, including the Chairman of JEDEC's Board of Directors, JEDEC's President (who also serves as General Counsel of EIA and who is responsible for providing legal counsel to JEDEC), and individuals with decades of experience attending JEDEC meetings on behalf of a wide array of companies representing virtually every segment of the industry. *Not a single witness testified that the JEDEC rules were voluntary.* Rather, every one of these witnesses, including Rambus's own witnesses, testified that the JEDEC rules imposed mandatory disclosure obligations.

This testimony came from JEDEC officials and consultants, as well as from representatives of DRAM manufacturers, DRAM buyeof DRAM EDEC Pa1.1(oce)4.a0iV(vo8TD

meetings for Micron since the mid-1990's. CCPFF 319-20, 324, 330-32; Kellogg, Tr. 4973; CX 2057 at 200, CX 3136 at 132-42. The testimony of these witnesses establishes beyond any serious doubt that all JEDEC members, like Rambus itself, understood that they had mandatory disclosure obligations.

None of this conclusive evidence can be undermined by a few instances in which other JEDEC members did not disclose a patent or application that related to a proposed JEDEC standard. Another company's imperfect compliance with JEDEC's rules does not negate the existence of those rules. Moreover, there is no evidence that the companies identified by the ALJ as having failed to comply with the policy (*e.g.*, IBM, HP, Micron), *see* Initial Decision ¶¶ 691-700, 708-10, ever attempted to do what Rambus did here – enforce the undisclosed patent rights against a JEDEC standard.[4] Whenever a JEDEC member tried to enforce undisclosed patent rights against JEDEC standards, JEDEC and its members made clear that such conduct was unacceptable and a violation of JEDEC policy. *E.g.*, CCPFF 424-32 (Texas Instruments' failure to disclose and attempts to enforce patent rights against Quad CAS standard), CCPFF 409, 434 (Wang's failure to disclose and attempts to enforce patent rights against SIMM standard). JEDEC

members testified in this case that failure to disclose patents or applications at JEDEC can result in forfeiture of the right to enforce intellectual property rights against the standard. CCPFF 422 (citing testimony of JEDEC Board Chairman Desi Rhoden, Micron Technology CEO Steven Appleton, and Micron Technology JEDEC participant Terry Lee). The ALJ ignored this testimony.[5]

What this testimony demonstrates is that members of JEDEC recognize that it is

1081, 1085, 1098 (Fed. Cir. 2003). Thus, in stark contrast to the ALJ, the Federal Circuit concluded that "Rambus's duty to disclose . . . encompassed any patent or application with claims that a competitor or other JEDEC member reasonably would construe to cover the standardized technology." *Id.* at 1100.

B.   The JEDEC Policy Required the Disclosure of Both Patents and Applications that Might Be Involved in the Work of JEDEC.

The ALJ makes much of supposed inconsistencies in testimony regarding whether the disclosure policy extended to patent applications as well as issued patents, the type of JEDEC activity triggering disclosure obligations, and the requisite connection between the patent rights and the JEDEC activity. Despite the large number of witnesses with diverse perspectives who testified, the record is substantially clear on each of these points. The policy requires the disclosure of patent applications as well as issued patents. Disclosure of such patent rights is triggered by any standard-setting work of JEDEC and is not limited to formal balloting. And th

allegations that it had broken JEDEC's disclosure rules, Wang claimed that it did not understand the JEDEC patent policy to apply to patent applications, only to patents. CCPFF 409. This caused immediate concern at JEDEC and sparked an initiative to clarify the patent policy so that it stated what JEDEC members understood: that the patent policy applied equally to patents and patent applications. *Id.; see also* CCPFF 362. As a result, JEDEC published a revised Manual in October 1993 (publication JEP21-I), which included the following provisions:

- "[C]ommittees should ensure that no program of standardization shall refer to a product on which there is a known patent unless all of the relevant technical information covered by the patent is known" to the committee. CX 208, § 9.3

discussed. CCPFF 940-43 (December 1992 meeting), 968 (September 1993 meeting).

Mr. Crisp acknowledged that he received and read a copy of the JEDEC Manual of

Organization and Procedure and understood it to require JEDEC members to disclose

both patents and patent applications that "related to the work of the committee." CCPFF

820, CX 208A (copy of the JEDEC Manual from Rambus's files).

Following the *Wang* dispute, JEDEC's rules requiring disclosure of pending

patent applications were clarified in other ways as well. For example, committee

chairman Jim Townsend circulated memos accompanying the patent tracking list which

referred to the "existing rules of EIA governing *patentable* matters"; his oral

presentations on the disclosure policy routinely referred to both patents and applications;

and the sign-in sheets used at JEDEC meetings stated that "[s]ubjects involving

patentable or patented items shall conform to EIA Policy." CCPFF 366, 370, 377-78

(emphasis added).

Even before the post-*Wang* clarifications, the evidence shows that Rambus itself

understood the JEDEC rules to require the disclosure of patent applications. Following

one of the first JEDEC meetings that Rambus attended, Rambus's Billy Garrett sent an

email to Rambus personnel, which stated: "Fujitsu indicated that they do have patents

applied for, but that they will comply with the JEDEC requirements to make it a

standard!!!" CX 672. In addition, Rambus did not interpret the pre-*Wang* policy

language, which referred to "patents," to apply only to issued patents. Rather, Rambus

generally used the word "patent" to include patent applications as well. CX 545 at R

169929 (Rambus 1992 business plan uses the phrase "the patents are extensive and

fundamental" to refer to patent applications), CX 2088 at 56 (testimony of Rambus CEO

Geoff Tate: "Q: [by Rambus's own counsel]* * * So if some of these business reports talk about patents and intellectual property you are referring to applications for patents, is that correct? A: Right. At the time and even today I get confused.").

Following the *Wang* clarifications, the evidence is clear that Rambus understood perfectly well that the JEDEC patent disclosure policy applied to patent applications as well as issued patents. Mr. Crisp testified that when he read the JEDEC Manual "it was clear that the manual required disclosure of both patents and patent applications" and he understood that JEDEC members "wanted to know about both patents and patent application that might relate to the works that were going on w

1085, 1100 (Fed. Cir. 2003) (emphasis added). The ALJ's finding to the contrary is unsupportable.

2.

C.   The ALJ's Tortured Construction of the JEDEC Disclosure Policies Defeats the Essential Purpose of JEDEC and the Common Understanding of its Members

The ALJ's decision to ignore all of these official and public statements of the JEDEC's intellectual property disclosure policy is based on a series of errors and misunderstandings. For example, the ALJ supposes that the October 1993 JEDEC Manual must be disregarded because Complaint Counsel provided insufficient evidence that it was approved by "EDEC." Initial Decision ¶¶ 627-28. Such a hypertechnical analysis cannot be used to defeat the understanding and reasonable expectations of Amici and every single other JEDEC participant, including Rambus, that JEDEC members had a disclosure obligation. The October 1993 Manual was officially published by JEDEC, was reviewed and approved by the governing JEDEC Council, and was treated by JEDEC officers and members as the controlling manual that governed JEDEC's procedures. CX 208 at Jedec 0009326; CCPFF 403-04, 414, 417.

The ALJ also states that the 1993 JEDEC Manual "does not provide a basis" for the disclosure duty, and he purports to find some "inconsisten[cy]" between the disclosure obligation described in Section 9.3.1 of the 1993 Manual and its reference to the EIA legal guidelines reproduced in Appendix E to the Manual. Initial Decision ¶ 631. But there is no requirement that obligations set forth in JEDEC's Manual of Organization and Procedure have some basis outside of the Manual; after all, the purpose of the Manual is to set forth JEDEC's procedural rules.

And even so, the EIA guidelines set forth in Appendix E to the Manual do provide a basis for the disclosure rule described in Section 9.3.1 of the Manual, and are certainly consistent with Section 9.3.1. Appendix E, echoing the 1990 Style Manual and the 1981

Manual for Committee, Subcommittee and Working Group Chairmen and Secretaries,

states that "[s]tandards that call for use of a patented item or process may not be

considered by a JEDEC committee unless all of the relevant technical information

covered by the patent or pending patent is

ignored the extensive and detailed testimony of JEDEC participants and industry members that feasible alternatives were available and well known in the field. Even Rambus recognized that it should assume that "[t]here are always ways to get around any patent." CX 534 at R 128742.

The alternatives presented to the ALJ were not mere hypothetical constructs

standardization at JEDEC. This testimony stands unrebutted and should be accepted by the Commission.[7]

1. Programmable CAS Latency

Industry participants identified no fewer than three alternatives to programmable CAS latency. All three of them had been proposed for incorporation into the JEDEC SDR SDRAM standard in the early 1990's. CCPFF 2131.

First, the testimony and exhibits established that JEDEC could have standardized fixed CAS latency to avoid Rambus's patent rights. During the relevant time, two of the world's largest semiconductor manufacturers made proposals to JEDEC to make fixed CAS latency a standard. In 1991-1992, Samsung presented an SDRAM proposal that included a fixed CAS latency of 2. CCPFF 2138; JX 10 at Jedec 0014250-53; Rhoden, Tr. 427-30. In 1995, NEC proposed using a fixed CAS latency of 3 in a proposed reduced-feature part called SDRAM Lite. CCPFF 2139, 2142; JX 27 at Jedec 0016621-26. Micron actively supported this proposal. CCPFF 2144. Testimony from JEDEC and industry participants established that fixed CAS latency offered advantages over

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[7] In his decision, the ALJ concludes that complaint counsel, "through the testimony of Professor Jacob" (complaint counsel's technical expert), did not demonstrate that there were viable alternatives to Rambus's claimed technologies. Initial Decision at 312-16. In framing his conclusion this way, the ALJ appears to have believed that only expert testimony on this issue is relevant, and that none of the extensive fact testimony from industry participants was material. The ALJ's view plainly is erroneous in at least two ways. First, unlike Rambus's experts who have little or no relevant technical experience, the industry witnesses who testified about design alternatives have extensive experience in DRAM design and architecture. Rhoden, Tr. 262-65, 283-85, Lee, Tr. 6585-95, Kellogg, Tr. 4937-41, 4971-72. Second, Professor Jacob's testimony is completely consistent with, and in many cases was based on, information supplied by industry and JEDEC participants. In this regard, Professor Jacob's testimony is far more credible than the testimony of Rambus's paid experts, who did not review JEDEC records or interview the engineers who made proposals to adopt alternative technologies. CCPFF 2109-29; Soderman, Tr. 9447, 9472, 9488, 9491, 9503, 9506-07.

programmable CAS latency, because it would be faster and easier to design, cheaper to produce, and less costly to test. CCPFF 2139, 2144; Rhoden, Tr. 476-77 (explaining that fixed CAS latency would "significantly" reduce test costs compared to programmable CAS latency); Lee, Tr. 6632-34, 11008 (testifying about cost advantages of fixed CAS latency). Even though Rambus concealed its patent rights from JEDEC, fixed CAS latency still received substantial support at JEDEC. CCPFF 2143.

Second, JEDEC could have selected CAS latency using a fuse rather than a programmable mode register. Numerous industry representatives testified that fuses had been used to select between different DRAM functions during the relevant time. CCPFF 2159, 2166. Fuses also had been used to repair defective memory bits by many companies for many years. CCPFF 2173-74, 2176. Not surprisingly, therefore, JEDEC received a concrete proposal from Cray in 1992 to use fuses in SDRAMs to select between different CAS latency values. CCPFF 2159, 2162 (discussing 1991 Samsung proposal to use fuses to select between DRAM operating modes), 2167; CX 34 at Jedec 0014695; Kellogg, Tr. 5103-05 (describing Cray proposal to set CAS latency using fuses). In the early 1990's, fuse-selectable CAS latency received substantial support at JEDEC, thereby confirming its viability. Rhoden, Tr. 429-30, 435-36 (describing support and consideration of fuse option). One advantage of fuses was that they allowed DRAM manufacturers to distinguish between faster and slower SDRAMs and thereby fetch higher prices for the faster parts. CCPFF 2165.

Third, JEDEC could have used a pin to select a CAS latency value for SDRAM rather than a mode register. As with fixed CAS latency and fuses, pin-selectable CAS latency was actually considered by JEDEC in the early 1990's. CCPFF 2186. This

alternative plainly was viable, as it received substantial support from JEDEC participants at the time. CCPFF 2187. Indeed, Andreas Bechtelsheim, a vice president and general manager at Cisco Systems, testified that he preferred using a pin to select CAS latency over a programmable mode register because it was "simpler" and "less effort on the system side." CCPFF 2187. Others in the industry agreed that pin-selectable CAS latency would not have cost any more than a programmable mode register and "probably could have been made to work just fine." Polzin, Tr. 3991-92.

2. Programmable Burst Length

In their testimony, industry witnesses and JEDEC participants identified at least three alternatives to programmable burst length, namely, fixed burst length, use of fuses to select burst length, and use of pins to select burst length. CCPFF 2234. During the relevant time, each of these alternatives was presented to JEDEC for incorporation into the JEDEC SDRAM standard. CCPFF 2235.

JEDEC twice considered proposals that called for a fixed burst length. In the early 1990's, Samsung made a proposal to fix the burst length of SDRAMs at 8. CCPFF 2243. Later, in the mid-1990's, JEDEC considered using a fixed burst length of 4 in connection with the proposed SDRAM Lite part. CCPFF 2244, 2250. Fixed burst length received substantial support at JEDEC. CCPFF 2268. This was because fixed burst length would have been easier and less costly to design and test than programmable burst length. CCPFF 2239, 2245, 2246, 2260; Rhoden, Tr. 476-77; Macri, Tr. 4673-74.

JEDEC also considered using fuses to select burst length in SDRAM. In 1992, Cray proposed using fuses to select between two different burst lengths, namely, a burst of 8 and a full page burst. CCPFF 2266. As with a CAS latency fuse option, using fuses

significantly less expensive than on-chip DLL. Kellogg, Tr. 5167-

did not require the lengthy "lock" time needed to initialize on-chip DLLs. *Id.* Mark

Kellogg testified that IBM investigated the data capture issues involved with high speed

DRAMs in the 1995-1998 time frame and concluded that vernier circuits solved more

problems than on-chip DLL. CCPFF 2396. As a result, IBM advocated vernier circuits

at JEDEC. CCPFF 2397. The ALJ's decision never weighs or evaluates this detailed

testimony from credible industry participants who have been working on clocking and

timing issues for years.[9]

4. Dual-Edge Clocking

As with the other features at issue, the evidence at trial showed that JEDEC

actively considered alternatives to using dual-edge clocking in DDR SDRAMs. CCPFF

2324. One alternative about which industry personnel provided extensive testimony

during the hearing is to double the clock frequency but use only the rising edge of the

clock. CCPFF 2324; JX 31 at Jedec 0016839; CX 371 at MR00111843. Desi Rhoden

described a 1996 VLSI presentation at JEDEC which proposed running the SDRAM

clock at higher speeds in order to double the data rate. CCPFF 2322; Rhoden, Tr. 542-

43. Terry Lee of Micron discussed Texas Instruments's 1997 proposals to use a single

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[9] The ALJ rejected vernier circuits as a viable alternative to on-chip DLL because, "upon a formal infringement analysis," verniers "might be determined to be covered by" two U.S. patents, one assigned to Micron and the other assigned to SLDRAM. Initial Decision at 315 and ¶¶1376-77. This analysis makes no sense. To begin with, neither of the patents identified by the ALJ is owned by Rambus. The issue before the Commission is whether JEDEC would have adopted alternatives to Rambus's patent rights had they been disclosed to JEDEC. The existence of patents assigned to companies other than Rambus is irrelevant to that inquiry. Moreover, there is no evidence in the record that Micron or SLDRAM intended to assert these two patents against a JEDEC standard that called for vernier circuits in DDR SDRAM. Any suggestion that either patent would have been asserted against such a standard, and that Micron or SLDRAM would have demanded royalties for the use of vernier circuits, is nothing more than rank speculation. Indeed, there is no evidence that Micron or SLDRAM have ever tried to enforce undisclosed patent rights against the use of a JEDEC standard.

edge of a faster clock (either double the speed of the system clock or use an on-chip clock doubler). CCPFF 2333-35. The evidence showed that this alternative was entirely viable. In fact, industry witnesses testified that using a single edge of a faster clock may have been easier to implement than using both edges of a slower clock. This is because single-edge clocking does not require a 50-50 duty cycle or slew rate symmetry, whereas dual-edge clocking does. CCPFF 2327-28. High speed clocks and clock doublers were available, technically feasible, and acceptable from a cost point of view. CCPFF 2329; Lee, Tr. 6712-14, 6799.

B. The ALJ's Conclusion that There Were No Viable Alternatives Is Based on Groundless Testimony from Rambus's Paid Experts.

Rather than credit the testimony of JEDEC participants and a cross-section of industry members about the viability of alternative technologies, or even weigh the testimony, the ALJ ignored it completely. In its place, the ALJ accepted wholesale the testimony of Rambus's paid experts, Donald Soderman and Michael Geilhufe, that the alternative technologies were not viable because they would have cost more than Rambus's claimed technologies or would not have worked. At the same time, the ALJ completely rejected the testimony of Professor Bruce Jacob, much of which was corroborated by industry testimony and contemporaneous documents. In doing so, the ALJ fundamentally erred.

made clear that JEDEC could have developed alternatives that could have "competed within the market effectively by making different cost performance trade-offs." CX 2109 at 77. The ALJ completely ignored this testimony.

Second, the testimony of Rambus's paid experts that various alternatives would not have worked is entirely unsupported. For example, relying on Rambus's experts, the ALJ concludes that using a data strobe to capture data was not a viable alternative to an on-chip DLL. Initial Decision at 202, ¶¶1381-84. Nowhere in the decision, however, does the ALJ cite to any underlying facts or data to support this conclusion. This omission is telling, because the evidence of record uniformly shows that most JEDEC members believed that on-chip DLL could be eliminated if a data strobe were used to capture data. CCPFF 2379, 2405-06; MacWilliams, Tr. 4874-75.

Third, the testimony of Rambus's paid experts that the alternatives would have been more costly than Rambus's claimed technology is without basis in the record. For example, Rambus's experts testified, and the ALJ concluded, that the fixed CAS latency alternative would cost more to design and would yield fewer good die than Rambus's claimed programmable CAS latency. Yet this conclusion is directly at odds with the contemporaneous documents and the testimony of those involved in considering the alternatives at JEDEC. The evidence shows that JEDEC considered fixing CAS latency precisely because it would cost less than setting latency through a mode register. NEC's SDRAM Lite proposal states that the reduced feature part, which included only a single CAS latency, would "[s]ave money (for everyone)." JX 27 at Jedec 0016622. Terry Lee, a Micron engineer who was personally involved in evaluating the SDRAM Lite proposals at JEDEC, testified that fixed CAS latency would be faster to design and would provide

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yields that were the same as or better than programmable CAS latency. CCPFF 2139, 2144, 2148. Mr. Lee explained that yields for fixed CAS latency parts would be better because the parts would be less complex to manufacture. Lee, Tr. 11012-13. The ALJ failed to cite any documents or industry testimony showing that fixed CAS latency would have resulted in higher design costs or reduced die yield.

Nor was there any basis for the ALJ to credit the opinions of Rambus's paid experts over industry testimony. Neither Dr. Soderman nor Mr. Geilhufe ever designed an SDRAM or a DDR SDRAM. CCPFF 2113. Neither witness ever attended a JEDEC meeting during the time that JEDEC was standardizing SDRAM and DDR SDRAM. CCPFF 2115. And neither witness adequately considered evidence about JEDEC's investigation and discussion of alternatives to Rambus's claimed features. CCPFF 2117-20. In contrast, the industry witnesses whose testimony the ALJ ignored – Messrs. Rhoden, Kellogg, and Lee, for example – were involved in architecting and designing SDRAMs and DDR SDRAMs, attended JEDEC meetings during the relevant time, and made and debated the merits of alternatives to Rambus's claimed features.

64-megabit SDRAMs than Rambus's experts assumed it would produce. As a result, even if Rambus's total cost estimates were valid (which they are not), Rambus's experts vastly overstated Micron's costs of adopting the alternative technologies.

Witness after witness testified that it would have been relatively easy to implement alternatives to Rambus's claimed technologies in the early- and mid-1990's. CCPFF 2106. Witness after witness testified that the proposed alternatives offered advantages over Rambus's claimed technologies. CCPFF 2107. The ALJ's findings fail to include any reference to or discussion of this testimony, and Rambus's experts failed to account for it. As such, the ALJ's findings should be rejected.

C. JEDEC Would Have Adopted Alternatives Had Rambus Disclosed Its Patent Rights.

The evidence convincingly shows that, had Rambus disclosed to JEDEC that it had patent rights on various features, JEDEC would not have incorporated those features into the SDRAM and DDR SDRAM standards, but instead would have chosen alternative approaches. CCPFF 2101. Even the engineer most closely associated with the SDRAM mode register – Howard Sussman – testified that he would have voted to fix CAS latency and burst length had he known there was Rambus intellectual property covering programmable CAS latency and burst length. Sussman, Tr. 1416-17.

This testimony is fully corroborated by JEDEC's actions during the relevant time. When JEDEC knew that Rambus patent rights might cover a proposal, JEDEC rejected the proposal and adopted alternatives that it believed were not covered. This happened in March 1997, when NEC proposed using a loop-back clocking scheme in connection with a DDR SDRAM proposal. JX 36 at Jedec 0017154. When NEC illustrated its proposed

clocking scheme, JEDEC members strongly objected on the grounds that Rambus might have intellectual property relating to a loop-back clock, which was depicted in Rambus's '703 patent (the one Rambus patent that was on JEDEC's tracking list at the relevant time). JX 36 at Jedec 0017154; Rhoden, Tr. 527-28, Lee, Tr. 6694-96. To avoid this issue, Micron presented an alternative clocking scheme to JEDEC in April 1997 that did not include a loop-back clock, namely, a bi-directional data strobe. CX 368 at MR 0073366-69; Lee, Tr. 6698-99. In supporting its proposal, Micron stated that "Loop back strobe could have intellectual property problems," a clear reference to Rambus. CX 368 at MR 0073367; Lee, Tr. 6699. This contemporaneous evidence strongly shows that when JEDEC was made aware of Rambus's patent rights, JEDEC took affirmative steps to avoid them.[10]

III. The Industry is Now Locked-in to the Existing SDRAM and DDR SDRAM Standards.

Reaching conclusions at odds with the testimony of virtually every JEDEC and industry participant, the ALJ found that the industry is not locked-in to the current SDR and DDR SDRAM standards. He did so even though one witness after another testified that changing the standards after Rambus asserted its patent would impose enormous inventory and opportunity costs on the DRAM manufacturers and would cause tremendous disruption and upheaval among DRAM users. The ALJ's findings are contrary to the evidence and common sense and therefore should be rejected.

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[10] This is consistent with JEDEC's conduct in dealing with others' efforts to enforce undisclosed patent rights against a JEDEC standard. For example, when JEDEC discovered that Texas Instruments asserted patent claims against the Quad CAS standard, JEDEC began the process of rescinding the standard. CCPFF 423-32.

A. Rambus Recognized Before Trial that the Industry Is Locked-In

It is only common sense to expect that, after an industry adopts a standard and develops complementary products and infrastructure that depend upon the standard, the industry would incur enormous costs if it suddenly were forced to change the standard. While the ALJ apparently did not appreciate this, Rambus itself did. Rambus's own documents show that it well understood the difficulties involved in avoiding patents that cover a standard after the standard has been adopted.

In 1997, JEDEC actively was debating what the next-generation memory standard should be after SDR SDRAM. One of those possible standards was DDR SDRAM. In 1997, Rambus knew that JEDEC was considering DDR SDRAM as a standard. Rambus also knew that JEDEC had not yet adopted DDR SDRAM as a standard. So, in February 1997, Geoff Tate, Rambus's CEO, prepared a "DDR threat assessment." In the assessment, he stressed to Rambus's officers and employees that they should "*NOT* tell customers/partners that we feel DDR may infringe." CX 919. His rationale? "[O]ur leverage is better to wait." *Id.* In other words, Rambus understood the simple truth that if it did not tell the industry that Rambus had patents on DDR SDRAM, and JEDEC adopted DDR SDRAM as a standard, Rambus would be in a much stronger position to extract monopoly profits because it would be costly for the industry to change the standard after it had been adopted. Inexplicably, the ALJ made no mention of Rambus's own documents in discussing manufacturer lock-in.

B.   Changing the Standards Would Have Imposed Massive Costs on DRAM Manufacturers.

The ALJ simply ignored overwhelming testimony from the industry that DRAM manufacturers were locked-in to the SDR and DDR SDRAM standards because changing them in or after 2000 would have imposed massive costs on DRAM manufacturers.

First, the ALJ ignored the testimony that changing the standard would have resulted in huge inventory costs. Every DRAM manufacturer has a long, costly pipeline of "work in progress" inventory. It is undisputed that it takes approximately 45-60 days to fabricate a DRAM. CCPFF 2535; Becker, Tr. 1131-32. This means that every DRAM manufacturer has, at any moment in time, approximately two months of product in

claimed features from their products and replace those features with alternatives, the manufacturers would have had to devote considerable resources to designing, testing, and qualifying replacement parts – parts that offer no meaningful performance advantage over the parts they are replacing. In other words, rather than spending resources on improving DRAMs by designing faster, smaller, smarter, or less expensive DRAMs, the DRAM manufacturers would be forced to expend valuable resources just to move "sideways" with no real end-user benefits. Numerous witnesses, including Micron CEO Steve Appleton, Micron design manager Brian Shirley, and AMD vice president and general manager Richard Heye, recognized these huge opportunity costs. Heye, Tr. 3744-45, 3810-13 ; Shirley, Tr. 4207-08; Appleton, Tr. 6399-403; Bechtelsheim, Tr. 5881-83; McAfee, Tr. 11294-95. The ALJ completely ignored these costs in discussing lock-in.

C.   **Changing JEDEC Standards Would Have Imposed Enormous Costs on DRAM Consumers.**

By 2000, consumers of DRAMs – microprocessor manufacturers such as AMD, computer manufacturers such as HP, graphics card manufacturers such as ATI and NVidia, and network companies such as Cisco Systems – were fully committed to the SDRAM and DDR SDRAM standards that included Rambus's claimed features. CCPFF 2502, 2504, 2517-20, 2522-24. As a result of this huge customer commitment, changing the JEDEC standards in 2000 to remove Rambus's claimed features would have been virtually impossible. CCPFF 2512 (Appleton: "virtually impossible"), 2514 (Peisl: "near impossible"), 2516 (Oh: "almost impossible"). The reasons are amply demonstrated in the record.

Changing the JEDEC standards for SDRAM and DDR SDRAM to avoid Rambus's claimed features long after the adoption of the standards would have been "disastrous," "painful," and "seriously detrimental" for those in the industry, "extremely difficult" to implement, and "chaotic" to manage. CCPFF 2503 (Krashinsky), CCPFF 2517 (Polzin), CCPFF 2519 (Macri), CCPFF 2521 (Wagner); Polzin, Tr. 4041-42, Peisl, Tr. 4454-57; MacWilliams, Tr. 4875-76. It also would have been hugely expensive. For HP alone, such a change would have cost "millions and millions of dollars in expenses." Krashinsky, Tr. 2781-82. For AMD, the cost of such changes "would get out to the millions." Heye, Tr. 3742-43. For Cisco Systems, the cost to adapt to a change in the SDRAM standard would be in the range of $1 billion. CCPFF 2505. These costs are in addition to the opportunity costs that DRAM users would have incurred to re-design existing systems, existing chipsets, and existing boards. Bechtelsheim, Tr. 5882-83; Heye, Tr. 3810-13.

As industry witness after industry witness explained, any given system that uses DRAM (whether a PC or a network switch or a chipset) is designed and manufactured in light of a specific DRAM memory interface standard. DRAM customers develop products and product platforms that are based on, and integrated with, the DRAM interface standards. CCPFF 2547 (Appleton), 2560 (Heye). Thus, if the SDRAM or DDR SDRAM standard were changed to remove the claimed Rambus features and replace them with alternatives, then all the customers of those DRAMs would have to, at incredible expense, re-design chipsets, modify motherboards, change the BIOS and DIMMs, and re-test and re-qualify all the various system components. CCPFF 2552-53; Heye, Tr. 3732-34, 3742-43; Krashinsky, Tr. 2782-89; *see also* MacWilliams, Tr. 4774-

76, 4781. In addition, products that were designed and sold based on the old DRAM standard immediately would become obsolete, as the products could not be upgraded to use the new memory standard. Heye, Tr. 3745-46.

The ALJ, in finding that DRAM consumers were not locked-in, never cited, discussed, or apparently even considered this body of evidence.

D. The Evidence on Which The ALJ Relied In No Way Suggests that the Industry Is Not Locked-In to the Current Standards.

Rather than consider this direct evidence of lock-in, the ALJ based his conclusion that the industry is not locked-in on a host of irrelevant facts.

First, the ALJ noted that the DRAM industry is constantly designing and "taping out" new SDRAMs and DDR SDRAMs. Initial Decision at 326-27. While true, this fact has nothing to do with lock-in. The new SDRAMs and DDR SDRAMs all comply with the current JEDEC standards. When a DRAM vendor "shrinks" a DRAM (e.g., makes a 0.20 micron 64-megabit SDRAM based on a 0.24 micron 64-megabit SDRAM), the "new" DRAM is interchangeable with the "old" DRAM from the user's standpoint. CCPFF 2539; Becker, Tr. 1156-57.[11] The large number of such "new" DRAMs does not speak in any way to the costs the industry would incur if DRAMs had to be made to a new standard after the industry had made substantial investments in the old standard.

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[11] Significantly, the ALJ ignored testimony that chip "re-designs" – that is, changes to circuits in DRAM of a given density and line width – are very expensive and painful for DRAM manufacturers. Brian Shirley of Micron described the costs associated with re-designing its 256-megabit DDR device after it discovered various flaws in the circuitry. He testified that the re-design was painful to Micron because it took approximately four months, diverted resources away from working on product improvements (opportunity costs), and burdened Micron with out-of-pocket and inventory costs. Shirley, Tr. 4168-70.

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The fact that DRAM manufacturers are constantly shrinking devices merely shows that there is strong pressure to reduce costs.

Second, the ALJ commented that the industry routinely coordinates transitions to new DRAM and PC standards. Initial Decision at 327. Again, this is true but irrelevant to lock-in. Over the years, the DRAM industry has developed new and better memory standards. The standards evolved from fast page mode to EDO to SDRAM to DDR SDRAM. In each case, the transition was "evolutionary" to maximize compatibility between generations, minimize cost, and ease introduction (CCPFF 127-29; Rhoden, Tr. 409-11, Appleton, Tr. 6297-98, Lee, Tr. 6759-60, Wagner, Tr. 3840-41, Polzin, Tr. 3978-80, Kellogg, Tr. 5191-92) was planned to minimize costs and disruption (Appleton, Tr. 6297-98, Heye, Tr. 3804-05) and was driven by performance enhancements (CCPFF 2554). None of those factors applies to an unplanned revision to a memory standard that has already been adopted.

Third, the ALJ noted that most of the cost of any given memory device is spent on the memory array rather than the interface circuitry. Initial Decision at 328. This, too, does not rebut lock-in. The design of the memory array is invisible to the chipset, to the motherboard, to the BIOS, and to the other parts of a system infrastructure. In contrast, the design of the interface circuitry is integral to the design of the chipset, motherboard, BIOS, and other system components, because it is through the interface circuitry that the DRAM communicates with other system components. Indeed, that is why interface circuitry is subject to standards and memory array circuitry is not.

Finally, the ALJ noted that JEDEC considered alternatives to the claimed Rambus features in connection with standardizing DDR-II in 2000. The ALJ inferred from this

patent claims over standardized memory technologies. And the record shows that industry participants were not on notice of the scope of Rambus's patent claims. Rambus itself never said anything to put them notice. And Rambus's own witnesses have testified that the publicly available patent documents were insufficient to disclose the full scope of the patent claims that Rambus would one day assert.

A. **Contemporaneous Rambus Documents Show that Rambus Knew JEDEC Members Did Not Understand that Rambus Had Intellectual Property Claims that Could Apply to SDRAM or DDR SDRAM.**

Rambus's internal documents show a consistent belief inside Rambus, while it was still participating in JEDEC and after it left, that Rambus had successfully managed to keep the industry ignorant of Rambus's belief that its patent rights covered SDRAM and DDR SDRAM, not just RDRAM.

As late as May 1999, Rambus's Vice President of Intellectual Property Joel Karp concluded that JEDEC members "probably think they avoid our IP if they don't go 'packet-based'"—*i.e.*, if they do not use Rambus's proprietary RDRAM architecture. CX 1069.

The emails of Rambus's JEDEC representative Richard Crisp are full of references to Rambus's strategy of hiding the full scope of its intellectual property claims from JEDEC. In early 1995, for example, he wrote of a "big intellectual property trap" for members of standards bodies and stated that "I certainly do not want to bring this intellectual property issue up without careful consideration. I especially do not want it all over JEDEC." CX 783. In another 1995 email he explained why: "it makes no sense to alert [JEDEC] to a potential problem they can easily work around." CX 711 at R 69583; *see also*, *e.g.*, CX 837 at R 233838 (Crisp email discussing Rambus's position with

respect to its patents at JEDEC and advising that "we should re-evaluate our position

relative to what we decide to keep quiet about, and what we say we have").

Importantly, Rambus never stood up at a JEDEC meeting and said that it believed its patent rights covered, or even related to, SDRAM and DDR SDRAM. Rambus had many opportunities to do so. It declined each and every one. Even when JEDEC asked Rambus to comment on whether its patent rights covered a proposed feature, Rambus declined to commit one way or the other. CCPFF 903-05, 1063-66. In declining to comment, however, Rambus misleadingly called JEDEC's attention to the fact that Rambus had reported a Rambus patent to the Committee (a reference to the '703 patent disclosed in 1993), thereby giving JEDEC the false impression that Rambus would comply with its disclosure obligations (when, in fact, Rambus had no intention of doing so). CCPFF 1066. By failing to state its patent position at JEDEC, and by misleadingly suggesting that it would comply with the patent disclosure policy, Rambus effectively concealed the trap it was laying for JEDEC.

During the 1990s, Rambus routinely met with DRAM manufacturers to promote Rambus's technology and negotiate RDRAM license agreements. Rambus witnesses uniformly testified that Rambus never discussed the elements of RDRAM that Rambus claimed were inventive and patentable and never told another company that it had patents that applied outside of RDRAM. CCPFF 1240-43. Rambus's President David Mooring testified that the slides used in presentations with customers would "definitely not have put anybody on notice" of the scope of Rambus's claimed patent coverage. CCPFF 1241. According to Mr. Mooring, the first time that Rambus ever told a DRAM manufacturer that Rambus believed its intellectual property claims covered SDRAM was in late 1999 or 2000. CCPFF 1241.

The witnesses at trial who had attended these meetings on behalf of other indure2t7Theparticipantt tl

2. As Rambus Witnesses Have Admitted, Publicly Available Patents and Applications Could Not Have Alerted JEDEC Members that Rambus Would Assert Claims Against SDRAM or DDR SDRAM.

The ALJ places heavy, but completely misplaced, reliance on the publicly available PCT application, which mirrored Rambus's original US patent application, and the specification of the '703 patent that Rambus did disclose to JEDEC. *See, e.g.*, Initial Decision ¶¶ 826-28, 836-41. Nothing in these documents could permit a reasonable engineer attending JEDEC to conclude that Rambus's intellectual property claims extended to non-RDRAM devices like SDRAM and DDR SDRAM. Indeed, the background sections of the PCT application and the '703 patent describe the wide bus architecture (which is used in SDRAM and DDR SDRAM devices) as a prior art architecture.[12]

Rambus admitted in the *Infineon* case that "the '703 patent and the [PCT] application did not relate to JEDEC's SDRAM work but were directed to the implementation of Rambus's RDRAM products." CX 1801 at 3; CCPFF 972-73. And while the ALJ stresses that the PTO has found the specification of the original Rambus patent application sufficient for patent law purposes to support the claims in subsequent patents that Rambus has asserted against SDRAM and DDR SDRAM, *see* Initial Decision at 284-85, the specification does not delineate the scope of Rambus's claims.

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[12] In fact, the Board of Appeal of the European Patent Office recently revoked one of Rambus's European patents that claims priority to the PCT application on the ground that the patent application did not support claims that cover a non-multiplexed bus architecture. *See* "Rambus loses a European memory-chip patent," USA Today, Feb. 12, 2004 (attached hereto as Exhibit C). The Board of Appeal has not yet issued its written decision, but its preliminary opinion (attached hereto as Exhibit D) expresses doubts about any claim based on Rambus's PCT application that is not limited to devices with a multiplexed bus, which the Board of Appeal described as the "natural entity" of Rambus's application.

To the contrary, the specification is directed toward de

Rambus . . . and in the course of those negotiations, they never claimed or disclosed that they had patents that would relate to any other technology" besides RDRAM although "they would have had a self-interest to do so"). And on two different occasions, when JEDEC members specifically asked Rambus whether it had additional intellectual property claims relating to discussions at JEDEC, Rambus declined to comment. CCPFF 904, 1044, 1064. Yet at the same time, Rambus fostered the appearance that it was complying with the JEDEC disclosure policy when it disclosed its newly issued '703 patent in September 1993. CCPFF 971, 1066; *see also* Crisp, Tr. 3313 (Crisp reminded JEDEC members that Rambus had disclosed the '703 patent and so was "in the category of JEDEC members who had disclosed patents"). Under these circumstances, there was no reason for other JEDEC members to give greater credit to these rumors than to the expectation that Rambus was participating in JEDEC in good faith and complying with JEDEC's rules.

Second, even if such rumors could be trusted, they did not provide a basis for JEDEC to act. One purpose of the disclosure policy is to enable the JEDEC committees to make informed decisions based on solid information, and to avoid the foolhardy game of trying to define important standards on the basis of guesswork and speculation. Such rumors did not obviate Rambus's duty to disclose that it had patent rights to JEDEC. The general rumors cited by the ALJ also did not include information about which specific features of SDRAM and DDR SDRAM Rambus claimed to have invented. Thus, these rumors did not tell JEDEC members which features would be burdened with Rambus royalty claims if adopted and what sort of alternative designs needed to be compared on a cost and performance basis with those features.

And third, one JEDEC member's information about Rambus patents cannot be attributed to the entire organization. Unless these rumors were communicated to the committee (and they were not), they cannot be deemed to have put JEDEC on notice and they could not have saved the integrity of JEDEC's decision making process from Rambus's nondisclosures.

CONCLUSION

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CERTIFICATE OF SERVICE

I, Wilson D. Mudge, hereby certify that, on this the 16th day of April, 2004, I caused copies of the foregoing MOTION OF MICRON TECHNOLOGY, INC., HYNIX SEMICONDUCTOR, INC. AND INFINEON TECHNOLOGIES AG FOR LEAVE TO FILE BRIEF AS AMICI CURIAE and BRIEF OF AMICI CURIAE MICRON TECHNOLOGY, INC., HYNIX SEMICONDUCTOR, INC., AND INFINEON TECHNOLOGIES AG to be served by the method indicated upon the following:

_____

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