PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302** (n[1B529.83.02.9447 -1.1521 TD( )Tj0 T*2.9447 -1.152)T

I. INTRODUCTION

In support of their Appeal Brief, Complaint Counsel have filed two "attachments" and three "appendices." Contrary to Complaint Counsel's representation, neither

arrangement." Attachment 1 at 2. The number of bus lines has grown significantly since Complaint Counsel proposed findings last fall, where they stated that "[a] typical synchronous DRAM bus contains 100-120 parallel lines." CCPF 718. As Rambus pointed out in response, even that number was a gross exaggeration, since the first published SDRAM standard showed *no* configuration of an SDRAM chip with more than *26* bus lines connecting to it. RRPF 718. Certain configurations of RDRAM use 24 bus lines, in the same range as the 21 to 26 bus lines shown in the first published SDRAM standard. RRPF 719.

Complaint Counsel go on to say that, unlike RDRAM, SDRAM "bus lines were not multiplexed." Attachment 1 at 2. This is false. First, as Complaint Counsel's technical expert admitted, certain lines *were* multiplexed in the SDRAM bus architecture. RRPF 1268. While it is true that not all SDRAM bus lines are multiplexed, this is also the case for certain configurations of RDRAM. RRPF 721. Attachment 1 is also misleading in referring to "RDRAM" as if it were a single well-defined technology when, in fact, there were different generations of RDRAM with different numbers of bus lines and different degrees of multiplexing. *Id.*

Finally, Complaint Counsel assert that in an RDRAM system information was sent in "sequential waves of signals," while in an SDRAM system "signals were sent as a simultaneous wave." Attachment 1 at 2-3. In fact, it is not true that all the signals relevant to a given operation were sent simultaneously in an SDRAM system. For example, as Complaint Counsel themselves explain, the row address and column address related to a given read or write operation are sent sequentially in SDRAM systems. CCPF 1306.

B. Complaint Counsel's Attachment 1 Exaggerates SDRAM's Supposed Advantages

The Attachment also confuses the time lines and relative advantages and disadvantages of RDRAM as opposed to SDRAM and DDR SDRAM. Complaint

Counsel refer to SDRAM and DDR SDRAM architecture as “traditional,” as though they

limited and ultimately prevented RDRAM's successful market launch. IDF 526-559; RPF 1548-1602.[1]

RDRAM's lack of success caused substantial consumer harm, since it represented the best solution from a cost/performance perspective. As one of Complaint Counsel's own witnesses -- an Intel executive closely involved in the RDRAM launch -- testified at trial:

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MacWilliams, Tr. 5075 (*in camera*), *quoted* and afforded *in camera* treatment in IDF 557.

III. RAMBUS'S OBJECTIONS TO APPENDIX A

Complaint Counsel's "Glossary of Terms" is not only riddled with errors, but also, under the guise of "objectivity," takes positions on issues in dispute in this matter, without bothering to tell the Commission that the issues are disputed and without bothering to cite to record evidence in support of their position. Some examples of the errors and disputed facts in Appendix A follow; this is not, however, meant to be an exhaustive list of all the errors in Appendix A and does not signify agreement with

[1] Judge McGuire found, for example, that

particular "definitions" that are not addressed below.

A. Auto Precharge

Complaint Counsel provide a nonsensical definition of "auto precharge," stating that precharging "eliminates the data stored in the DRAM in order to prepare for the next operation." Of course, if the next operation were intended, for example, to read data from the DRAM, eliminating all the data beforehand would be ill-advised. In fact, precharging only eliminates the data temporarily stored in one part of the DRAM, the "sense amplifiers," as part of a read or write operation, while retaining all of the data in the memory cells. Moreover, while mentioning that auto precharge is included on both SDRAM and DDR SDRAM, Complaint Counsel neglect to mention that the feature was invented by Rambus and first included on RDRAM.

B. DDR SDRAM Standard

Complaint Counsel's definition suggests that the DDR SDRAM standard consisted simply of adding features to the previous SDRAM standard. This is not based on any evidence in the record and is incorrect; some features of SDRAM were changed or removed by the DDR standard. For example, while a burst stop command could be used during read or write operations in SDRAMs, the command could only be used during read operations in DDR SDRAMs. Likewise, unlike SDRAMs, DDR SDRAMs were not capable of "full page" bursts of data.

Moreover, the statement that DDR SDRAM "was developed during the mid to late 1990s at JEDEC" is contrary to Judge McGuire's findings. First, DDR SDRAM development began outside JEDEC. IDF 372-74, 376-78. Second, DDR development at JEDEC did not begin until December 1996. IDF 371-74, 376-78.

C. Dual Bank Design/Multibank Design

Complaint Counsel's definition suggests that SDRAM and DDR only have two banks. In fact, they generally have four banks.

D. Externally Supplied Reference Voltage

Complaint Counsel state that this technology is included on SDRAM. This is contrary to the Initial Decision which found that "Complaint Counsel did not present evidence sufficient to find that [externally supplied reference voltage] was ever balloted or incorporated into the SDRAM standard." IDF 350.

E.

M. SyncLink

Complaint Counsel's definition of SyncLink is highly misleading in what it chooses to omit. For example, Judge McGuire found that "the SyncLink Consortium was well aware that that their work could or would violate [Rambus intellectual property]." IDC at 308. Complaint Counsel's definition also ignores the findings of fact suggesting that the purpose of the SyncLink Consortium was to block RDRAM by presenting a purported alternative. *See* IDF 484-85. The statement that "SyncLink never achieved significant market penetration," which suggests that there was actually a SyncLink product, is misleading. In fact, SyncLink's chip never went into volume production. IDF 486.

N. System Clock

The statement that a clock signal resembles a sine wave is incorrect. Clock signals are approximations of square waves.

O. Source Synchronous Clocking

The definition states that, in source synchronous clocking, "a clock signal travels

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CERTIFICATION

I, Rebecca A. Williams, hereby certify that the electronic copy of the public version of *Rambus's Objections to Attachment 1 and Appendix A Submitted by Complaint Counsel* accompanying this certification is a true and correct copy of the paper version that is being filed with the Secretary of the Commission on June 14, 2004 by other means.

Rebecca A. Williams
June 14, 2004