

UNITED STATES OF AMERICA  
BEFORE FEDERAL TRADE COMMISSION

COMMISSIONERS:                    Deborah Platt Majoras, Chairman  
   Orson Swindle  
   Thomas B. Leary  
   Pamela Jones Harbour  
   Jon Leibowitz

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In the Matter of                    )  
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RAMBUS INCORPORATED,            )  
   )  
   )                    Docket No. 9302  
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**APPENDIX TO BRIEF OF APPELLEE AND CROSS-APPELLANT**  
**RAMBUS INC.**

Pursuant to the Commission’s October 4, 2004 Order granting Rambus leave to file an appendix, Rambus submits this appendix to its appeal brief containing a glossary of terms.

## Glossary of Terms

**Auto precharge:** DRAMs store information as minute quantities of electrical charge in memory cells – no charge is interpreted as “0” and positive charge as a “1.” Sense amplifiers are circuits on the DRAM that sense the charge in a memory cell and amplify it when information is to be read from the DRAM. Before the sense amplifiers can perform this function, they must be “precharged” to an intermediate charged state. “Auto precharge” is a feature that was originally found in RDRAMs and later adopted by SDRAMs and DDR SDRAMs that allows the controller to determine whether the sense amplifiers are to be automatically precharged – that is, precharged without the need for a separate precharge command – at the end of a read or write operation.

**Bit/Byte:** A bit or “binary digit” is the unit of information used by digital computers that takes on only two values – “0” or “1.” Each memory cell in a DRAM stores a single bit. A “byte” usually refers to eight bits. Since each bit in a byte can take on two values, a byte can take on  $2^8$ , or 256, possible values.

**Bus:** As the Federal Circuit has found, the ordinary meaning of “bus” is “a set of signal lines to which a number of devices are connected, and over which information is transferred between devices.” *Rambus Inc. v. Infineon Technologies AG*

**DRAM:** Dynamic Random Access Memory. DRAM is a form of computer memory that makes up the main memory of most computers and is also used in other products. When one sees a computer advertised as having, say, 128 megabytes or 256 megabytes of RAM, this is referring to the main memory that the CPU uses for temporary storage when executing programs as opposed to, for example, the hard drive that is used for more permanent storage. “Random Access” means that any location in the DRAM can be accessed in about the same amount of time as any other, as opposed to, for example, a tape storage system in which data can only be accessed sequentially. “Dynamic” means that the information stored in the memory cells must be refreshed, that is read from and written back into the memory cells, thousands of times every second in order to retain the information.

**Dual bank design / multibank design:** The memory cells in a DRAM may be organized into one or more banks. The advantage of a dual or multibank design is that one bank may be accessed while others are precharging or performing other operations. RDRAM originally used a multibank architecture. Later, SDRAM and DDR SDRAM also adopted multibank architectures, generally using four banks, although some earlier chips used only two banks.

**Dual edge clocking:** A clock in a computer system refers to an electrical signal that transitions between low and high voltages at a regular rate – the “rising edge” is the transition from a low to high voltage while the “falling edge” is the transition from a high to low voltage – and is used to time operations. RDRAMs have always used both the rising and falling edges of the system clock to read and write data so as to double the data transmission rate. The SDRAM standard contemplates using only the rising edge of the clock, but the DDR SDRAM standard later adopted the dual edge clocking feature.

**Externally supplied reference voltage:** Computer systems determine whether a signal is meant to represent a “0” (low voltage) or a “1” (high voltage) by comparing the voltage of the signal to a reference voltage which is set to a value intermediate between the low and high values. RDRAMs have always received this reference voltage from an external source, that is, they used an “externally supplied reference voltage,” in order to have a more accurate reference than an internally generated reference voltage could supply. An externally supplied reference voltage was not part of the SDRAM standard but was later high volta9:rnan9004(i)1.6(e.000ce at is, wnstit8 T-0.0E.2(puter s9IT-0nst4(-Mh( )Tj0 -1.1382 TD-0c00-0.def.0ee, s 21.3(g8.5not)0 8.5nong:.88 1n “502 mTj-24.47 -20ed an3.0not)0 n3.0no386.ba y to doub179upply. An

**Megahertz:** One million cycles per second.

**Memory module:** A small circuit board that holds multiple memory chips and can be plugged into the motherboard of a computer. The main memory of most PCs consists of DRAM modules, but, in other applications, DRAM chips are sometimes used singly.

**MOST / Mosys:** Mosys was a company founded by a former Rambus engineer that developed the MOST DRAM in the mid-1990s. The MOST DRAM never achieved significant market penetration.

**Multiplexed bus:** As the Federal Circuit has noted, “multiplexing” simply refers to the “sharing of a single set of lines to send multiple types of information.” *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003). RDRAMs, SDRAMs and DDR SDRAMs all use multiplexing. Early RDRAMs multiplexed address, data and control on the same set of bus lines, although later RDRAMs did not do so. SDRAMs and DDR SDRAMs also use multiplexed busses: the lines used to transmit address information are also used to transmit control information (such as autoprecharge information and the data to be loaded into the mode register at system initialization).

**Nanosecond:** One billionth of a second. Light travels approximately one foot in one nanosecond. A frequency of 1 gigahertz corresponds to 1 nanosecond per cycle, while a frequency of 100 megahertz corresponds to 10 nanoseconds per cycle.



**SyncLink:** A specification for a memory technology that began at IEEE in the mid 1990s and was later developed in the private Synclink Consortium. Synclink, which was similar to RDRAM designs in numerous respects, was never commercialized.

**System clock:** A clock in a computer system refers to an electrical signal that transitions between low and high voltages at a regular rate. A “system clock” is a central clock that is used to coordinate the timing of various parts of the system.

**Variable burst length:** “Variable burst length or block size” refers to a feature used in RDRAMs that allows the amount of data to be transmitted by the DRAM in response to a read request (or written into the DRAM in response to a write request) to be varied. This feature was subsequently adopted in the SDRAM and DDR SDRAM standards. In SDRAMs and DDR SDRAMs, a value representative of this amount of data is programmed into a register called the mode register.

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**CERTIFICATE OF SERVICE**

I, Kenneth A. Bamberger, hereby certify that on October 18, 2004, I caused a true and correct copy of the *Appendix To Brief Of Appellee And Cross-Appellant Rambus Inc.* to be served on the following persons by hand delivery:

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**CERTIFICATION**

I, Kenneth A. Bamberger, hereby certify that the electronic copy of *Appendix To Brief Of Appellee And Cross-Appellant Rambus Inc.* accompanying this certification is a true and correct copy of the paper version that is being filed with the Secretary of the Commission on October 18, 2004 by other means.

**Kenneth A. Bamberger**  
**October 18, 2004**