Table of Contents

PUBLIC RECORD VERSION

I. INTRODUCTION[1]

Rambus Inc. is a developer and licensor of computer memory technologies. For more than four years during the 1990s, Rambus participated as a member of the Joint Electron Device Engineering Council (JEDEC), an industrywide standard-setting organization (SSO) that operated on a cooperative basis. Through a course of deceptive conduct, Rambus exploited its participation in JEDEC to obtain patents that would cover technologies incorporated into now-ubiquitous JEDEC memory standards, without revealing its patent position to other JEDEC members. As a result, Rambus was able to distort the standard-setting process and engage in anticompetitive "hold up" of the computer memory industry. Conduct of this sort has grave implications for competition. The Federal Trade Commission (FTC or Commission) finds that Rambus's acts of deception constituted exclusionary conduct under Section 2 of the Sherman Act, and that Rambus unlawfully monopolized the markets for four technologies incorporated into the JEDEC standards in violation of Section 5 of the FTC Act.

Standard setting occurs in many industries and can be highly beneficial to consumers. Standards can facilitate interoperability among products supplied by different firms, which

At the beginning of a standard-setting process, if there are a number of competing technologies, and if any one of them could win the standards battle, then no single technology will command more than a competitive price. Once the standard has been set, however, the dynamic changes. Soon after a standard is adopted, industry participants likely will start designing, testing, and producing goods that conform to the standard. Early in the process of implementing a standard, industry members still might find it relatively easy to abandon one technology in favor of another. But as time passes, and the industry commits greater levels of resources to developing products that comply with the standard, the costs of switching to alternative technologies begin to rise. Industry members may

was locked in. Only then did Rambus reveal its patents – through patent infringement lawsuits against JEDEC members who practiced the standard.[2]

The Commission finds that Rambus violated Section 5 of the FTC Act by engaging in exclusionary conduct that contributed significantly to the acquisition of monopoly power in four relevant and related markets. We further find a sufficient causal link between Rambus's exclusionary conduct and JEDEC's adoption of the SDRAM and DDR-SDRAM standards (but not the subsequent DDR2-SDRAM standard). Questions remain, however, regarding how the Commission can best determine the appropriate remedy. Accordingly, the Commission orders additional briefing for further consideration of remedial issues.

II. BACKGROUND

A. Technology Background

The dispute before us involves four relevant product markets: (1) latency technology; (2) burst length technology; (3) data acceleration technology; and (4) clock synchronization technology. These markets include technologies that, beginning in 1993, have been incorporated into the JEDEC standards for computer memory, and over which Rambus now claims patent rights.[3]

1. The Function of Computer Memory

Main memory – often referred to as random access memory, or RAM – consists of integrated circuits that hold temporary instructions and data for the central processing unit (CPU), the central "brain" of a computer system.[4] The CPU performs each command given by a computer user by extracting instructions from the computer's memory, then decoding and

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[2] Complaint Counsel also allege that Rambus engaged in spoliation of evidence. Rambus instituted a document retention policy that entailed the systematic destruction of a large volume of documents. This destruction policy included documents related to Rambus's participation in JEDEC and Rambus's patent prosecution files. As discussed in greater detail *infra*ssnotd(sol haom tsory)Tj2.013 0 Td(pnizatiquc di by)Tj2.867 0 Tatibecaer our(As)Tj5.0333 Tc -0c 0 T

executing them. Most computers use a type of RAM known as dynamic random access memory (DRAM),[5] which stores and processes information while the computer is on.[6]

DRAM is only one piece in the computer hardware infrastructure. A typical personal computer is built around a motherboard – the main circuit board upon which many of the important components of a computer system are fastened. The motherboard includes, for example, the CPU, chipset, and graphics and sound cards. A computer system also includes a system clock, a power supply, mass storage devices (such as hard drives or CD ROM drives), assorted controllers that enable the computer to connect to external peripheral devices (such as monitors, printers, and scanners), and a main memory system (containing DRAM). The main memory circuits typically attach to the memory module (a small printed circuit board that plugs into the motherboard).[7] Communications between the main memory circuits and the CPU are managed by a memory controller, which generally is part of the chipset.[8] DRAM must be compatible and interoperable with other components in the same computer system.[9]

2. Evolution of RDRAM and SDRAM Memory Technologies: Breaking Through the Memory Bottleneck

In the early 1980s, an imbalance emerged in the speed at which CPU technology was developing relative to memory technology.[10] CPU speeds have doubled every eighteen months for the past two decades,[11] while memory speeds have increased more slowly. This "memory

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[5] DRAM is "dynamic" because it must be refreshed every fraction of a second to prevent memory loss. Rhoden, Tr. 266-67.

[6] Rhoden, Tr. 267-68. DRAM also is incorporated into other electronic devices such as servers, printers, and cameras. IDF 3; Rhoden, Tr. 298; RA 3.

[7] Rhoden, Tr. 269, 272-73; RA 4.

[8] Rhoden, Tr. 275-76; CA A-1; RA 2.

[9] *See, e.g.*, IDF 6.

[10] IDF 27-40.

[11] Farmwald, Tr. 8068 (describing "Moore's law," based on observations by Intel co-founder Gordon Moore regarding the rate of

bottleneck problem"[12] became a widely recognized concern in the computer hardware industry during the early 1990s.[13] The industry considered several different solutions.[14]

One of those solutions – Rambus DRAM, or RDRAM – was developed by Rambus.[15] Rambus was founded in March 1990 by two professors who wanted to commercialize their concept for a new DRAM design that would break the "memory bottleneck."[16] Rambus develops, secures patents on, and licenses technologies to companies that manufacture semiconductor memory devices. Rambus is not a manufacturing company; rather, Rambus earns its revenue through the licensing of its patents.[17]

A month after its founding, on April 18, 1990, Rambus filed Patent Application No. 07/510,898 (the '898 application) with the U.S. Patent Trademark Office (PTO).[18] This application described many of the technologies developed and integrated into the initial RDRAM design. The '898 application also is the original source of the patents that Rambus has asserted with regard to the four technologies at issue in this case. The PTO issued a restriction requirement in late 1990, requiring Rambus to decide which of the multiple claimed inventions it wished to pursue in the '898 application. On March 5, 1992, Rambus responded to the PTO's demand by filing ten divisional applications.[19]

Beginning in 1990, Rambus tried to license its RDRAM technology to manufacturers of DRAM chips and DRAM-compatible microprocessors.[20] Rambus attempted to position RDRAM as the *de facto* standard.[21] Rambus made numerous presentations on RDRAM to the major DRAM manufacturers in an effort to persuade them to adopt the technology.[22] Rambus also tried to develop relationships with major systems companies, and pursued commitments from these companies to introduce systems using RDRAM technology.[23] RDRAM failed to achieve significant market success, however, at least in part because manufacturers were reluctant to pay royalties and licensing fees to Rambus.[24]

These manufacturers rejected RDRAM and instead turned to standards promulgated by JEDEC. JEDEC was a semiconductor engineering standardization body within the Electronic Industries Association (EIA). It comprised manufac

alternative solutions are discussed in greater detail below.[33] JEDEC first incorporated programmable column address strobe (CAS) latency into its SDRAM standard and retained the technology in its DDR SDRAM and DDR2 SDRAM standards.[34] Programmable CAS latency controls data output timing by determining the number of clock cycles that should be allowed to elapse a

as the default and use the memory controller to terminate the burst if a shorter burst length is desired.[41]

Rambus claims that its patents cover JEDEC's implementation of programmable burst length technology.

c. Data Acceleration Technology

Data acceleration technology determines the speed at which data are transmitted between the CPU and memory. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted one particular type of data acceleration technology, known as dual-edge clocking, which captures data off both the rising and falling edges (the "tick" and the "tock") of the clock.[42] This technology enables twice the amount of data to be sent in each clock cycle compared to single-edge clocking, by which data are sent only on one edge of the clock.[43]

When JEDEC was considering whether to adopt dual-edge clocking technology as part of its DDR SDRAM standard, several alternatives were available. As discussed in greater detail below,[44] alternative technologies included interleaving

DRAM with the system clock.[47] Rambus developed a technology that places a PLL/DLL[48] on the SDRAM chip itself.[49] On-chip PLL/DLL clock synchronization technology was incorporated into JEDEC's DDR SDRAM and DDR2 SDRAM standards.

One alternative approach to on-chip PLL/DLL involved placing a PLL/DLL circuit on the memory controller that synchronizes all DRAMs.[50] Another approach involved placing one or more PLL/DLL circuits on the memory module.[51] Still other alternatives involved the use of vernier circuits, which introduce static delays on a signal to reduce timing uncertainties in a memory system, or reliance on a data strobe to signal the memory controller the timing of data capture.[52] These alternatives, which were considered by JEDEC prior to its adoption of on-chip PLL/DLL, are discussed in greater detail below.[53]

Rambus claims that its patents cover JEDEC's implementation of on-chip PLL/DLL technology.

B. Procedural History

1. History of FTC Matter

The Complaint in this matter was issued on June 18, 2002. The Complaint charged that Rambus: (1) monopolized certain memory technology markets through a pattern of anticompetitive and exclusionary conduct; (2) attempted to monopolize these markets; and (3) engaged in unfair methods of competition.[54]

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[47] Jacob, Tr. 5442-43; Kellogg, Tr. 5150-55; RA 4; CA A-3. PLLs use voltage oscillators to synchronize the internal clock with the system clock. *See* Jacob, Tr. 5443, 5616-17; Soderman, Tr. 9401. In contrast, DLLs introduce a variable amount of delay into the internal clock to synchronize that clock with the system clock. *See* Jacob, Tr. 5443, 5616-17; Soderman, Tr. 9401.

[48] Horowitz, Tr. 8607 (Rambus co-founder testified that, under his usage of the terms, "a PLL is the generic term for any circuitry that adjusts phase, so a DLL is a kind of PLL").

[49] Farmwald, Tr. 8117-18; Horowitz, Tr.

The Complaint's allegations focused on Rambus's participation in JEDEC. It alleged that Rambus deceived JEDEC's members by, for example, concealing the fact that it

> was actively working to develop, and did in fact possess, a patent and several pending patent applications that involved specific technologies proposed for and ultimately adopted in the relevant standards. By concealing this information – in violation of JEDEC's own operating rules and procedures – and through other bad-faith, deceptive conduct,

Rambus allegedly conveyed the "materially false and misleading impression that it possessed no relevant intellectual property rights"[55] and that it had no plans to enforce any intellectual property rights that might later become relevant, leaving a materially misleading impression of its intellectual property ownership and plans.[56] The Complaint further alleged that Rambus's conduct resulted in anticompetitive effects including: increased royalties; increased prices for memory products compliant with JEDEC standards; decreased incentives to produce memory using JEDEC-compliant memory technology; and decreased incentives to participate in, and rely on, standard-setting organizations and activities.[57] According to the Complaint, Rambus gave no notice that it intended to claim patent rights over technologies used in JEDEC's DRAM standards, and, by failing to do so, likely affected the content of those standards and/or the terms on which Rambus later licensed its patent rights.[58]

a. Pre-Trial Orders

The case was first assigned to Administrative Law Judge (ALJ) James P. Timony and, upon his retirement, was reassigned to Chief ALJ Stephen J. McGuire.[59] Before retiring, ALJ Timony issued two orders on February 26, 2003: first, an Order Granting Complaint Counsel's Motion for Collateral Estoppel; and second, an Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument. Both orders influenced the trial and ALJ McGuire's Initial Decision.

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[55] *See* Complaint ¶ 2; *see also id.* ¶¶ 54 (alleging deception and bad-faith conduct), 71 (alleging that Rambus conveyed "a materially false and misleading impression").

[56] *See* Complaint ¶¶ 70-78.

[57] *See* Complaint ¶¶ 119-120.

[58] *See* Complaint ¶¶ 62, 65, 69, 70-78, 86.

[59] All references within this opinion to "the ALJ," unless otherwise specifically identified, will refer to ALJ McGuire.

On February 12, 2003, Complaint Counsel filed a motion seeking recognition of the collateral estoppel effect of prior factual findings that Rambus had destroyed material evidence. ALJ Timony granted the motion, thus barring Rambus from re-litigating certain findings of fact made by the district court in prior private litigation, *Rambus Inc. v. Infineon Technologies AG*.[60] Those findings included:

1. When Rambus instituted its document retention policy in 1998, it did so, in part, for the purpose of getting rid of documents that might be harmful in litigation.

2. Rambus, at the time it implemented its document retention policy, … [c]learly … contemplated that it might be bringing patent infringement suits during this timeframe if its efforts to persuade semi-conductor manufacturers to license its JEDEC-related patents were not successful.

3. Rambus's document destruction was done in anticipation of litigation.[61]

Complaint Counsel also moved for default judgment as a remedy to counter Rambus's intentional destruction of documents. ALJ Timony denied the motion, but set forth seven rebuttable adverse presumptions against Rambus. The presumptions included:

1. Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of patents held or applied for by Rambus;

2. Rambus never disclosed to other JEDEC participants the existence of these patents; [and]

3. Rambus knew that its failure to disclose the existence of these patents to other JEDEC participants could serve to equitably estop Rambus from enforcing its patents as to other JEDEC participants.[62]

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[60] 155 F. Supp. 2d 668 (E.D. Va. 2001), *aff'd in part and rev'd in part*, 318 F.3d 1081 (Fed. Cir. 2001). The district court's findings, upon which ALJ Timony relied, were not raised on appeal to the Federal Circuit.

[61] CE at 5 (internal quotations omitted).

[62] Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9 (Feb. 26, 2003).

Four additional presumptions addressed the foreseeability of litigation and Rambus's document retention program.[63]

b. ALJ McGuire's Initial Decision

On February 17, 2004, ALJ McGuire issued his Initial Decision and Proposed Order dismissing the Complaint in its entirety. Specifically, although he noted that Section 5 of the FTC Act authorizes the FTC to define and proscribe unfair methods of competition, the ALJ determined that Complaint Counsel had established no basis for finding a violation of Section 5.[64] He concluded that Complaint Counsel's arguments lacked a reasonable basis in law,[65] and ruled that Complaint Counsel's factual showing was insufficient to establish a violation even if the legal theories had been deemed adequate.[66]

The ALJ found that the adverse presumptions entered by ALJ Timony were not material to the disposition of the case. The ALJ found no indication that Rambus had destroyed any relevant and material documents. He found that the first and second presumptions were moot because Rambus was not required to disclose its patents or patent applications.[67] He also rejected the second presumption on the ground that Rambus's conduct raised sufficient red flags to put members of JEDEC on notice that Rambus had applications pending.[68] The ALJ then found the remaining five adverse presumptions to be irrelevant to the material issues of the case.

The ALJ found that there was no causal link between JEDEC's adoption of Rambus's technology into its standards and Rambus's acquisition of monopoly power. Rather, the ALJ found that Rambus acquired its monopoly power as a result of superior technology and market preferences.[69] Moreover, the ALJ found that JEDEC, and many members of the DRAM industry, were aware of Rambus's patent portfolio. Thus, according to the ALJ, no member of JEDEC

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[63] *Id*. (announcing presumptions that Rambus's document retention program failed to provide adequate guidance and direction to its employees and that Rambus knew or should have known that litigation over the enforcement of its patents was reasonably foreseeable).

[64] ID at 254.

[65] ID at 254-60.

[66] ID at 259-61.

[67] ID at 244.

[68] ID at 244-45.

[69] ID at 300-04.

reasonably could have relied on any misrepresentation or omission by Rambus in its dealings with JEDEC.[70] The ALJ found no basis for ascribing to Rambus an intent to deceive.[71]

The ALJ concluded that the challenged conduct did not result in any anticompetitive effect because Complaint Counsel failed to prove there were viable alternatives to Rambus's technologies.[72] Furthermore, according to the ALJ, Complaint Counsel did not demonstrate that Rambus's conduct had resulted in higher prices to consumers.[73] In contrast, the ALJ found that Rambus had put forth legitimate business justifications for its conduct. He agreed with Rambus that its secrecy regarding its patent applications constituted normal and legitimate protection of trade secrets. The ALJ concluded that this business justification precluded a finding of exclusionary conduct.[74]

Finally, the ALJ found that the DRAM industry never became locked into using Rambus's technologies as incorporated into the JEDEC standards, because "economic evidence shows that switching costs and coordination issues would not prevent the DRAM industry from going to alternatives."[75]

c. Questions Raised on Appeal/Cross Appeal

Complaint Counsel filed a notice of appeal on March 1, 2004. They challenge virtually all of the ALJ's rulings and ask that the Initial Decision be set aside in its entirety. They contend that Rambus acquired monopoly power by pursuing a secret and deliberate pattern of conduct to obtain patents covering JEDEC standards. According to Complaint Counsel, Rambus's course of conduct undermined the fundamental purpose of JEDEC to adopt open standards; contravened JEDEC's procedures for adopting patented technologies only on the basis of full information and after securing a commitment to reasonable licensing terms; breached Rambus's duty of good faith; and also violated Rambus's specific obligation, as a member of JEDEC, to disclose patents and patent applications that might be involved in JEDEC's work.[76] Complaint Counsel claim that the facts and a proper application of the law show that Rambus violated Section 5 of the FTC Act, and they offer a proposed cease and desist order to remedy the alleged violation.

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[70] ID at 304-09.

[71] ID at 295-300, 331-32.

[72] ID at 312-16.

[73] ID at 323-26.

[74] ID at 287-89.

[75] ID at 328, 326-29.

[76] CCAB at 27-28.

Rambus filed a cross appeal arguing that the ALJ erred by applying a "preponderance of the evidence" standard to the government's case, rather than requiring Complaint Counsel to meet a "clear and convincing" burden of proof. Rambus contends that the heightened burden of proof is required due to an "inherent tension" between the interests served by the patent and antitrust laws, as well as by similarities to cases that have required clear and convincing evidence in assessing alleged failures to disclose material information and bad faith enforcement of patents. Rambus also argues that the nature of the remedy sought by Complaint Counsel (which Rambus views as essentially terminating its patent rights), and important policy considerations implicated by SSOs, merit application of the clear and convincing standard.

d. Re-Opening of the Record Before the Commission

The ALJ closed the record on October 9, 2003. The Commission later reopened the record to admit supplemental evidence – entering orders on May 13, 2005, July 20, 2005, and February 2, 2006 – after finding compelling circumstances. The first two orders reopened the record to allow the admission of documents produced in the *Infineon* litigation relating to Rambus's alleged spoliation of evidence, as well as the submission of amended proposed findings of fact and conclusions of law in light of this supplemental evidence. In the third order, the Commission reopened the record to admit documents on Rambus's back-up tapes, described as newly found, from discovery produced during the *Hynix* litigation.[77]

e. Motion for Sanctions

On August 10, 2005, Complaint Counsel moved for sanctions, asserting that Rambus had committed spoliation of evidence. Complaint Counsel asked for entry of default judgment or such other relief as the Commission deems appropriate. Rambus replied on August 17, 2005, arguing that Complaint Counsel failed to prove that Rambus acted in egregious bad faith when it adopted its document retention policy or that the effect of that policy has been to deprive Complaint Counsel of the ability to obtain a full and fair adjudication of this case.

2. Non-FTC Judicial Developments Relating to this Proceeding

Rambus is engaged in myriad litigations involving its efforts to enforce patents it claims cover JEDEC's DRAM standards. Rambus has sued, or been sued by, several of the major DRAM manufacturers, including Samsung, Hynix, Infineon, and Micron.[78] Although Rambus

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[77] For discussion of the *Infineon* and *Hynix* litigation, *see infra* Section II.B.2.

[78] These actions include a variety of patent infringement and antitrust-related allegations. *See, e.g.*, Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW (N.D. Cal.); Rambus Inc. v. Hynix Semiconductor Inc., *et al.*, No. CV-05-00334 RMW (N.D. Cal.); Rambus Inc. v. Samsung Electronics Co., No. CV-05-02298 RMW

and Infineon settled their litigation in 2005, all of the actions involving other companies are ongoing. In addition, the U.S. Department of Justice (DOJ) is investigating whether the major DRAM manufacturers engaged in price fixing in the DRAM market; four of those manufacturers have entered plea agreements.[79] While we will not discuss each of these non-FTC actions in detail, we will highlight certain relevant information.

In late 2000, Rambus sued Infineon Technologies AG, a manufacturer of semiconductor memory devices, in the U.S. District Court for the Eastern District of Virginia for infringement of four patents. Infineon counterclaimed, alleging Rambus committed fraud under Virginia state law by failing to disclose to JEDEC its patents and patent applications related to the organization's SDRAM and DDR SDRAM standards, as required by JEDEC's rules. During trial, Judge Payne granted judgment as a matter of law (JMOL) for Infineon, holding that Infineon did not infringe Rambus's patents. The jury later found Rambus liable for fraud associated with JEDEC's standard-setting activities on SDRAM and DDR SDRAM technologies. In response to post-trial JMOL motions by Rambus, the court set aside the jury's verdict of fraud regarding the DDR SDRAM technology, but let stand the fraud verdict regarding the SDRAM technology.[80] The court then issued an injunction against Rambus and awarded attorney fees to Infineon. Both Rambus and Infineon appealed to the Federal Circuit.

In a 2-1 opinion, the U.S. Court of Appeals for the Federal Circuit vacated the JMOL of noninfringement and remanded the case for consideration under a revised claim construction.[81] In addition, the court reversed the denial of JMOL that had allowed the SDRAM fraud verdict to stand, holding that clear and convincing evidence did not support the implicit jury finding that Rambus breached a duty to disclose its patents or patent applications as required by JEDEC's rules. Finally, the Federal Circuit upheld the district court's decision to set aside the DDR SDRAM fraud verdict. These holdings rendered the injunction against Rambus moot, and required the Federal Circuit to vacate and remand the award of attorney fees for reconsideration.

(N.D. Cal.); Samsung Electronics Co. v. Rambus, Inc., No. 3:05-CV-00406-REP (E.D. Va.); Micron Technology, Inc. v. Rambus Inc., No. 3:06-CV-00132-REP (E.D. Va.); Rambus Inc. v. Micron Technology, Inc., No. CV-06-00244 RMW (N.D. Cal.); Micron Technology, Inc. v. Rambus Inc., No. CV-00-792-KAJ (D. Del.); Rambus Inc. v. Micron Technology, Inc., *et. al.*, No. 04-431105 (San Francisco Super. Ct.).

[79] *See* Plea Agreement, United States v. Samsung Electronics Co., No. CR 05-0643 (PJH) (N.D. Cal. Nov. 30, 2005), *available at* http://www.usdoj.gov/atr/cases/f213400/213483.pdf; Plea Agreement, United States v. Hynix Semiconductor Inc., No. CR 05-249 (PJH) (N.D. Cal. May 11, 2005), *available at* http://www.usdoj.gov/atr/cases/f209200/209231.pdf; Plea Agreement, United States v. Infineon Techs. AG, No. 04-299 (PJH) (N.D. Cal. Oct. 20, 2004), *available at* http://www.usdoj.gov/atr/cases/f206700/206700.pdf; *cf.* Information, United States v. Elpida Memory, Inc., No. CR 06-0059 (MMC) (N.D. Cal. Jan. 30, 2006), *available at* http://www.usdoj.gov/atr/cases/f214300/214342.pdf.

[80] Rambus, Inc. v. Infineon Techs. AG, 164 F. Supp. 2d 743 (E.D. Va. 2001).

[81] Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081 (Fed. Cir. 2003).

Following remand, Infineon moved to compel production of various documents that Rambus was withholding on the basis of attorney-client and work product privileges. Specifically, the motion was a continuation of an earlier motion to compel under the "crime/fraud exception" to the attorney-client privilege. In ruling on the earlier motion, the district court had concluded that "Rambus implemented a 'document retention policy,' in part, for the purpose of getting rid of documents that might be harmful in litigation."[82]

On May 18, 2004, the district court entered a second order compelling Rambus to produce additional documents.[83] Under this order, the court held that the crime/fraud exception extends to materials or communications created in planning, or in furtheran3mTd(N)TjET

litigation.[94] Ruling in the context of Samsung's motion for an award of attorney's fees, the court found that Rambus planned for litigation throughout 1998 and 1999 and, "as part of the plan . . . implemented a pervasive document destruction program" that targeted "discoverable documents."[95] The court deemed the contrary ruling in *Hynix* "not persuasive."[96]

III. STANDARD OF REVIEW

We review the record *de novo* by considering "such parts of the record as are cited or as may be necessary to resolve the issues presented and . . . exercis[ing] all the powers which [the Commission] could have exercised if it had made the initial decision."[97] *De novo* review is particularly appropriate in this case because we must consider supplemental evidence, as well as new proposed findings of fact and conclusions of law, that were unavailable to the ALJ.[98] In light of our plenary review, we set aside all findings and conclusions of the ALJ, other than those that are expressly cited and relied upon.

A. Standard of Proof: The Preponderance of the Evidence Standard Applies in FTC Adjudications

FTC enforcement actions typically are governed by the preponderance of the evidence standard.[99] The Supreme Court has held that Section 7(c) of the Administrative Procedure Act (APA), which is applicable to administrative adjudicatory proceedings unless otherwise provided by statute, establishes "a standard of proof and . . . the standard adopted is the traditional preponderance-of-the evidence standard."[100] Furthermore, the preponderance of the evidence

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[94] Samsung Elecs. Co. v. Rambus Inc., No. 3:05-CV-00406-REP, 2006 WL 2038417 (E.D.Va. July 18, 2006).

[95] *Id*. at *42.

[96] *Id*. at *38.

[97] 16 C.F.R. § 3.54 (2005).

[98] The record was reopened on separate occasions after the Initial Decision to admit documents relating to Rambus's alleged spoliation of evidence and documents on Rambus's newly found backup tapes. *See supra* Section II.B.

[99] *See, e.g.*, In re Adventist Health System West, 117 F.T.C. 224, 297 (1994) ("Each element of the case must be established by a preponderance of the evidence"); FTC v. Abbott Laboratories, 853 F. Supp. 526, 535 (D.D.C. 1994) (government must show "by a preponderance of the evidence that [respondent's] action was the result of collusion with its competitors").

[100] Steadman v. SEC, 450 U.S. 91, 95-102 (1981) (considering standard of proof in SEC proceedings adjudicating alleged violations of the anti-fraud provisions of the securities laws).

standard generally applies in civil suits to enforce federal statutes such as the antitrust laws.[101] Rambus acknowledges that the preponderance of the evidence standard applies in most agency adjudicatory proceedings, including FTC adjudications.[102] Nevertheless, Rambus advances four arguments why the Commission should apply the clear and convincing evidence standard in this matter.[103]

1. Relationship between Patent and Antitrust Law in Cases Involving Fraud on the Patent Office or Patent Enforcement Initiated in Bad Faith

Rambus argues that "Complaint Counsel should bear the burden of proving the essential elements of their claims by clear and convincing evidence"[104] because of what it terms the "inherent tension between the patent and antitrust laws."[105] Rambus's attempt, however, to broaden the applicability of the clear and convincing evidence standard based on "inherent tension" between the patent and antitrust laws is unavailing. Patents are not inherently in tension with antitrust law. Patents do not necessarily create market power.[106] More fundamentally, competition and patent policy both are aimed at encouraging innovation that benefits consumers, and generally work well together in doing so.[107]

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[101] *See* Herman & MacLean v. Huddleston, 459 U.S. 375, 387-91 (1983).

[102] RB at 134.

[103] RB at 134-40.

[104] RB at 140.

[105] RB at 134.

[106] Ill. Tool Works, Inc. v. Indep. Ink, Inc., 126 S. Ct. 1281 (2006); *see also* U.S. DEP'T OF JUSTICE & FED. TRADE COMM'N, ANTITRUST GUIDELINES FOR THE LICENSING OF INTELLECTUAL PROPERTY, INTITRU 0.0130 Td6u706.960069 B2Tm(R

Nevertheless, Rambus suggests that two cases, in particular, support an extension of the clear and convincing standard to the facts in this proceeding. Neither case creates such a broad rule. The first case Rambus relies on is the Supreme Court's decision in *Walker Process Equipment v. Food Machinery & Chemical Corp.*[108] In *Walker Process*, the Supreme Court held that a patentee may be liable for violation of the antitrust laws if it enforces a patent obtained by knowing and willful fraud on the PTO, and if all other elements of a violation of Section 2 of the Sherman Act are established.[109] The rationale for this holding was to achieve "a suitable accommodation" between policies of the patent and antitrust laws by enjoining enforcement of a patent that conferred monopoly power when the patent was "procured by deliberate fraud."[110] Complaint Counsel in this case do not, however, allege that Rambus procured its patents through fraud on the PTO. Rather, it is alleged that Rambus manipulated the JEDEC standard-setting process by e

the use of the clear and convincing standard to "proceedings in which the alleged violation of the antitrust law consists solely of one or more infringement actions initiated in bad faith."[114] This case, however, involves allegations of deceptive conduct in the context of SSO activities; Rambus is not accused of initiating infringement actions in bad faith.

In short, the cases cited by Rambus do not support its assertion that the clear and convincing standard applies to the elements of this antitrust case because it happens to involve a patent. The Commission is not charged with deciding whether Rambus committed fraud on the PTO, or whether Rambus initiated its infringement actions in bad faith. The issue in the case before the Commission is whether Rambus, through its participation in JEDEC and in the context of JEDEC's standard-setting processes, engaged in a deceptive course of conduct under Section 5 of the FTC Act.[115] No court has held that clear and convincing evidence is required to establish Section 5 deception.[116] To the contrary, as previously stated, the Supreme Court held that Section 7(c) of the APA establishes "a standard of proof and that the standard adopted is the traditional preponderance-of-the evidence standard."[117]

2. Standard of Proof Should Be Commensurate With Proposed Remedy

Rambus's second argument – that a heightened standard of proof is necessary because Complaint Counsel seek to bar enforcement of Rambus's patents under certain circumstances – in effect would allow one potential remedy to determine the standard for establishing whether a violation of the antitrust laws occurred. The potential remedy should not influence the standard

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[114] *Id*. Other cases cited by Rambus arose in similar contexts. *See* Loctite Corp. v. Ultraseal, Ltd., 781 F.2d 861, 876-77 (Fed. Cir. 1985) (requiring a clear and convincing showing that a plaintiff brought a patent infringement suit in bad faith, knowing that there was no infringement), *overruled on other grounds*, Nobelpharma AB v. Implant Innovations, Inc. 141 F.3d 1059, 1068 (Fed. Cir. 1998); *CVD*, 769 F.2d at 849-51 (requiring an antitrust plaintiff to prove bad faith assertion of trade secrets – with knowledge that no trade secrets existed – by clear and convincing evidence).

[115] *See, e.g.*, Complaint ¶¶ 2, 122-24.

[116] *See generally* FTC v. Algoma Lumber Co., 291 U.S. 67, 78-81 (1934) (holding that proof of fraud is not required to prove Section 5 deception).

[117] *See* Steadman v. SEC, 450 U.S. 91, 95-102 (1981).

of proof for liability.[118] To the extent Rambus's arguments might be relevant to our consideration of particular remedies, we will address them in that context.

We note, however, that even a remedy barring enforcement of a patent does not necessarily require a heightened 0.03 Tc 0.0anda 0 Td1.5b

cooperative standard setting depends on some assurance that other participants will not exploit the process by acting deceptively.

IV. MONOPOLIZATION CLAIM[124]

Section 2 of the Sherman Act makes it unlawful to "monopolize, or attempt to monopolize, or combine or conspire with any other person or persons, to monopolize any part of the trade or commerce among the several States, or with foreign nations . . . ."[125] The Supreme Court has identified the basic elements of the offense:

> The offense of monopoly under § 2 of the Sherman Act has two elements: (1) the possession of monopoly power in the relevant market and (2) the willful acquisition or maintenance of that power as distinguished from growth or development as a consequence of a superior product, business acumen, or historic accident.[126]

The fundamental issues in this case are: (1) whether Rambus engaged in exclusionary conduct; (2) whether Rambus acquired monopoly power; and (3) whether there is a causal link between Rambus's conduct and its monopoly power. We consider each of these issues in turn.

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infringe Rambus's patents, work for entities that are entirely controlled by DRAM manufacturers, or are committed to developing technologies that will compete with Rambus's technologies." ID at 265. This standard would call into question the utility and reliability of trial procedures in virtually all antitrust cases. In antitrust litigation, witnesses inevitably are "interested," in the sense that they represent one economic actor or another. In this proceeding, *both* Rambus's and Complaint Counsel's witnesses have an interest in the outcome; depreciating their evidence on that basis indicts all live witness testimony. Economic interest gives us no basis to find that trial procedures – such as requiring a foundation for evidence and subjecting witnesses to cross-examination – are inadequate to compile a reliable record. Therefore, absent a specific reason to question the credibility or reliability of a specific witness or a specific statement, we find no basis to discredit any of the testimony in the record.

[124] Because we find that Rambus unlawfully monopolized the four relevant markets delineated by Complaint Counsel (and whose definition was not contested by Rambus), we need not consider the further allegations that Rambus attempted to monopolize those markets or that Rambus's conduct otherwise constituted an unfair method of competition.

[125] 15 U.S.C. § 2. The Commission's authority under Section 5 of the FTC Act reaches conduct that violates the Sherman Act. *See, e.g.*, FTC v. Cement Inst., 333 U.S. 683, 694-95 (1948); Fashion Originators' Guild of America v. FTC, 312 U.S. 457, 463 (1941); Polygram Holdings, Inc., 5 Trade Reg. Rep. (CCH) ¶ 15,453 at 22,452 n.11 (FTC 2003), *available at* http://www.ftc.gov/os/2003/07/polygramopinion.pdf (slip op. at 13 n.11), *enforcement ordered*, Polygram Holding, Inc. v. FTC, 416 F.3d 29 (D.C. Cir. 2005).

[126] United States v. Grinnell Corp., 384 U.S. 563, 570-71 (1966); *see also* Verizon Communs., Inc. v. Law Offices of Curtis V. Trinko, 540 U.S. 398, 407 (2004) (terming the *Grinnell* formulation "settled law").

A. Exclusionary Conduct

1. Framework for Analysis

technology and thwarting their ability to make informed choices. This sort of deceptive conduct is not competition on the merits. Just as "false or misleading advertising has an anticompetitive effect,"[134] distorting choices through deception obscures the relative merits of alternatives and prevents the efficient selection of preferred technologies.[135]

The courts have established that deception may constitute "exclusionary conduct" that will support a Section 2 claim in appropriate circumstances.[136] In *United States v. Microsoft*, for example, the United States Court of Appeals for the District of Columbia Circuit found that Microsoft's deception with respect to Java applications was exclusionary.[137] As discussion of the legal and factual circumstances and the nature of Rambus's conduct makes clear, proof of the deceptive conduct alleged in this case would establish the exclusionary element required by Section 2.

We stand on familiar ground when we evaluate whether Rambus engaged in a deceptive course of conduct. Section 5 of the FTC Act proscribes, *inter alia*, deceptive acts and practices, and accordingly, the Commission has developed special expertise to determine whether conduct is deceptive.[138] Lest there be any doubt as to the elements of deceptive conduct under Section 5, those elements were spelled out in the Commission's 1983 Policy Statement on Deception (Policy Statement),[139] which the courts have treated as the definitive description of those elements under the FTC Act.[140]

According to the Policy Statement, for conduct to be found deceptive, there must have

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[134] Cal. Dental Ass'n v. FTC, 526 U.S. 756, 771 n.9 (1999).

[135] *Cf.* FTC v. Ind. Fed'n of Dentists, 476 U.S. 447, 461-62 (1986) (describing the anticompetitive consequences of "an effort to withhold (or make more costly) information desired by consumers for the purpose of determining whether a particular purchase is cost justified").

[136] *See* Conwood Co., LP v. U.S. Tobacco Co., 290 F.3d 768 (6th Cir. 2002) (maintaining monopoly power by, *inter alia*, providing misleading market data to retailers in order to distort their purchasing decisions violated Section 2); Caribbean Broad. Sys. Ltd. v. Cable & Wireless PLC, 148 F.3d 1080, 1087 (D.C. Cir. 1998); International Travel Arrangers, Inc. v. Western Airlines, 623 F.2d 1255, 1274 (8th Cir. 1980), *cert. denied*, 450 U.S. 1029 (1981).

via the acquisition of long-run monopoly power.[144] Stated more generally, the so-called sacrifice test condemns conduct that would not make "economic sense" but for the elimination or lessening of competition.[145] Rambus contends that keeping information about its patent applications secret and refusing to share that information with competitors was beneficial to Rambus, regardless of what happened at JEDEC, and therefore could not be exclusionary.[146] The ALJ concurred.[147] We believe this was error both as a ma r

advertising. Therefore, there was a relatively low risk that significant anticompetitive effects would occur in that context.

Unlike those advertising cases, the very different circumstances presented here suggest that deceptive conduct could have caused lasting competitive harm by obscuring crucial information, known only to one industry member, until it was too late to counteract the consequences. In this context, we cannot stress too strongly the importance we place on the fact that the challenged conduct occurred in the context of a standard-setting process in which members expected each other to act cooperatively. We recognize that standard setting of the type sponsored by JEDEC potentially yields significant efficiencies[155] – especially when the standards facilitate interoperability among various components, to the likely benefit of industry participants as well as consumers.[156] Although standard setting displaces the normal process of selection through market-based competition – by which, without any agreement, the purchasing decisions of customers determine which interoperable combinations of products and technologies ultimately will survive – the efficiency benefits of consensus standard setting easily can outweigh that loss of competition.

Even under the best of circumstances, however, the standard-setting process has a unique potential to skew the competitive process by aligning supply and demand in a prescribed direction.[157] The risk of competitive harm is heightened in the face of exclusionary conduct that does not constitute competition on the basis of efficiency and that interferes with the cooperative nature of the standard-setting process. Exclusionary conduct such as deception may distort the selection of technologies and evade protections designed by SSOs to constrain the exercise of monopoly power, with substantial and lasting harm to competition.[158] Additionally, unlike misleading statements made in advertising – which can be corrected quickly by a competitor's counter-advertising – there are fewer "quick fixes" available to correct the competitive harm caused by deception in the SSO context, once a standard has been chosen and the industry has become locked in. If exclusionary conduct reduces or destroys the efficiencies to be gained through consensus standard setting, it may cause considerable harm to competition. If the anticompetitive harm exceeds any remaining efficiencies, standard setting is no longer beneficial on balance.

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[155] *See* Moore v. Boating Indus. Ass'n, 819 F. 2d 693, 695 (7th Cir. 1987); *cf.* United States Dep't of Justice and Federal Trade Comm'n, Antitrust Guidelines for Collaborations Among Competitors (2000)

Consequently, courts have scrutinized conduct related to standard setting.[159] For example, the Supreme Court has condemned efforts to bias the standard-setting process by "stacking" the decision making body with voters interested in excluding a competing product.[160] The Court also has recognized that the power to distort the interpretation of standards is the "power to frustrate competition in the marketplace."[161] Likewise, prior Commission enforcement

those practicing the standard – may be considered a material omission and may constitute deceptive conduct under Section 5. If an SSO chooses not to require such disclosures, SSO members still are not free to lie or to make affirmatively misleading representations. In either case, whether the SSO requires disclosure should be judged not only by the letter of its rules, but also on how the rules are interpreted by its members, as evidenced by their behavior as well as by their statements of what they understand the rules to be.

c. Nature of the Conduct

In order to assess fully the circumstances under which the alleged deception occurred, we also must understand the nature of the allegedly deceptive course of conduct, which combined the acquisition and exploitation of patents with a cooperative standard-setting process. A patent holder's market power may be materially enhanced once the patented technology is incorporated into a standard, as alternatives become less attractive relative to the chosen technology and less able to constrain its price.[164] For this reason, Rambus's alleged course of conduct, if established, could be especially pernicious to the competitive process.

An SSO may elect to require disclosure of patent positions before standardization decisions are made, because this enables SSO participants to make their choices with more complete knowledge of the consequences – including the potential that those practicing the standard may be liable for patent infringement, unless they negotiate licenses and pay royalties. If the SSO members prefer a given technology, notwithstanding the prospect of royalties, they can vote to incorporate it into the standard. If, in light of likely royalty payments, members prefer an alternative technology, they can vote against inclusion of the patented technology.

Disclosure of potential patent liability also helps avoid the possibility of hold-up by enabling SSO participants to seek protection from excessive royalties "*ex ante*" – *i.e.*, before choosing which technologies to incorporate into the standard. For example, an SSO member expecting to sell products that conform to the standard, who gains knowledge of potential patent exposure, may have powerful economic incentives to negotiate a license *rife*

the owner of the patented technology may prefer to offer an *ex ante* license – even at a lower *ex ante* rate – knowing that the other SSO participants otherwise might engage in a cost/benefit analysis and opt to standardize an entirely different technology. Indeed, under certain circumstances, members of an SSO may even collectively negotiate these types of *ex ante* licenses, without necessarily running afoul of the antitrust laws.[166]

In sum, standard setting can function as an efficient substitute for selecting interoperable technologies through direct competition. Rambus's course of conduct allegedly impaired these processes within JEDEC. Complaint Counsel argue that Rambus deprived other JEDEC members of information needed to make an efficient selection of the "best" technologies for SDRAM standards, based on an analysis of likely costs as well as benefits. Rambus's conduct also purportedly prevented other JEDEC members from avoiding exposure to monopoly pricing by securing commitments regarding future royalty rates at a time when alternative technologies still offered unblunted competition. Under the Policy Statement, these circumstances are relevant to our analysis of whether Rambus's course of conduct constituted deception in violation of Section 5 of the FTC Act. Under Section 2 case law, these circumstances suggest exclusionary conduct: deceptive behavior that hides the price of a patented technology is not "competition on the merits,"[167] and deception that thwarts informed choice is not competition on the "basis [of] efficiency."[168]

2. Rambus's Course of Conduct

Applying the analytical framework to the facts of this case, we first consider whether Rambus engaged in a course of conduct in its JEDEC activities that included potentially deceptive conduct – *i.e.*, "misrepresentations, omissions, or practices."[169] There is little room for

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agreement with Complaint Counsel's general theory, not as representative of any concession that anticompetitive conduct occurred in this case.)

[166] *See* Chairman Deborah Platt Majoras, Recognizing the Procompetitive Potential of Royalty Discussions in Standard Setting, Remarks Before Standardization and the Law: Developing the Golden Mean for Global Trade (Stanford, Cal., Sept. 23, 2005), *available at* http://www.ftc.gov/speeches/majoras/050923stanford.pdf.

[167] *See, e.g.*, Aspen Skiing Co. v. Aspen Highlands Skiing Corp., 472 U.S. 585, 605 n.32 (1985); Multistate Legal Studies, Inc., v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 63 F.3d 1540, 1550 (10th Cir. 1995), *cert. denied*, 516 U.S. 1044 (1996); Town of Concord v. Boston Edison Co., 915 F.2d 17, 21 (1st Cir. 1990), *cert. denied*, 499 U.S. 931 (1991).

[168] *See Aspen Skiing*, 472 U.S. at 605 ("If a firm has been 'attempting to exclude rivals on some basis other than efficiency,' it is fair to characterize its behavior as predatory") (footnote omitted), quoting ROBERT H. BORK, THE ANTITRUST PARADOX 138 (1978).

[169] *Policy Statement, supra* note 139, at 20,911-12.

dispute about what Rambus did, because much of the evidence in the record regarding Rambus's conduct came from Rambus's own documents and witnesses.[170]

Based on that evidence, we find that Rambus concealed the patent applications it filed, and the patents it obtained, until JEDEC had adopted its SDRAM and DDR SDRAM standards. Once those standards were adopted, Rambus abused their adoption by suing firms that practiced the standards for patent infringement. Rambus also used information derived from JEDEC meetings to develop a patent portfolio that would cover JEDEC's SDRAM standards – a practice which, although it may not be clearly "deceptive" standing alone, nonetheless facilitates hold-up in a cooperative standard-setting context.

The record reveals the following chronology of events.

a. The Chronology of Concealment

1991. JEDEC was in the early stages of work on the SDRAM standard[171] when Rambus attended its first JEDEC meeting and joined JEDEC in December 1991.[172] Within a few days of that JEDEC meeting, Rambus's Executive Vice President (EVP), Allen Roberts, called Lester Vincent, Rambus's outside patent counsel, to speak with him about "patent deadlines"; Roberts also informed staff that a Rambus goal for the first quarter of 1992 was "patent filing."[173]

1992. Rambus engineer William Garrett represented Rambus at its first JEDEC meeting as a member in February 1992. Following the meeting, Garrett reported to his supervisors that SDRAMs were inevitable and that SDRAM could be standardized sooner than expected.[174] Shortly afterwards, on March 5, 1992, Rambus responded to the PTO's restriction requirement[175]

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[170] Of course, documents destroyed by Rambus might have provided additional details regarding Rambus's activities. *See infra* Section V.

[171] Fully synchronous DRAM initially was proposed to JEDEC in May 1991. IDF 297. Rambus's patented versions of two of the relevant technologies are included in the SDRAM standard: programmable CAS latency and programmable burst length. Rambus's patented versions of the other two relevant technologies – dual-edge clocking and on-chip PLL/DLL – were included in the next generation of SDRAM, called DDR-SDRAM. All of these technologies were considered for inclusion into the SDRAM standard.

[172] CX 602 at 1-3. Rambus already had met with a number of DRAM manufacturers in an effort to convince them to license RDRAM. *See supra* Section II.A.

[173] CX 1705 at 34.

[174] CX 672 at 1 ("SDRAMs will happen.").

[175] *See supra* note 19 and accompanying text.

Vincent to discuss adding claims to the divisional applications.[183] In that same month, Rambus CEO Tate called a meeting with Rambus executives, including Crisp and Roberts, to discuss: (1) how JEDEC SDRAMs might infringe Rambus's patents ("What patents do synchronous

The following month, the JC 42.3 subcommittee voted to send its proposed SDRAM standard, which included programmable CAS latency and burst length, to the JEDEC Council for approval.[202]

filed.[210] Crisp responded that this "sounds really good [and] matches what I have requested and what I believe has happened."[211]

1994. Rambus executives continued to correspond and meet with Vincent in early 1994 to "talk about patent strategies."[212] In March 1994 Rambus President David Mooring called for an "IP maximization strategy" to be put in place by the next quarter.[213]

Throughout 1994, Rambus continued to work on amending its applications, focusing on SDRAMs or future SDRAMs such as DDR. In May of that year, Roberts requested that Vincent consider ways to add or strengthen claims covering programmable CAS latency and dual-edged clocking, which subsequently became features of DDR SDRAM.[214] Rambus CEO Tate monitored the progress of Rambus's patent activity and asked for progress reports, particularly regarding the claims "that read directly on current/planned sdrams."[215]

In September 1994, JEDEC participants made formal presentations relating to on-chip PLL/DLL technology for later-generation SDRAM (which became known as DDR SDRAM).[216] Although Crisp knew that Rambus had been pursuing patent claims covering on-chip PLL, he omitted to disclose any patents or patent applications at this meeting.[217] His report to Rambus management on the meeting stated, "Obviously we need to think about our position on this for potential discussion with NEC regarding patent issues here."[218] Crisp e-mailed Roberts that he thought Rambus eventually would bring infringement actions in areas such as "PLL on a DRAM

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[210] CX 1959. *Compare* Nusbaum, Tr. 1584 *with* Fliesler Tr. 8867 (disagreeing as to whether claims filed on June 28, 1993 actually covered a subsequent PLL proposal).

[211] CX 703.

[212] CX 718 (e-mail dated January 5, 1994, setting up meeting with Vincent for January 12, 1994).

[213] CX 726 (e-mail dated March 15, 1994). Mooring's e-mail also proposed that Rambus "kick-off another patenting spree focused on the controller side of things" to take advantage of "a window of opportunity left while we still have confidential information . . . ." *Id*.

[214] CX 734.

[215] CX 740 (June 1994 e-mail from Tate to Roberts requesting "a list of which claims we are making that read directly on current/planned sdra 0 33 i516.72 Tm(C(dentiaurrewh.48 0 Td(er sij0mo)Tjmiambube.027 0 Td(18 (ti)o i c/MCtrackos

. . . programmable access latencies and host of other areas."[219] In that same month, September 1994, Rambus amended its 08/222,646 application (the '646 application) to add claim 151, relating to dual-edged clocking.[220]

1995. In April 1995, Rambus CEO Tate reiterated objectives of "get[ting] royalties from competitive memory" that used just one or a few of Rambus's technologies; called for verification that "all ideas we have requested to be filed as general patents re [SDRAM] have been [filed]"; and directed that Rambus "hold on patent issuances till then."[221] In May 1995, Crisp recommended that Rambus continue to keep its patent position secret, explaining that "it makes no sense to alert them [JEDEC] to a potential problem they can easily work around."[222] Through the summer, Crisp participated in work "on enhancing claim coverage."[223] In October 1995, Rambus amended one of its patent applications to insert claims relating to on-chip PLL/DLL technology.[224] One week after filing these amendments, Rambus received a JC 42.3 survey ballot on "Future Synchronous DRAM F

"even after seeing this disclosure of a patent application," he "did not say anything with respect to any Rambus patent application concerning PLLs or DLLs."[227]

Crisp advised management in September 1995 that Rambus should "redouble [its] efforts to get the necessary amendments completed, the new claims added and make damn sure this ship is watertight before we get too far out to sea."[228] In fall 1995, Rambus's new in-house counsel, Anthony Diepenbrock, outlined Rambus's patent strategy at a company-wide retreat.[229] Diepenbrock's presentation described Rambus's "offensive" patent strategy as "find[ing] key areas of innovation in our IP that are essential to creating a competing device" and "claim[ing] these areas as broadly as possible within the scope of what we invented."[230] The first two examples cited in Diepenbrock's presentation were DLLs and dual-edge clocking.[231]

Meanwhile, Diepenbrock advised Crisp – just as Vincent had in 1992 – that Rambus faced a risk of equitable estoppel based on its participation in JEDEC.[232] Diepenbrock urged that Rambus withdraw from JEDEC.[233] At his next JEDEC meeting, in December 1995, Crisp made private inquiries regarding JEDEC's patent policy.[234] Based on these discussions, as summarized in an e-mail to Rambus executives, Crisp stated that it was unacceptable "to not speak up when we know that there is a patent issue, to intentionally propose something as a standard and quietly have a patent in our back pocket we are keeping secret that is required to implement the standard and then stick it to them later (as WANG and SEEQ did)."[235]

Later that month, Vincent sent Diepenbrock "materials relating to the proposed [FTC] consent order involving Dell computer," which resolved allegations of unfair methods of competition based on Dell's assertion of patent rights after its representative had certified to an

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[227] Crisp, Tr. 3341-44. Crisp promptly reported MOSAID's disclosure to Rambus management. *See* CX 711 at 192.

[228] CX 837 at 2.

[229] Diepenbrock, Tr. 6129-30.

[230] CX 1267; Diepenbrock, Tr. 6131.

[231] CX 1267; Diepenbrock, Tr. 6132-33.

[232] Crisp, Tr. 3442.

[233] *Id*. at 3442-43.

[234] *Id*. at 3440-44, 3447-48; CX 711 at 188 (Crisp e-mail describing conversations with Sanyo's Howard Sussman and VLSI Technology's Desi Rhoden). Crisp testified that he sought this information because Rambus was considering making a presentation regarding a proposed technology. Crisp, Tr. 3440-41, 3447-48.

[235] CX 711 at 188. Crisp's e-mail adds, "I am unaware of us doing any of this or of any plans to do this." *Id*.

its intellectual property."[247] Rambus omitted from the list that it provided to JEDEC the only then-issued patent that Rambus believed covered technology under consideration by JEDEC – the '327 patent.[248]

Rambus's June 1996 withdrawal letter also omitted information that would have allowed JEDEC members to adopt standards that would avoid infringing Rambus's intellectual property. While the letter mentioned inconsistency between JEDEC and Rambus with respect to the "terms" of licensing, and purported to reserve Rambus's rights respecting its intellectual property, Rambus omitted to disclose that it had used information gleaned during JEDEC meetings to develop a patent portfolio covering JEDEC's SDRAM and DDR SDRAM standards, and also omitted to disclose the patent applications Rambus had filed to implement its strategy. To the contrary, the letter stated, "To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents."[249] Rambus's list identified *only* patents unrelated to JEDEC's work.[250] Rambus's letter stated that Rambus had applied for "a number of additional patents" but the letter did not suggest that future patents would be any more applicable to JEDEC's DRAM standards than were the issued patents on the list.

1997 and subsequent years.[251] Although Rambus terminated its JEDEC membership in 1996, Rambus continued to receive information on the activities of JEDEC after 1996. Beginning in 1997, Crisp received information from a source that he referred to as "deep

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[247] *Id*.

[248] *See* CX 5013 (designated R401208-09) (Joel Karp presentation regarding "Enforcement Scenario for 1999," stating, " '327 – covers DDR (dual-edged clocking)"). (The "R" designation refers to Bates stamp numbers

throat."[252] Crisp also received information from three other unsolicited sources known as "Mixmaster," a reporter called "Carroll Contact," and "secret squirrel."[253] According to Crisp, these sources provided information on the features of devices being proposed for standardization.[254] Crisp shared the information he obtained from these inside sources with Rambus's executives and engineers,[255] and this information was used in the continuing process of filing and amending Rambus's patent applications.[256]

Additionally, although no longer a JEDEC member, Rambus continued to conceal its relevant patent applications. Rambus CEO Tate, for example, stated in a February 1997 e-mail to Rambus executives, "do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait."[257] Likewise, a July 1997 e-mail by Rambus Chairman of the Board Bill Davidow stated that "[o]ne of the things we have avoided discussing with our partners is intellectual property problem [infringement by SyncLink and SDRAM/DDR SDRAM] . . . . We are hoping that they will either drop their competitive efforts or discover for themselves that they have v

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1999.[261] By November 1999, Rambus had obtained all four patents cited in its first complaint against JEDEC-compliant uses (filed against Hitachi) in January 2000.[262]

b. Rambus's "Notice" to JEDEC

Rambus claims that it twice gave notice to JEDEC of its patents and patent applications through responses to questions. Based on our review of the evidence regarding those incidents, we find that, far from giving notice, Rambus's responses were evasive and, indeed, misleading.

The first incident, in May 1992, was an outgrowth of concerns held by IBM and Siemens regarding possible Rambus patents on dual-bank designs. In the course of a discussion of that technology at a JEDEC meeting, some of the participants noted the possibility that Rambus and Motorola might have patents on multi-bank designs (a technology that is not at issue here).[263] Motorola's representative promised to check and to get back to JEDEC with an answer.[264]

answer to the question posed, or something else. He did *not* say that the gesture meant that Rambus would not disclose relevant patents or patent applications, and the record shows that those present did not read that into his gesture.[268]

The second incident relates to a May 1995 JEDEC subcommittee discussion of the SyncLink memory technology. This is not a technology at issue here.[269] A number of companies were asked whether they had relevant patents. Intel's Sam Calvin asked whether Rambus had patents relevant to SyncLink, and then DRAM task group chairman, IBM's Gordon Kelley, addressed to Crisp a request that Rambus provide a statement as to whether Rambus had patents that covered SyncLink.[270]

At the next JEDEC subcommittee meeting on September 11, 1995, Rambus furnished a written response that focused on its patents and patent applications relevant to SyncLink alone.[271] Indeed, except for the concluding sentence, the entire statement referred exclusively to SyncLink. The record shows that the JEDEC meeting attendees interpreted the statement as relating to SyncLink only and therefore of no moment.[272] Moreover, Rambus took additional steps to

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[268] Intel's Calvin testified that the incident gave him no concern. Calvin, Tr. 1070-71. Meyer and Kelley ultimately concluded that Rambus had no relevant patents. CX 2089 at 151-52 (Meyer *Infineon* dent gave Tdoncern

deflect attention from the potential breadth of the statement's final sentence.[273] After Kelley commented that Rambus had not said anything, Crisp re-framed the final sentence in terms of SyncLink: "I reminded them . . . that our silence was not an agreement that we have no IP *related to SycLink* (sic). . . ."[274] In addition, Crisp reminded the members that Rambus previously had reported a patent to JEDEC, suggesting that this placed Rambus in the category of JEDEC members who had disclosed patents.[275]

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The record demonstrates that Rambus's course of conduct included two species of potentially deceptive conduct set forth in the Policy Statement:

- Rambus made potentially deceptive omissions via its continuing concealment of its patents and patent applications until after the DDR SDRAM standard was in place; and

- Rambus made outright misrepresentations when it gave evasive and misleading responses to questions about its conduct.

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by recipient to IBM and Hewlett Packard (HP) JEDEC participants, among others), 104-05 (s,,sTc 6.c). . . ."

process would be cooperative and free from deceptive conduct. In that environment, we find that Rambus's course of conduct was likely to be "material" because it was likely to infect the decisions of JEDEC members with respect to the SDRAM standards to be adopted.

a. EIA/JEDEC Policies and their Dissemination

The record shows that although EIA/JEDEC policies are not a model of clarity, a duty of good faith underlies the standard-setting process under those policies. Specifically, under the EIA/JEDEC rules, "[a]ll EIA standardization programs . . . shall be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation . . . ."[278] Another general EIA regulation provides that EIA standardization programs "shall not be proposed or indirectly result in . . . restricting competition, giving a competitive advantage to any manufacturer, excluding competitors from the market . . . except where required to meet one or more of the" enumerated "legitimate public interest" objectives.[279]

To accomplish that EIA goal, as the majority opinion in *Rambus v. Infineon Technologies A.G.* declared,[280] JEDEC's Manual of Organization and Procedure (the JEDEC manual) expressly obligated the subcommittee chairperson to remind members to inform the meeting of any patents or applications "that might be involved in the work" being undertaken.[281] EIA General Counsel/JEDEC legal counsel John Kelly testified that JEDEC's rules required disclosure of patents and patent applications.[282] For most of the time that Rambus was a member

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[278] CX 204 at 5.

[279] *Id*.

[280] 318 F. 3d 1081, 1098 (Fed. Cir. 2003).

[281] CX 208 at 19 (JEP21-I, JEDEC Manual of Organization and Procedure) (Oct. 1993). Although Rambus and the ALJ question whether this manual was officially adopted, *see* RB at 15-16, IDF 627-28, the record does not support that speculation. *See* CX 205 at 15 (establishing procedure for amending predecessor manual 21-H); CX 54 at 7, G. Kelley, Tr. 2428, and J. Kelly, Tr. 1925 (together establishing that the specified steps occurred). For present purposes, however, the important point is that manual JEP21-I was operative – it shaped JEDEC members' expectations. Numerous JEDEC members understood that the JEP21-I manual set out JEDEC's disclosure policies. *See, e.g.*, Rhoden, Tr. 311-13; Sussman, Tr. 1349; Landgraf, Tr. 1702-04; G. Kelley, Tr. 2408-09. Indeed, when Crisp requested a copy of JEDEC's patent policies in 1995, JEDEC sent him JEP21-I. CX 2104 at 215–16 (deposition transcript at 851-52) (Crisp *Micron* Dep.) (*in camera*).

[282] *See* J. Kelly, Tr. 1903-04 (disclosure "not optional"), 1925-27 (a "requirement to disclose"), 1870 (EIA Publication EP-3 means that participants need to disclose known patents and patent applications), 1894 (Kelly always understood "patent" to include applications), 1897 (coverage of applications was necessary to make the protections effective), 1931-33 (JEP21-I was an effort "to make it abundantl

steer clear of patents which must be used to be in compliance with the standard whenever possible."[287] Rambus was aware of JEDEC's disclosure policy through written manuals and oral presentations.[288] Crisp understood that disclosure of patents was mandatory,[289] and as early as December 1992, he acknowledged that he understood that patent applications had to be disclosed under JEDEC's policies at least "in some circumstances."[290]

c. Other JEDEC Participants' Understanding of JEDEC's Policy Objectives

Other witnesses besides Crisp testified that JEDEC had determined that prompt disclosure of relevant intellectual property was important for its standard-setting process to work.[291] Absent such disclosure, JEDEC members would face the possibility of patent hold-up. A member possessing relevant intellectual property could stay silent while JEDEC adopted a standard. Then, after a standard had been adopted and it had become expensive to switch to what initially were good alternatives, the patentee could assert its patent and "hold up" the industry by charging higher royalties than could have been extracted before the standard was set. Witnesses testified that early disclosure of intellectual property helped to identify potential hold-up situations while there still was time to avoid the problem.[292]

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[287] CX 903 at 2; Crisp, Tr. 2941-42.

[288] Crisp attended a JEDEC meeting at which revisions subsequently incorporated into the JEDEC manual – including specific references to pending patents and to the participants' obligation to disclose – were presented. *See* JX 14 at 1, 3, 25 (minutes of JC 42.3 meeting, December 9-10, 1992, providing text with proposed changes underlined); Rhoden, Tr. 312; G. Kelley, Tr. 2418.

[289] Crisp, Tr. 3477-78 (stating that "[n]on-presenters were obligated to disclose any known patents they had at the time of the committee letter ballot if those patents were required to – were required by the standard" and that presenters were required to disclose patents and applications earlier); *see also* CX 868 (February 1996 Crisp e-mail stating, with reference to a presentation to JEDEC by Micron, "I think we should have a long hard look at our IP and if there is a problem, I believe we should tell JEDEC there is a problem.").

[290] Crisp, Tr. 2978, 2982, 3477-78. *See also* CX 5105 (December 1992 Crisp e-mail stating "I know that JEDEC takes the position that we should disclose," but commenting, "Of course, we believe that we do not want to do this [disclose patent applications] yet.").

[291] *See, e.g.*, Rhoden, Tr. 536 (describing a "fundamental premise inside JEDEC" that standards that are developed are "either free of intellectual property or at least all intellectual property is known at the time of creation of the standard"); Calvin, Tr. 1002 ("you at least needed to understand the [e]ffect of patents upon thinga0533 Trequired ents

participants,[301] consistently testified that JEDEC members were "obligated" or "required" to disclose both patents and applications.[302]

Several of these witnesses also testified to an expectation that members would disclose planned amendments to pending applications. One witness testified that there was an obligation to disclose "everything that is in the patent process . . . if you intend to seek protection of your intellectual property as it relates to the standard . . . ."[303] Similarly, another witness testified that the disclosure obligation focused on the reasonable possibility that a firm's "invention" might apply to what was being discussed within JEDEC, "no matter what stage a patent might be."[304] As stated succinctly by a former HP employee, "the expectation was that members would disclose anything they're working on that they potentially wanted to protect with patents down the road."[305]

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always say disclosure of applications was required), 357 (duty to disclose covered applications), 637 (same).

[299] *See* Calvin, Tr. 1003-04 ("anyone who was aware of patent – patented items, that could affect policy, had an obligation to bring that awareness to the group); 1006-07 (a requirement to disclose patent applications), 1012-13 (same).

[300] Landgraf, Tr. 1693-95 (from the time that he started attending JEDEC meetings in 1994, disclosure of applications was required).

e. The Behavior of JEDEC Participants

enforce its patents against the industry.[311] Considerable litigation ensued, and the incident generated concern and discussion among JEDEC participants about the need to prevent the problem from recurring.[312]

The second instance involved a proposal by a company called SEEQ, which sought adoption of a standard regarding silicon signature.[313] SEEQ had two patents or applications relating to the technology, but disclosed, and provided licensing assurances for, only one.[314] JEDEC learned of the second item when it was recommending standardization of the SEEQ technology, and it sought RAND assurances, which SEEQ apparently refused.[315] Ultimately, JEDEC chose an alternative technology.[316] Although the events traced to 1989, they left "a negative taste in our mouth" that was still "almost current" in 2003.[317]

The third occurrence involved an attempt by Texas Instruments (TI) to enforce an undisclosed patent on Quad CAS technology. After JEDEC learned of the patent in 1993, the JC 42.3 subcommittee placed a ballot covering the technology on hold,[318] and voted to withdraw a preexisting standard.[319] It took the ballot off hold and dropped the withdrawal of the standard only after TI had provided satisfactory assurances of compliance with JEDEC's licensing policies.[320] A witness from Micron testified that TI's actions led to "a great uproar" and that TI's representative was "pummeled in th[e] meeting for his failure to disclose."[321] Crisp reported to his superiors that TI was "chastised" for not reporting the patent and that discussion was

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[311] Williams, Tr. 787; Sussman, Tr.TI

"nasty."[322] In the course of the dispute, IBM's Gordon Kelley, chairman of JC 42.3's DRAM Task Group, addressed TI in the strongest of terms:

> I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards . . . . If we allow JC-42 standards to be used for patent collection purposes, then we do a great disservice to the very industry that feeds us.[323]

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The only information that Rambus made available, however, was that it was claiming patent rights with regard to technologies in *RDRAM* – not with respect to SDRAM, DDR SDRAM, or any JEDEC-based successors. The prevailing view in the industry was that RDRAM, with its narrow-bus architecture and its multiplexing and packetization, was quite different from the SDRAM and DDR SDRAM standards that were being developed by JEDEC.[328] JEDEC representatives who viewed an RDRAM presentation emerged with the view that RDRAM bore little or no resemblance to JEDEC-compliant SDRAM.[329] For example, IBM's Gordon Kelley testified that after Rambus presented its technology to IBM in April 1992, he believed that "the Rambus DRAM [RDRAM] was so different from the synchronous DRAM RDRA mrigh ap

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similarly relies on its September 1993 disclosure to JEDEC of the '703 patent, which had substantially the same written description as the PCT and '898 applications.[333]

We find that these materials did not provide notice that Rambus might seek to enforce patent rights covering the standards under consideration by JEDEC. None of the original 150 claims in the '898 patent application – which were reproduced in the PCT application – covered SDRAM or DDR SDRAM;[334] nor did any claims in the '703 patent.[335] Although notice might come from the written descriptions as well as from the claims, those descriptions, like Rambus's RDRAM marketing efforts, suggested that claims would be confined to the RDRAM architecture – with a narrow bus, multiplexing, and packetization. Several JEDEC members reviewed Rambus's PCT application or '703 patent and concluded that they had no relevance to JEDEC's standards. Thus, when Infineon's Meyer read the PCT application and the '703 patent, he understood them to relate to RDRAM, including, specifically, its multiplexing.[336] And when Micron's Terry Lee reviewed Rambus's patent abstracts and the '703 patent in 1995, he concluded that the patents "seemed to apply kind of specifically to this bus architecture, to this RDRAM product. . . . the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme."[337] Even Rambus's own JEDEC representative, Crisp, initially read the '898 application as limited to multiplexed, packetized architectures, *i.e.*, to RDRAM.[338]

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[333] IDF 181; Jacob, Tr. 5500-01.

[334] Nusbaum, Tr. 1526; Jacob, Tr. 549

Rambus attempts to transform its argument into a matter of law by presenting the following syllogism: (1) the PTO may only approve patents when their written description covers their claims; and (2) the PTO issued the patents that Rambus has sued upon; so that (3) the written description in the '898/PCT applications and the '703 patent necessarily must have given adequate notice to the world of every claim that eventually issued.[339] This miscasts an inquiry designed for application with hindsight as a test for the reasonable bounds of foresight. The ability, after the fact, to determine from a written description that at the time of filing an applicant "*was* in possession" of a particular invention "*now* claimed"[340] is not the same thing as the ability to predict, prior to their publication, the potential scope of future claims.[341] Rambus's own patent expert regarded the unrevealed claims of a published application as "the family jewels."[342] Rambus avoided displaying those jewels to JEDEC members, and we find that, without knowledge of Rambus's eventual claims, JEDEC members were unable to foresee the implications of the pending applications.

Finally, the ALJ and Rambus point to two incidents – one involving IBM and Siemens in 1992, the other involving Rambus licensing negotiations in 1995 – to demonstrate the industry's awareness of Rambus's relevant patents and patent applications. The IBM/Siemens incident involved a conference call on April 29, 1992, recorded as follows in Siemens's notes: "RAMBUS has announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the RAMBUS storage device architecture."[343] The only concern, however, was that Rambus might have a patent on a technology outside any of the alleged relevant product

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Counsel's experts stated the opposite. *See* Nussbaum, Tr. 1642-43; Jacob, Tr. 5460-67; 54576-85, 5490, 5493, 5498-501.

[339] RB at 39-40.

[340] *See* Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 27 h 93

markets in this case.[344] Ultimately, IBM and Siemens both concluded that Rambus posed no patent problems for SDRAM.[345]

The other incident involved Rambus meetings with LG Semiconductor, Samsung, NEC, and Oki in 1995, at which Rambus CEO Tate claimed he announced that Rambus was seeking patents on DDR SDRAM.[346] In his testimony, Tate did not indicate the specific information that he purportedly conveyed. While his testimony names on-chip PLL and dual-edge clocking as the likely technologies at issue, nowhere does he state that he identified those technologies to the outside firms.

Other evidence suggests that any information conveyed by Rambus would have been opaque. Indeed, a 1997 Tate e-mail indicates that LG continued to believe that DDR SDRAM was a "royalty-free alternative[]" to RDRAM.[347] Moreover, Rambus President Mooring admitted that, to the best of his knowledge, Rambus did not inform any DRAM manufacturer that [Rambus intellectual property covered SDRAM and did not tell anyone that on-chip PLL might infringe a Rambus patent until late 1999.[348] Similarly, Rambus's Senior Vice President Gary Harmon testified that any discussion relating to the [scope of Rambus's patents in the course of 1993-96 licensing negotiations, including those with all four firms identified by Tate, would have been "just a passing reference" and that, even in the case of the one firm with which discussions were more extensive, "I don't believe we ever specifically

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[344] *See* RX 297 at 5 (showing that a few days later, in the course of discussing two-bank designs at JEDEC's May 4-8, 1992 meetings, Siemens and Philips indicated that they were "concerned about [the] patent situation" with regard to Rambus and Motorola); *see also* RX 303 (June 1992 presentation by Gordon Kelley to IBM and Siemens engineers listing "cons" for SDRAMs to include "Patent Problems? (*Motorola/Rambus*)") (emphasis added); CX 2089 at 41-44 (Meyer *Infineon* Trial Tr.) (the concern in May 1992 for Meyer was the possibility that Rambus might obtain patents covering two-bank synchronous DRAM design); RX 289 at 1 (Siemens document prepared by Meyer on May 6, 1992, stating concern that "2-BANK SYNC MAY FALL UNDER RAMBUS PATENTS"). Although the ALJ also cites an IBM "Rambus Assessment" as revealing IBM's concern that Rambus might have patents over SDRAM, IDF 791-95, ID at 307, the document says nothing about such patents. RX 279.

[345] G. Kelley, Tr. 2537-38, 2545-46; CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*).

[346] CX 2111 at 313-21 (Tate FTC Dep.) (*in camera*).

[347] CX 957 at 1. Tate did not correct LG's misimpression, despite having an incentive to do so if he already had chosen to inform LG of Rambus's patent position on DDR SDRAM.

[348] CX 2112 at 172-73, 179-80 (deposition transcript at 171-72, 178-79) (Mooring FTC Dep.) (*in camera*). Rambus apparently did tell Intel in late 1997 or early 1998 that Rambus might have patent applications related to DDR, but Rambus provided "no specifics" and gave "nothing concrete" as to what the applications covered. MacWilliams, Tr. 4905.

royalties or fees."[355] A 1998 Siemens presentation compares RDRAM's "Proprietary solution (Royalties, License fees)" unfavorably with SDRAM II's "Open standard."[356]

In addition, it makes little sense that JEDEC members – which had, for example, "chastised" TI during a "nasty" discussion when it attempted to enforce an undisclosed patent[357] and which cared deeply about cost[358] – would, if they had known about Rambus's patents and patent applications, simply have ignored them and, knowingly and without discussion or hesitation, adopted a standard incorporating Rambus's technology. At a minimum, we would expect the members to have confronted Rambus and demanded RAND terms (even if, as Rambus argues, its technology was so superior that JEDEC had no choice but to adopt it).[359]

Rambus's own documents evince the belief that it had kept secret its patent position relative to JEDEC's standards. In August 1997, Rambus CEO Tate remarked, "[W]e already have the 327 patent but few people are aware of what it means," continuing, "[O]ur policy so far has been NOT to publicize our patents and i think we should continue with this."[360] In May 1999, Rambus Intellectual Property Vice President Karp surmised, "They probably think they avoid our IP if they don't go 'packet based.'"[361] In November 1999, Rambus named its IP initiative "Lexington 'The Shot Heard Around the World,'"[362] which Karp thought fitting because, "We fully anticipated at that point that once people became aware that we had IP covering sync DRAM, DDR, that it was going to make some noise."[363] Even in December 1999 Tate was still directing that, if asked whether DDR SDRAM infringes Rambus IP, "it's important

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[355] CX 2294 at 15. Similarly, Hyundai's 1998 cost comparison [illegible]

At the same time that Rambus was avoiding disclosure of its patent activity, Rambus was engaged in a program of amending its applications to develop a patent portfolio that would cover JEDEC's standards. Rambus made full use of information gleaned from its JEDEC participation to accomplish this objective. Rambus's JEDEC representative was charged with overseeing development of patent claims that would provide better coverage of products compliant with JEDEC's SDRAM standards, and Rambus's CEO asked for progress reports on claims that imp9.731a

applications – was that Rambus would have disclosed if it had had anything relevant to reveal. Even Rambus's withdrawal letter misleadingly conveyed the impression that it was listing its issued patents, while failing to disclose the one patent that might have mattered to the other JEDEC members. Under the circumstances, JEDEC members acted reasonably when they relied on Rambus's actions and omissions and adopted the SDRAM and DDR SDRAM standards.

Rambus withheld information that would have been highly material to the standard-setting process within JEDEC. JEDEC expressly sought information about patents to enable its members to make informed decisions about which technologies to adopt, and JEDEC members viewed early knowledge of potential patent consequences as vital for avoiding patent hold-up. Rambus understood that knowledge of its evolving patent position would be material to JEDEC's choices, and avoided disclosure for that very reason.[368] We thus find that Rambus engaged in representations, omissions, and practices that were likely to mislead JEDEC members acting reasonably under the circumstances, to their substantial detriment, and we conclude that Rambus intentionally and willfully engaged in deceptive conduct.

As discussed in detail in Sections IV.B. and IV.C. below, Rambus's course of deceptive conduct contributed significantly to Rambus's acquisition of monopoly power by distorting JEDEC's technology choices and undermining JEDEC members' ability to protect themselves against patent hold-up. This conduct caused harm to competition. In sum, the record establishes a *prima facie* case that Rambus engaged in exclusionary conduct.

5. Rambus's Procompetitive Justification for its Conduct

Our finding that Complaint Counsel established a *prima facie* case of exclusionary conduct shifts the burden to Rambus to establish a nonpretextual, procompetitive justification for its conduct.[369] Rambus must prove "that its conduct is indeed a form of competition on the merits because it involves, for example, greater efficiency or enhanced consumer appeal."[370]

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[368] Rambus now argues that disclosure would not have changed JEDEC's decision because of the superiority of Rambus's technologies. We address that argument *infra* in Secti

Deceptive conduct is extraordinarily difficult to justify.[371] Rambus tries to avoid this challenge by characterizing its conduct as a refusal to deal with its competitors or a failure to "share its trade secrets with others."[372] Rambus then defends its conduct on the grounds that it preserved the secrecy of Rambus's patent applications, which contained confidential information about Rambus's inventions.[373] Rambus's characterization ignores much of its deceptive course of conduct, as well as the context in which that conduct occurred.

As discussed above, Rambus engaged in a deliberate course of deceptive conduct that included selective omissions and outright misrepresentations relating to its intellectual property.[374] Indeed, Rambus used information obtained via its participation in JEDEC to help shape and refine the very patent applications it now claims it was seeking to protect.[375] Rambus's supposed desire to maintain the secrecy of its intellectual property does not justify the totality of its deceptive conduct in the standard-setting context.

We weigh Rambus's justification in the context of its conduct. In the competitive marketplace, companies generally are justified in choosing not to disclose or share their unpublished patent applications and trade secrets.[376] The ALJ (and Rambus), citing Rambus's patent law expert, found three reasons why, in a competitive context, the non-disclosure of this information serves legitimate and procompetitive purposes.[377] However valid these justifications might be in the abstract – or when applied within a competitive marketplace – they do not fit the record facts or the context that existed here. Further, if protecting trade secrets was critical to Rambus, it had the option to refrain from participating in JEDEC.

First, Rambus argued that withholding of information was justified because disclosure of that information "shows which inventions the applicant is seeking to protect, and thus reveals both technical information and the applicant's business strategies." Preserving trade secrets by preventing access by rivals in a competitive marketplace often may be procompetitive, particularly when that information is not otherwise protected from free-riding by those rivals. However, the technical information comprising Rambus's inventions (as opposed to its

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[371] *Id*. at 77 ("[u]nsurprisingly, Microsoft offers no procompetitive explanation for its campaign to deceive developers.")

[372] RB at 113.

[373] *See* RB at 86-88, 114-15.

[374] *See supra* Section IV.A.

[375] *Id*.

[376] The PTO held patent applications in confidence during the period that Rambus belonged to JEDEC. In 1999, the law changed to require publication of most patent applications 18 months after filing. 35 U.S.C. § 122.

[377] ID at 288-89; RB at 87.

intentions to claim that those inventions covered technologies in JEDEC's DRAM standards – which, as discussed above,[378] could not be divined until the ultimate claims became public) already had been disclosed with publication of the written descriptions of the inventions in the PCT application and the '703 patent. Morever, Rambus has claimed in its numerous infringement actions that the patent laws provide full protection against unlicensed use of its technical inventions, at least for periods after Rambus's patents issued.

It is true that if Rambus had disclosed its relevant patent applications to JEDEC members, the disclosure might have exposed Rambus's business strategy to obtain patents covering JEDEC's DRAM standards – but Rambus does not explain how keeping that strategy secret would be procompetitive given the cooperative atmosphere of the SSO. To the contrary, disclosure would have enabled other participants in the standard-setting process to make their decisions based on knowledge that Rambus's business strategy was to enforce its patents and demand royalties if they were incorporated in standards adopted by JEDEC. As one treatise summarizes, withholding information as to the existence of patent applications in such a setting "would be most valuable as a tool for deception."[379]

Second, Rambus argued that disclosure "could jeopardize the applicant's ability to obtain foreign patents" by "enabl[ing] a competitor to win the 'race'" to foreign patent offices, most of which have "a 'first to file' rule."[380] But under typical first-to-file rules, patents go to the first *inventor* to file.[381] If a competitor merely read or heard Rambus's disclosure, copied its application, and filed first in a foreign jurisdiction, the competitor would not have invented the technology and would not be entitled to a patent.[382] Rambus failed to identify any foreign jurisdiction in which its ability to obtain patent protection would have been threatened by disclosures within JEDEC. Under these circumstances, and on this record, the only effect of Rambus's behavior was to prevent JEDEC participants – who expected Rambus to conduct itself

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[378] *See supra* notes 328-338 and accompanying text.

[379]

cooperatively and without deception – from making their standard-setting decisions with knowledge of the consequences. That is not procompetitive.

Third, we are not persuaded that Rambus's non-disclosure of its patent applications was justified because disclosure "may enable a competitor to slow down or interfere with the patent application process," such as by "enabl[ing] a competitor to provoke an 'interference' at the Patent Office by claiming the same invention in one of the competitor's applications."[383] This, too, is a hypothetical justification. There is no evidence in this record that Rambus's patent position in the United States or elsewhere would have been jeopardized in that fashion.

Finally, Rambus cites Crisp's trial testimony and an e-mail he sent to Rambus executives to support its claim regarding the protection of trade secrets.[384] Crisp testified that Rambus's outside patent counsel advised him that patent applications should be confidential; however, Crisp did not state that counsel's advice was tied to Rambus's course of conduct in the JEDEC standard-setting context.[385] Moreover, although Crisp's e-mail mentioned the desirability "of not disclosing our trade secrets any earlier than we are forced to," the context suggested that this comment reflected Rambus's desire for leverage over its customers.[386] There is abundant additional evidence in the record that Rambus's conduct was motivated by a desire to anticompetitively bias the standard-setting process.[387] In short, there is nothing to support Rambus's claim except the claim itself.

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We find that Rambus did not carry its burden of establishing that its conduct served procompetitive purposes. The record establishes that the purpose and effect of Rambus's deceptive conduct was to manipulate the standard-setting process at JEDEC and gain market power. Furthermore, even if we were to credit Rambus's proffered justification, we find that it would not outweigh the anticompetitive effects of Rambus's exclusionary conduct, particularly in light of the potential to distort industrywide standard setting.

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[383] RB at 87.

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B. Possession of Monopoly Power

Rambus held over 90 percent of the market share in the relevant markets.[395] JEDEC's standards have been ubiquitous in the computer industry: from 1998 on, the decided majority of DRAMs sold have complied with the JEDEC SDRAM and DDR SDRAM standards.[396] Rambus claims that its patents are necessary to make, use, or sell DRAMs that comply with the JEDEC standards.[397] Courts typically find such a high market share sufficient to infer the existence of

PUBLIC RECORD VERSION

The ALJ rejected this evidence regarding JEDEC's cost sensitivity and technology debates because, in his opinion, it was based on "the subjective perceptions of JEDEC members at the time," reasoning that while it "may speak to whether JEDEC would have selected a [substitute] technology, it does not go to whether an alternative is equal or superior in objective terms."[414]

The ALJ's analysis misses the point of the causation inquiry. Evidence that a properly-informed JEDEC may have selected a substitute technology suggests a causal link between Rambus's deceptive course of conduct and JEDEC's decision-making process. This evidence – combined with the evidence of Rambus's strategy, JEDEC members' overriding concern with costs, and the magnitude of the potential royalties in the absence of RAND assurances or the opportunity to negotiate *ex ante* – is enough to show that JEDEC's adoption of the SDRAM and DDR SDRAM standards was linked to Rambus's exclusionio

SDRAM standards;[415] and (3) that Rambus acquired 90 percent market shares in all four of the relevant markets.[416]

These market results were a natural consequence of DRAM industry attributes. In part, the results reflected the nature and composition of JEDEC, a broad-based organization that included essentially all the DRAM manufacturers and their largest customers.[417]

DRAM market whereby multiple DRAM suppliers could supply interchangeable DRAMs; standardization made this possible.[421]

These considerations strongly suggest that the market was likely to coalesce around a standardized choice.[422] Joined with the historical record of the predominant market position of DRAMs compliant with the JEDEC standards, these industry attributes support our finding that JEDEC's choice of standards significantly contributed to Rambus's monopoly power.

3. Rambus's Claims That The Chain of Causation Was Broken

Rambus claims that its course of conduct and its acquisition of monopoly power cannot be linked for four principal reasons.

a. Rambus's Intel Claim

First, Rambus argues (and the ALJ agreed) that Intel's technology choices,[423] not any conduct in which Rambus engaged, caused the monopoly position Rambus enjoyed with respect to SDRAM technologies.[424] If we were to accept this conclusion, implicitly we would be assigning to Complaint Counsel the burden of proving that Rambus's conduct was the *sole* cause of Rambus's monopoly position. This is error as a matter of law.

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[421] *See, e.g.*, Rhoden, Tr. 298-99; Williams, Tr. 763; Becker, Tr. 1152-53 ("[customers like Dell, IBM, and Compaq] want to be able to buy my parts or Samsung's parts or Micron's parts and use them interchangeably, and through the standards process, they get that benefit"); Sussman, Tr. 1328; Landgraf, Tr. 1692-93; G. Kelley, Tr. 2387-88; Heye, Tr. 3641 ("Apple thought it was very, very important to have multiple suppliers"); Polzin, Tr. 3973; Peisl, Tr. 4408-10; Goodman, Tr. 6013; McAfee, Tr. 7225-26; Farmwald, Tr. 8296; CX 1354 at 5 (1999 Tate presentation stating, "Customers want multiple sourced, compatible DRAMs").

[422] *See* McAfee, Tr. 11228-29. Indeed, outside the litigation context, Rambus recognized this very point. *See* CX 533 at 9 (1989 RamBus Business Plan noting "[t]he DRAM industry's penchant for standardization)"; CX 1284 at 28 (1989 RamBus Technology Overview stating, "There is real value in having a world DRAM standard").

[423] In late 1996, Intel announced that its future chipsets – the "gatekeeper" or "traffic cop" components that link CPUs with main memory – would support RDRAM exclusively. *See* IDF 1058; Crisp, Tr. 3432-33; Tabrizi, Tr. 9134-35; RX 1532 at 2. By March 1999, however, Intel determined that "a strategy that puts our chipset and value processor line dependent, solely on Rambus is no longer viable." CX 2527 at 2. In June 1999, Intel announced it might discontinue its exclusive support of RDRAM, and two months later, Intel confirmed that it would also support main memory compliant with

PUBLIC RECORD VERSION

Rambus argues that, even in light of full disclosure, JEDEC still would have standardized Rambus's technologies, because they were superior to all alternatives on a cost/performance basis. We find that the evidence does not establish that Rambus's technologies were superior to all alternatives on a cost/performance basis.[432] Although Complaint Counsel argue that at least six alternative technologies were a

consideration.[437] However, Rambus's cost estimates are unreliable for at least two reasons. First, Rambus assumes, without demonstrating, that alternatives to programmable CAS latency would have provided support for three latency values.[438] Considerable evidence indicates that JEDEC would have required only one or two latency values if it had standardized one of the alternatives.[439] Second, Rambus fails to take account of ways in which the alternative technologies may have reduced costs.[440]

Fixed CAS Latency: A fixed CAS latency part sets a single latency value.[441] Rambus did not present any evidence that this technology had any performance issues. Nevertheless, Rambus argues that fixed CAS latency was not a viable alternative, estimating that it would have increased per-unit costs by three cents for reduced yields and two cents for inventory (while simultaneously reducing per-unit costs by one cent for improved testing).[442] Rambus potentially overstates the inventory costs because it assumes that three latencies would have been supported – a premise that, as discussed above, is not established by the evidence.[443] Rambus also fails to

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[437] *See* Rapp, Tr. 9813-18, 9831-33.

[438] *See* Geilhufe, Tr. 9578. Rambus's other engineering expert presented general testimony that different latencies provided optimal performance with different bus speeds and that users benefitted from the flexibility afforded by programmable CAS latency. Soderman, Tr. 9347, 9350-51.

[439] *See* McAfee, Tr. 11245-48. The record establishes that SDRAMs primarily used only two CAS latency values in main memory. *See* Rhoden, Tr. 394; Lee, Tr. 11004-05, 11063-67, 11097 (testifying that while Micron did produce a part that used a third CAS latency value, this was a small-volume part targeted to the graphics industry). JEDEC standards frequently have required only two latency values.

Dedicated Pins: Dedicated pins can determine latency during DRAM operation.[453] A single dedicated pin can store two CAS latency values, setting one CAS latency under a high voltage and the other latency under a low voltage.[454]

Rambus argues that programmable CAS latency enjoyed cost and performance advantages over dedicated pins. The record does not establish this argument. First, Rambus again fails to show that any alternative to programmable CAS latency would have had to support three latency values.[455] As discussed above, numerous witnesses disagreed with Rambus on this point. Rambus also fails to rebut testimony that, under most circumstances, the implementation of dedicated pins might have been considerably more cost-effective than Geilhufe's predictions.[456]

In terms of performance, Rambus's engineering expert testified that implementing dedicated pins would have required additional wiring and "quite possibl[y]" could have created a "noise glitch."[457] However, IBM's engineer, Mark Kellogg, testified that such wiring would not have been necessary;[458] and the chief platform architect of Advanced Micro Devices (AMD), Steve Polzin, testified that pin-based solutions "probably could have been made to work just fine."[459] Rambus does not demonstrate that its contrary assertions deserve greater weight.

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[453] Jacob, Tr. 5386-87; Soderman, Tr. 9463.

[454] *See* Jacob, Tr. 5386-87; Polzin, Tr. 3991-92. Rambus's engineering expert agreed that two latencies can be supported with a single pin. Soderman, Tr. 9463.

[455] Geilhufe testified that the use of dedicated pins would have increased per-unit costs by four cents, reflecting the fact that four dedicated pins would have been required to replace the range of latency values available with programmable CAS latency. Geilhufe, Tr. 9590. An alternative that supported two latency values would have required the addition of at most two pins (given that pins must be added in pairs). *See generally* Polzin, Tr. 3991-92 (use of pins to set latency would

Data Acceleration Technology. As discussed above,[474] data acceleration technology determines the speed at which data are tra

Based on the totality of the evidence, we find that Rambus has established the superiority of dual-edge clocking over this particular technology.[482]

Double Clock Frequency: Double clock frequency involves operating a single-edge clock at twice the frequency of a dual-edge clock.[483] Rambus has failed to demonstrate that this technology was an unacceptable alternative to dual-edge clocking.

Rambus argues that double clock frequency raises clock distribution problems,[484] requires that the internal circuitry operate at twice the speed of a dual-edge clock,[485] and presents electromagnetic interference concerns.[486] However, these performance concerns were rebutted by Micron's Lee, IBM's Kellogg, and Complaint Counsel's expert witness, Jacob.[487] Other testimony portrayed double clock frequency as a technologically satisfactory alternative to dual-edge clocking.[488] TI clearly found double clock frequency desirable: in 1997 it proposed that JEDEC adopt double clock frequency for its standards.[489]

Rambus's expert testified that double clock frequency would increase per-unit costs by 28 cents,[490] including 24 cents for a clock on the dual in-line memory module (DIMM), which he believed would be necessary.[491] However, the record does not support Rambus's assertion that

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[482] Because we conclude that Rambus has not established the superiority of dual-edge clocking over double clock frequency and toggle mode, however, a showing of superiority over interleaving ranks matters little. Absent a sufficient showing regarding the remaining alternatives, Rambus has not demonstrated that its monopoly power resulted from the superiority of its technology, rather than from its failure to disclose its patent position.

[483] Jacob, Tr. 5433-34.

[484] Soderman, Tr. 9393-94.

[485] Soderman, Tr. 9394-95.

[486] Soderman, Tr. 9395; 9500-01 (asserting that this interference might breach Federal Communications Commission guidelines).

[487] *See* Jacob, Tr. 5433-34, 11115, 11128-29 (slightly reducing voltage mitigates the interference problem); Lee, Tr. 11039-40; Kellogg, Tr. 5182-83 (engineers reduce electromagnetic interference over time).

[488] *See* Kellogg, Tr. 5182, 5184-85; Macri, Tr. 4779-80 (*in camera*) (identifying a "huge" benefit from single-edge clocking).

[489] *See* Lee, Tr. 6711-14; CX 371 at 3.

[490] Geilhufe, Tr. 9610.

[491] Geilhufe, Tr. 9609-10 (speaking in terms of "on-DIMM clock circuitry, possibly on-DIMM PLL/DLL"), 9715 (speaking in terms of an "[o]n-DIMM PLL or DLL circuit, maybe more than a PLL/DLL").

an on-DIMM clock would be needed.[492] Moreover, considerable evidence suggests that Rambus's estimates for the cost of an on-DIMM clock are unreliable.[493] Finally, Rambus fails to consider design, construction, and testing cost savings that would have resulted from substituting a single-edge clock for Rambus's dual-edge clock.[494]

Toggle Mode: Toggle mode was designed by IBM and uses synchronous technology for outputs but asynchronous technology for inputs.[495] JEDEC considered toggle mode in 1990 and 1991.[496] Rambus's contention that IBM's asynchronous design could not achieve the same performance as synchronous technology[497] was contradicted by other evidence.[498] Rambus's

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[492] Geilhufe neither spoke to anyone to confirm the assumption, nor conducted his own timing analysis. Geilhufe, Tr. 9715, 9729. In contrast, a July 28, 1997 TI proposal for using a high-frequency clock made no mention of an on-DIMM PLL/DLL. *See* CX 371. According to Micron's Lee, this proposal would have required "some changes to the bus topology," but not the addition of clock circuitry or a DLL to the module, and "would not have any additional cost over what we were doing." Lee, Tr. 6713-14, 11040. Indeed, Rambus's other engineering expert, Soderman, did *not* claim that on-DIMM clock circuitry would be needed. *See* Soderman, Tr. 9393-95.

[493] Geilhufe testified that an on-DIMM clock costs $3.80 per module (which, allocated over 16 DRAMs, increases cost 24 cents per unit). Geilhufe, Tr. 9606, 9609-10. Geilhufe acknowledged that 16 DRAMs was "the smallest number of units" over which the cost of on-DIMM clock circuit could be allocated. Geilhufe, Tr. 9605-06. For computers with more than 16 DRAMS, this calculation would overstate the clock-circuitry cost per DRAM.

On cross-examination, Geilhufe was shown a document stating that a Kentron PLL circuit cost $2, rather than the $3.80 that he had assumed. Geilhufe acknowledged that he had unsuccessfully sought cost information about the Kentron PLL. *See* CX 2613 at 7; Geilhufe, Tr. 9718-19. Kentron's CEO, Robert Goodman, stated that a standard PLL costs around $1, Goodman, Tr. 6049. Lee testified that Micron pays only 90 cents for PLLs used on register memory modules. Lee, Tr. 11179 (*in camera*); *see also id.* at 11180-81 (*in camera*) (mounting would add further cost but would be "much less" than the cost of the PLL itself). Geilhufe testified that he "did not review specifically the costs for register [memory modules]," but he did not explain why he had not done so. Geilhufe, Tr. 9719. Rambus seeks to dismiss the PLL cost data by suggesting that the Micron PLLs might not operate at the appropriate frequency, but fails to demonstrate that this was so.

[494] *See* Jacob, Tr. 5420-25, 5433-34.

[495] *See* G. Kelley, Tr. 2514; Jacob, Tr. 5608; CX 34 at 32. With asynchronous technology, the internal clock on each DRAM is not coordinated with the computer system clock. *See* IDF 284; Rhoden, Tr. 368. In contrast, operations in DRAMs that use synchronous technology are coordinated with the system clock, which facilitates rapid communication between the CPU and memory. *See supra* note 14.

[496] *See* CX 251 at 1; CX 314 at 1; CX 315 at 1-3; CX 318 at 1.

[497] *See* Soderman, Tr. 9398-99.

[498] *See* Jacob, Tr. 5417. Rambus introduced evidence that an IBM researcher had described toggle mode as "very big, very hot, and very nonstandard," which are "disastrous" attributes "in the commodity market." *See* RX 2099-7 at 16; Soderman, Tr. 9399-9400. Rambus omits that the researcher also found toggle mode "very fast" and, for some purposes, desirable. *See* RX 2099-7 at 16. All of the researcher's conclusions were confined to the "cumulative effect" of combining toggle mode with a specific "low multibit piecepart architecture" and did not

engineering expert also testified that the toggle mode alternative would increase per-unit costs by ten cents due to reduced yields and by two cents for design costs and an additional pin.[499] As mentioned above, Rambus's same expert testified that engineers "solve yield problems very quickly,"[500] which casts doubt on this predicted yield cost increase.

Clock Synchronization Technology. As discussed above,[501] clock synchronization technology coordinates the timing of a computer system clock with the internal clock in each DRAM. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted technology that uses on-chip PLL/DLL circuits to align more closely the timing of the two clocks. Rambus now claims that its patents cover on-chip PLL/DLL as implemented in JEDEC-compliant products.

Rapp analyzed four alternatives to on-chip PLL/DLL technology: placing DLL circuits on the memory controller; placing DLL circuits on the memory module; using vernier circuits instead of on-chip PLL/DLL circuits; and relying on the DQS strobe rather than the system clock

contemporaneous beliefs that this alternative was workable and desirable. For example, in March 1996, Samsung presented a proposal to JEDEC that involved removing the PLL circuit from the DRAM chip and placing it on the memory controller.[506] In light of the evidence as a whole, Rambus has not carried its burden with respect to this alternative.

DLL on the Module: Another alternative to on-chip PLL/DLLs involves placing one or more DLL circuits on the memory

circuits do not perform well enough to be viable alternatives to on-chip PLL/DLL.[515] However, several witnesses testified as to the advantages of vernier circuits.[516]

Rambus notes that the SyncLink consortium considered designing the SLDRAM chip using verniers, without PLLs or DLLs on the DRAM, but ultimately included both verniers *and* DLLs on the DRAM.[517] Rambus argues that this example demonstrates that verniers were not viable alternatives to on-chip DLL/PLL, but the record offers competing explanations for why Synclink included DLLs in SLDRAM.[518]

Rambus further asserts that Micron and SLDRAM hold patents that cover the use of verniers,[519] but provides no element-by-element analysis – indeed, no evidence beyond the bare

high speed performance.[523] The record contains conflicting evidence, however, suggesting that most JEDEC members believed this technology offered adequate performance.[524] Indeed, DQS strobes are part of the DDR SDRAM standard and were included in proposed specifications for DDR2 SDRAM.[525]

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We conclude that Rambus has failed to meet its burden of demonstrating that JEDEC would have standardized Rambus's technologies even if Rambus had disclosed its patent position. With regard to performance attributes, the testimony of Rambus's experts was offset by conflicting testimony from Complaint Counsel's experts, which called into question the significance of Rambus's performance concerns. In many instances, testimony from JEDEC members and evidence of their prior actions in sponsoring the alternative technologies substantially buttressed Complaint Counsel's case.

With regard to costs, Rambus failed to demonstrate that alternatives would have been more expensive. Rambus's economics expert, Rapp, compared the added variable costs associated with the alternatives, based on Geilhufe's cost estimates, to the costs of paying royalties for Rambus's patented technologies. Rapp testified that the least costly alternatives would add .82 percent to the selling price of SDRAM and 5.65 percent to the selling price of DDR SDRAM.[526] He concluded that these costs exceeded Rambus royalties of .75 percent of selling price for SDRAM and 3.5 percent for DDR SDRAM.

Rapp's calculations are fraught with uncertainty and potential for error. They are based on Geilhufe's admittedly imprecise cost estimates. Geilhufe acknowledged that his cost

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[523] *See, e.g.*, Soderman, Tr. 9415-17; RX 1040 (e-mail prepared by HP JEDEC representative Hans Wiggers explaining his preference for using DLLs at high speeds, in response to a message entitled, "Death to DLLs"); RX 1086 at 1 (*in camera*).

[524] *See* Lee, Tr. 6682-83; Kellogg, Tr. 5158-59; CX 368 (Micron proposal that JEDEC standardize DQS strobes in DDR SDRAM without DLLs); CX 370 (Silicon Graphics proposal that JEDEC standardize data strobes without DLLs); RX 911 at 3 (SyncLink's design included a data strobe); CX 711 at 72 (noting Hyundai's belief that strobes eliminate need for PLLs/DLLs); *cf.* Jacob, Tr. 5456-57 (presenting DQS strobe alternative).

[525] JX 57 at 5; RX 2099-14 at 3; RX 2099-39 at 5. On-chip DLLs can be disabled in DDR SDRAM but are needed for normal DDR operation. *See* Lee, Tr. 6680-81, 6683; CX 234 at 176; JX 57 at 5, 16.

[526] Rapp, Tr. 9831-32, 9850-54. To compare the dollar figures calculated for cost increases with the percentage figures used in stating Rambus's royalties, Rapp projected an average selling price over the expected lifetimes of the products, calculating an average selling price of $4.87 for SDRAM and $5.13 for DDR SDRAM. *Id.* at 9816-17, 9845. Rapp then translated the increased variable costs of the alternatives into a percentage of average selling price. *Id.* at 9816-17, 9845.

estimates were approximations and he assigned them a sizeable 25 percent margin of error.[527] Yet a 25 percent reduction of Rapp's estimate of the least-costly alternative to SDRAM would bring that estimate well below the level of SDRAM royalties.[528] Moreover, Geilhufe drew many of his estimates from personal experience, without verification by actual cost data or substantiation by supporting record evidence.[529] As to DDR SDRAM, Rapp had to premise his comparisons on projections of future DRAM selling prices and sales volumes.[530]

Rapp's cost estimates drop considerably when revised to reflect different assumptions. For example, recalculating Rapp's estimate of a least-cost alternative to Rambus technologies in SDRAM based on support of two, rather than three, latencies[531] yields total increased cost of .62 percent of selling price, which is less than the .75 percent SDRAM royalty paid to Rambus.[532] Similarly, applying Rapp's methodology to alternatives to Rambus technologies in DDR SDRAM yields costs well below Rambus royalty levels.[533] Moreover, Rapp's calculations, like Geilhufe's estimates, wholly ignore several possibilities for cost reductions from adoption of the alternative technologies.[534]

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[527] *See* Geilhufe, Tr. 9665.

[528] A 25% margin of error for SDRAM equates approximately to .21% of selling price.

[529] *See* Geilhufe, Tr. 9665-67. Geilhufe acknowledged that he did not seek actual cost data from DRAM manufacturers to verify his cost estimates. *Id*. at 9666-67.

[530] Rapp had to estimate future DRAM prices over the expected life of DDR SDRAM, then weight those prices by estimating sales volumes for each of the future years. *Id*. at 9816-17. Rapp acknowledged that for DDR SDRAM, with limited historical data, the numbers were "mostly estimate." *Id*. at 9845.

[531] *See supra* note 439 and accompanying text.

[532] *See supra* notes 443 and 473 (showing a total cost increase of only $.03 per unit for a combination of fixed CAS latency and burst terminate commands).

[533] If, as the record suggests, no clock-circuitry was needed for double clock frequency, *see supra* note 492, total increased cost for a combination of fixed CAS latency, burst terminate commands, double clock frequency, and a clock synchronization technology would have been seven cents, or 1.36% of DDR SDRAM selling price, which is far below Rambus's 3.5% royalty. (Like Rapp, we assign no added cost for alternative clock synchronization technology.) If clock-circuitry was necessary, the record shows that PLLs sold for between 90 cents and $2. *See supra* note 493. Even based on the *highest* price, the increased cost for the combination of alternatives to Rambus's four patented technologies would have exceeded Rambus's royalty by less than Geilhufe's admitted margin of error.

[534] *See supra* notes 440, 445, 452, 456, 467, and 494 and accompanying text.

In sum, Rambus has not shown that all alternatives would have been more costly than its royalties and has not carried the burden of establishing its inevitability/superiority defense.[535]

c. Rambus's Claim that the Link between its Conduct and the Standards Did Not Matter

Rambus backstops its inevitability/superiority claim by asserting that even if its conduct distorted the decisionmaking process at JEDEC, that did not have the effect of harming competition because the interests of JEDEC and it members were not necessarily aligned with the interests of the public as a whole.[536] We reject that argument. As discussed above, JEDEC comprises a broad range of industry participants – including, most importantly, the principal purchasers of both DRAM technologies and DRAMs. The technology choices made by the JEDEC members during the standard-setting process reflect the opinions of virtually the entire spectrum of economic actors who are directly impacted by JEDEC's standard-setting decisions. Courts and commentators long have recognized that a fair, honest, and consensus-based standard-setting process can be beneficial to consumers, while substantial competitive concerns may arise when the standard-setting choices of the SSO's participants are distorted.[537] Rambus offers no logical explanation, and cites no supporting precedent, for why the interests of JEDEC and its members would be inconsistent with a procompetitive result, or why we should overlook conduct that distorted the decisions of JEDEC.

Rambus also argues that because standard setting is a "winner-take-all" process, a "but for world" in which Rambus had disclosed its patent position would have been no better than the real world in which JEDEC adopted standards incorporating Rambus's patented technologies.[538] We reject this claim, too. Payment of royalties on memory interfaces has been very much the

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[535] Rambus also argues that the decision of three JEDEC members, with knowledge of Rambus's patents, to develop and manufacture a DRAM chip known as RLDRAM, using programmable CAS latency and burst length and dual-edge clocking, was evidence of the superiority of Rambus's technologies. RB at 59-60. RLDRAM, however, was a high-price, niche product used for specialty applications such as high-speed routers. *See* Bechtelsheim, Tr. 5867, 5870-71 (RLDRAM is priced "several times higher than commodity DRAM"); McAfee, Tr. 7428-31 (showing that RLDRAM sales were very small); Prince, Tr. 9021-22 (omitting mention of RLDRAM when asked to name "any DRAM" that had not been standardized by JEDEC or IEEE). Given RLDRAM's niche nature, a willingness to absorb Rambus royalties for RLDRAM tells little about JEDEC members's preferences for high-volume, low-cost, main memory purposes.

[536] RB at 126-28.

[537] *See, e.g.*, Allied Tube & Conduit Corp. v. Indian Head, Inc., 486 U.S. 492, 500-01, 510 (1988); II HOVENKAMP ET AL., IP AND ANTITRUST, §§ 35.4(a)(4), 35.5.

[538] RB at 126.

exception, rather than the rule, in the computer industry.[539] JEDEC could have turned to unpatented alternative technologies in each of the relevant product markets.[540] But even assuming, *arguendo*, that JEDEC still would have been willing to adopt Rambus's patented technologies after disclosures had been made, JEDEC and EIA policies would have prohibited the standardization of those technologies unless Rambus committed to licensing on RAND terms.[541] If Rambus had refused to provide the requisite RAND assurances, JEDEC would have been bound by its rules to avoid Rambus's patented technologies.[542]

Alternatively, Rambus might have acceded to JEDEC's licensing policies, and JEDEC members then would have had the benefit of RAND terms. Moreover, JEDEC members at least would have had the opportunity to seek specific royalty commitments from Rambus through *ex ante* negotiations; it was not up to Rambus to preclude that possibility.[543] No matter what the

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[539] *See, e.g.*, Heye, Tr. 3918 (AMD has not paid royalties on memory interfaces to anyone other than Rambus).

[540] *See supra* Section IV.C.3.b. For example, the record contains no suggestion that using fixed CAS latency or fixed burst length, setting CAS latency with fuses or pins, or setting burst length with fuses or burst terminate commands, would have raised patent issues. Nor does the record suggest that using double clock frequency or toggle mode, or relying on data strobes, or putting DLLs on the module or memory controller, would have involved proprietary technology.

[541] *See supra* note 285 and accompanying text (citing JEDEC and EIA rules that prohibited the standardization of patented technologies without first securing "all relevant technical information" and assurances that the patent holder will license on RAND terms).

[542] Rambus highlights the decision of a different EIA unit, the Consumer Electronics Association (CEA), to refrain from requiring a RAND assurance from Echelon Corporation. CEA chose not to invoke its licensing rule – potentially permitting Echelon to block a standard by non-compliance – but only after Echelon had announced its intention to block the standard; had engaged in a pattern of efforts over time to halt the standard development effort; and had "been unable to explain or document how the [CEA] standard refer[red] to or require[d] use of any of Echelon's patented technology." RX 2299 at 2; *see* J. Kelly, Tr. 2155-70 (EIA never received a response from Echelon as to how its patent related to the standard under development; CEA "could see no relevance whatsoever between the patent" and its standard-setting work); RX 2300.

Additionally, Rambus claims that JEDEC itself has adopted standards without seeking RAND assurances. Rambus cites only brief notations in JEDEC minutes, indicating that JEDEC approved ballots on which patent issues had been raised. The minutes – generally just one- or two-word notations – do not explain how the patent issues were resolved. They do not establish that the suspected patents actually existed, much less that they applied to the standards. Nor do the minutes indicate whether the patentee ever intended to enforce the patents against JEDEC-compliant products. The minutes do not even state that RAND assurances were not, in fact, offered. *See* JX 15 at 5-6, 8-9,14; JX 25 at 10. Rambus elicited no testimony to clarify these issues.

[543] Rambus nonetheless asserts that any incentive for the DRAM manufacturers to negotiate royalties *ex ante* would have been "very weak" because, under JEDEC's requirement of "non-discriminatory" terms, all DRAM manufacturers would have been affected uniformly. RB at 71-72. Rambus's sole record support is testimony from its economic expert, David Teece. *Id.* Teece, however, did not deny that DRAM manufacturers possessed incentives to negotiate *ex ante*. Rather, he characterized what he viewed as the practical difficulties of such

specific outcome might have been, the consequences of incorporating Rambus's patented technologies into the standards would have been identified and weighed *before* the standards were adopted, *when Rambus's technologies were competing with the alternatives.* That "but for world" would have been more competitive than the current DRAM marketplace, in which Rambus has monopoly power and can charge whatever royalties it chooses.

d. Rambus's "No Lock-In" Claim

Rambus claims that, even if it did acquire any monopoly power by virtue of the incorporation of the four key patented Rambus technologies into the JEDEC standards, this monopoly power was not enduring because industry participants who practiced the standards were not "locked in." In effect, Rambus claims that there were no barriers to entry to rivals wishing to challenge its monopoly position.[544] The ALJ agreed with this argument, concluding

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negotiations as counter-incentives. *See* Teece, Tr. 10349, 10352-54 (stating that "firms have got incentives to do lots of things that they don't do"), 10360 ("because of these costs and difficulties, you're incented not to incur those costs

that Complaint Counsel had failed to establish that the DRAM industry had become locked into the JEDEC standards.[545]

Our analysis necessarily is anchored by timing. Lock-in must be assessed as of the time that JEDEC members gained sufficient information to know that Rambus had relevant patents and could have taken responsive action. JEDEC members lacked knowledge of Rambus's patent position until Rambus filed its first infringement suit against a producer of JEDEC-compliant DRAMs in early 2000. After that, it took some time for the information to be disseminated and evaluated. Each JEDEC member individually needed to explore alternatives – such as licensing and possible design changes – and to determine how it preferred to proceed. At that point, the JEDEC members could begin in earnest to try to agree on a revised standard.[546]

If the DRAM industry had become locked into Rambus's technology by the time that industry participants were apprised of, and able to take action in response to, Rambus's enforcement efforts, Rambus would have achieved durable monopoly power. If, however, the industry still had the practical ability to avoid Rambus's patents by switching to alternative technologies, Rambus would not have obtained durable monopoly power.[547]

We find that the DRAM industry was locked into the SDRAM and DDR SDRAM standards by 2000, by which time the JEDEC members were, in theory, in a position to take actions to avoid Rambus's patents. The record does not, however, establish a sufficient causal link between Rambus's exclusionary conduct and JEDEC's adoption of DDR2 SDRAM.

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[545] ID at 326-29.

[546] *See, e.g.*, CX 1855 (January 2000 Rambus complaint alleging that Hitachi's SDRAM and DDR SDRAM products infringed four Rambus patents but not identifying the specific claims or technologies at issue). Rambus revealed the nature of its claims to additional JEDEC members during the second quarter of 2000. CX 1109 at 1; CX 1127; CX 1129; CX 1371; CX 2559 at 3; Crisp, Tr. 3435-36. Some JEDEC members quickly recognized the implications of Rambus's patent enforcement efforts. *See, e.g.*, Rhoden, Tr. 532-33; CX 2459 at 1 (indicating that initial work-around proposals regarding programmable CAS latency were presented in March 2000). Other JEDEC members needed additional time before they gained a detailed understanding of Rambus's claims. *See* Krashinsky, Tr. 2782 (stating that he learned that Rambus claimed a patent on programmable CAS latency "midyear or so" in 2000); Polzin, Tr. 3987 (stating that he learned that Rambus claimed patents on technologies used by AMD in "late summer 2000 " and that he conducted an analysis of the Rambus patents at that time). Discussions of possible ways to avoid Rambus's patents on dual-edge clocking for purposes of DDR2 SDRAM began in a JEDEC task group in late October 2000 and reached the JC 42.3 Committee in December 2000. Krashinsky, Tr. 2827-28; Lee, Tr. 6800-02; CX 426; JX 52 at 45-50.

[547] This issue also is one of causation. We could find that Rambus's deceptive course of conduct caused the ensuing anticompetitive effects because JEDEC members had become locked in before they could take effective countermeasures, and thus were unable to avoid Rambus's royalties. If, on the other hand, JEDEC members had obtained the necessary knowledge of Rambus's patent position at a time when they still were economically capable of switching technologies – but deliberately chose not to switch – the chain of causation would have been broken, and Rambus's monopoly power would not be attributable to its deceptive course of conduct.

SDRAM. The SDRAM standard was first published by JEDEC in 1993. Rambus claims patent protection over technology from the latency and burst length product markets that was incorporated into the standard.

Complaint Counsel's economic expert, McAfee, described lock-in as "something that grows over time. It's certainly been accomplished by the time that ramp-up starts."[548] McAfee reasoned that before the time DRAM production ramps up, most of the sunk investments in complementary goods must have been made, because "in order to deploy the standardized [DRAM] product in volume, it requires those complementary goods."[549] The progressive accumulation of switching costs gradually contributes to lock-in,[550] and most of the switching costs for both DRAM manufacturers and producers of complements accrue by the time DRAM production ramps up.[551]

Manufacturers ramped up SDRAM production around 1996.[552] SDRAM represented 78.4 percent of DRAM revenues by 2000.[553] DRAM manufacturers, component manufacturers, and systems OEMs testified that changing SDRAM to work around Rambus's patents in 2000 would have presented significant financial and technical difficulties.[554] For example, a witness

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[548] McAfee, Tr. 7444-45. McAfee defined ramp-up as the time "when the volume [of DRAM production] starts to dramatically increase." *Id*. at 7445.

[549] McAfee, Tr. 7445-46 ("they're not going to produce the DRAM for inventory in any large volumes and just sit on them hoping that the complementary goods would be provided in the future").

[550] Switching costs accumulate for manufacturers of DRAMs and of compatible, complementary components as they move from the standard-setting process, to designing chips and products that conform to the standard; testing and verifying those designs; building, testing, and qualifying prototypes; and ramping up production on a commercial scale. At each stage the manufacturers make sunk investments that have to be repeated in order to switch to an alternate design. *See* McAfee, Tr. 7444, 7453-54; Shirley, Tr. 4152-54.

[551] *See* Peisl, Tr. 4452-53 (a change to SDRAM that would have been "relatively easy" in 1992 would have been "near impossible" in 2000).

[552] McAfee, Tr. 7442 (ramp-up for SDRAM was "roughly 1995 or 1996"); *id*. at 7446 ("[T]he volume production start[ed] in the 1996-1997 time frame. And so that corresponds to the ramp-up."). SDRAM accounted for less than 2.9% of DRAM revenue in 1995, 4.3% in 1996, and 33.5% in 1997. Rapp, Tr. 10248. Revenues, of course, lag behind production. *See also* Rambus Inc.'s Response to Complaint Counsel's Proposed Findings of Fact, No. 577 (Oct. 1, 2003) ("Although SDRAM represented a relatively small percentage of the DRAM market in 1996, it was certainly 'volume' production.").

[553] Rapp, Tr. 10100-01.

[554] Witnesses from Infineon and Micron, respectively, stated that by 2000 the level of SDRAM development and implementation made substantial changes "very costly and . . . near impossible," Peisl, Tr. 4443-44, and "virtually impossible," Appleton, Tr. 6399. CPU manufacturer AMD stated that changing SDRAM to work around Rambus patents in 2000 would have introduced "a whole host of problems" and would have been "a major, major concern for AMD." Heye, Tr. 3731-34. Cisco Systems explained that changes to memory in 2000 would

from HP testified that by the time he learned of Rambus's patent claims in 2000, changing SDRAM to avoid Rambus's patent enforcement efforts would have been "[w]ay too expensive" for HP, whose SDRAM-based server

> was already out, qualified and you know, we sold to customers and you cannot change something like this after it was designed and already shipped, and if you do change it, you're talking about millions and millions of dollars in expenses. It wasn't even going to be considered.[555]

Similarly, an IBM e-mail from April 2000 states, "we have gone way too far with SDR [SDRAM] to even consider talking about" switching to fixed latency.[556] Redesigning programmable burst length at that time would have presented similar difficulties.[557]

The issue of timing was particularly critical in the DRAM market: the time it would take to redesign SDRAMs and their complements to avoid Rambus's claimed patents would have been prohibitive. Rambus's engineering expert, Geilhufe, indicated that the changes could have been implemented in six to eighteen months.[558] Most of the previous design projects cited in the

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have imposed "tremendous cost to Cisco to redesign the existing boards and systems Cisco was shipping." Bechtelsheim, Tr. 5881-82. Graphics processor/chipset designer nVIDIA stated that changing SDRAM in 2000 would have put it through a "painful process" of changing its development plan and redesigning its products. Wagner, Tr. 3862-63.

[555] Krashinsky, Tr. 2782-83. According to the HP witness, providing multiple latencies without using programmable CAS latency would have required changes to the memory module, the motherboard, and the memory controller. *Id*. at 2784-87. He characterized changing programmable CAS latency "a major change," *id*. at 2788, although he indicated that significantly less change would have been required if a fixed CAS latency would have sufficed. *Id*. at 2804-05. Joe Macri of ATI Technologies (ATI) stated that graphics system designer ATI would have incurred "a huge burden" if JEDEC had changed to fixed latency. Macri, Tr. 4764-65 (*in camera*). *See also* Jacob, Tr. 5377-78, 5569 (use of multiple fixed latencies would have caused compatibility problems absent either greater user understanding as to which latency value was needed or development of a more sophisticated memory controller).

[556] RX 1626 at 3. When the possibility of changing the SDRAM standard regarding programmable CAS latency was discussed within JEDEC in March 2000, it was "very poorly received" because of lock-in concerns. *See* Rhoden, Tr. 533; Kellogg, Tr. 5196-200; RX 1626 at 2.

[557] *See* Peisl, Tr. 4450-53 (removing programmable burst length in 2000 would have been "nearly impossible," with a "huge impact" on DRAM customers). Using a burst terminate command to set burst length would have required "an enormous amount of redesign"; it may have required "almost a full redesign of the graphics pipeline" and at a minimum would have meant design modifications and a "big disruption of [ATI's] engineering plans." Macri, Tr. 4776-77 (*in camera*). *See also* Jacob, Tr. 5572-73 (switching to fixed burst length would introduce incompatibilities in some systems and would have design implications similar to those for switching to fixed CAS latency).

[558] *See* Geilhufe, Tr. 9615. *See also id*. at 9675 (stating that the changes could be accomplished in a six to twelve month time frame).

expert, Rapp, argued that $4.3 million is small in relation to the royalties that are being charged by Rambus.

many as three densities,[569] and would incur switching costs separately for each density.[570] The figure also ignores – as Rapp conceded – that manufacturers with multiple plants might incur some of these costs at each facility.[571] Moreover, Rapp agreed that each affected DRAM manufacturer separately would bear these switching costs and that, as of 1995, there were five to ten major DRAM manufacturers.[572] Multiplying Rambus's $4.3 million estimate – by the number of manufacturers, then by the average number of densities, and then by a figure reflective of the costs that would have to be duplicated in multiple plants – suggests that total costs to DRAM manufacturers could have reached hundreds of millions of dollars. Adjusting for understatements of cost elements would increase that total even more.

Most significantly, Rambus's $4.3 million figure focuses solely on DRAM manufacturers. If JEDEC changed SDRAM, OEMs and manufacturers of complementary components would face substantial switching costs in redesigning their own products.[573] Rambus's estimate omits these costs, although even Rapp conceded that the switching costs of component manufacturers could exceed those of DRAM manufacturers.[574] As a consequence, Rambus's estimate wholly disregards a major source of lock-in. For all of the foregoing reasons, we find Rambus's switching cost estimates to be flawed.

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[569] *See* Rapp, Tr. 10144.

[570] *See* Rapp, Tr. 10143-46 ("whatever the switching costs were . . . would be multiplied by the number of parts that they were starting off with").

[571] *See* Rapp, Tr. 10123. Many DRAM manufacturers own multiple manufacturing facilities. *See, e.g.*, Appleton, Tr. 6267-69 (Micron operates five fabrication facilities); CX 2466 at 2 (Infineon operates three manufacturing facilities).

[572] *See* Rapp, Tr. 10124 ("You could multiply this as needed by the number of manufacturers"), 10146. *See also* CX 2747 at 7 (Micron DRAM Update presenting market shares of 18 DRAM manufacturers in early 1999), 15 (showing 16 DRAM manufacturers remaining in September 1999); Gross, Tr. 2309 (8-10 was a "generous" estimate of DRAM manufacturers in 2003); Appleton, Tr. 6259, 6276-6277 (the DRAM industry had consolidated from approximately 20-25 DRAM manufacturers in the early 1980s to 5-6 major DRAM manufacturers and 2-3 smaller manufacturers as of 2003).

[573] Complementary components – such as memory controllers, memory modules, and motherboards – must be compatible with industry-standard DRAM. *See, e.g.*, Peisl, Tr. 4382, 4410, 4402-03; Macri, Tr. 4589 ("A DRAM alone doesn't really do anything. It needs to talk to other things . . . ."); Heye, Tr. 3655-65, 3715; Polzin, Tr. 3954; CX 1075 at 1. For example, changing programmable CAS latency in SDRAM would require HP to redesign and generate "a whole new chip" for its proprietary memory controller. Krashinsky, Tr. 2786. Designing around Rambus's patents may have required changes to the memory controller, the motherboard, the memory module, and the BIOS (basic input/output slllers, ory1 1 Tf0.en

Rambus also argues that the DRAM industry was not susceptible

standards were based.[578] More importantly, the types of changes cited by Rambus raised fewer compatibility issues and, therefore, fewer lock-in implications.[579]

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[578] *See, e.g.*, CX 2108 at 65-66 (deposition transcript at 257-58) (Oh FTC Dep.) (*in camera*) (describing additional design work required for changing circuitry as opposed to conducting a shrink); CX 2334 at 3 (April 1999 Hyundai presentation stating, "PC100 to PC133 – The Same Die as PC100"). An Infineon witness explained that changes in DRAM type t

We find that high direct switching costs, combined with significant delays from revising standards and reworking products, rendered infeasible a change in SDRAM to avoid Rambus's patented technologies in 2000 and conferred durable monopoly power with respect to SDRAM.

DDR SDRAM. JEDEC first published the DDR SDRAM standard in 1999. Rambus claims patent protection over technology incorporated into the standard relating to dual-edge clocking and on-chip PLL/DLL, in addition to the programmable CAS latency and burst length technologies that carried over from SDRAM.

The DRAM industry was significantly locked in to DDR SDRAM by 2000. DRAM manufacturers had beTmTj16.16 8tr56 TmTechn

Similarly, HP's Krashinsky testified that DDR SDRAM already had been installed in HP server prototypes by about the third quarter of 2000.[584] Cisco's Bechtelsheim stated that a change in DRAM design in response to Rambus's assertion of patents in 2000 would have imposed "a tremendous cost to Cisco to redesign the existing boards and systems Cisco was shipping to accommodate this new type of memory."[585]

The adoption of programmable CAS latency and burst length in the DDR SDRAM standard raises the same issues as in SDRAM. The cost and delay associated with changing these technologies in SDRAM were equally applicable to DDR SDRAM.[586] Indeed, JEDEC rejected a March 2000 proposal to move to fixed latency in DDR SDRAM, and lock-in concerns were a significant factor.[587]

The DDR SDRAM standard adopted two additional technologies that Rambus now claims to have patented: dual-edge clocking and on-chip PLL/DLL. As to dual-edge clocking, Complaint Counsel's engineering expert testified that redesigning DDR SDRAM to avoid Rambus's patents would have required changes to the clock chip and the memory controller.[588] Producers of complements and OEMs voiced lock-in concerns. For example, AMD's Polzin testified that, by the summer of 2000, the firm was in the middle of a production ramp for DDR-based controllers and motherboards, and "[i]t would have been impossible for us to stop and change" the dual-edge clocking mechanism.[589] Likewise, Krashinsky explained that HP did not seek a change in JEDEC's DDR SDRAM standard, even after learning of Rambus's patent claims on dual-edge clocking, because HP already had developed a server prototype dependent

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(June 2000 AMD e-mail stating, "AMD powered on the first K7 DDR chipset (IGD4) in Dec 99"). *But cf.* Heye, Tr. 3750 (noting that the infrastructure of DDR-based complements was still developing in 2000 and had not yet been established in the marketplace).

[584] Krashinsky, Tr. [illegible] DDR [illegible] p Hen 99estab

June 2000 and June 2001.[602] JEDEC published the DDR2 SDRAM standard to its members in 2002, but final revisions still were being completed in June 2003.[603]

DDR2-based product design and development was in its early stages by 2000. For example, Micron started design work on DDR2 SDRAMs in late 1999,[604] and its first DDR2 design was "taped out" (*i.e.*, ready for initial transfer to masks) in January 2002.[605] The head of JEDEC's Future DRAM Task Group characterized JEDEC deliberations as fluid until first reaching a "stable point" in June 2000.[606] An April 2000 e-mail by Hitachi's Bob Fusco stated, "For DDR-2, we have no legacy to live with, so I like the Micron proposal [to avoid programmable CAS latency]."[607] Complaint Counsel point out that some firms had begun work on DDR2-based products by 2000.[608] However, the scope and extent of DDR2-related efforts is unclear, particularly when one contrasts the unambiguous statements that work had progressed too far to permit change to the SDRAM and DDR SDRAM standards. The evidence suggests that there would have been DDR2 switching costs by 2000, but provides little sense of their magnitude.

Some component manufacturers had started work on DDR2-based complements by 2000. For example, initial JEDEC-level work on the attributes of DDR2-based memory modules began as early as February 1999.[609] However, IBM's Bill Hovis wrote in April 2000 e-mail that, as to DDR2 SDRAM, "[o]bviously here, the situation with the system is that I am not currently locked in . . . ."[610] nVIDIA started work on the first product that it thought might prove DDR2-

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[602] *See* Macri, Tr. 4598-99 ("during June of 2000 to June of 2001, we were adding the meat, you know, the real description that an engineer would need to truly understand these – these concepts").

[603] *See* Rhoden, Tr. 411-12; Polzin, Tr. 4046.

[604] Shirley, Tr. 4211 (*in camera*). IBM's Gordon Kelley explained that design work may begin on aspects of the DRAM that are not covered by JEDEC standards. G. Kelley, Tr. 2590.

[605] Shirley, Tr. 4228 (*in camera*).

[606] Macri, Tr. 4598.

[607] RX 1626 at 4.

[608] *See, e.g.*, Macri, Tr. 4648 (by September 2000 "there were already companies in design on both the DRAM and the systems side"), 4649 (changes at this time would have affected "earliest adopters"), 4650-51; Kellogg, Tr. 5201 (in September 2000 IBM was "moving down the path" of designing its first DDR2-based memory controllers), 5204 (eliminating dual-edge clocking likely would mean "measurable schedule delay" for IBM's memory controller project).

[609] *See* Kellogg, Tr. 5194-95; CX 393.

[610] RX 1626 at 3. The e-mail addressed only issues regarding CAS latency. *Id.* at 3-4.

compatible in late 2000 or early 2001.[611] AMD's Polzin stated that, as of the time of his June 2003 testimony, AMD still had not started to develop an infrastructure for DDR2 SDRAM.[612]

Complaint Counsel stress the industry's desire to maintain backward compatibility. Several industry witnesses expressed concerns that changing DDR2 SDRAM to avoid Rambus's patents would have disrupted backward compatibility.[613] One witness testified that an effort to maintain backward compatibility after eliminating dual-edge clocking would have had "a big impact" from the perspective of design and that a desire to maintain backward compatibility was the reason that a sub-unit of JEDEC's task group in October 2000 chose to maintain dual-edge clocking.[614] Contemporaneous documents confirm that backward compatibility was a general goal, but do not conclusively establish that the decisions to retain Rambus's patented technology resulted from that factor.[615] One such example is the minutes of an October 2000 conference call among members of a sub-unit of JEDEC's Future DRAM Task Group, in which elimination of dual-edge clocking was discussed. The minutes conclude, "Single data rate clock is preferred provided that we can make it work."[616] Although "mak[ing] it work" might have encompassed considerations of backward compatibility, the minutes do not expressly state this. Follow-on testimony from the proponent of the change indicated that ultimately "there was not a lot of

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[611] Wagner, Tr. 3866-67.

[612] Polzin, Tr. 4043-44.

[613] *See, e.g.*, Macri, Tr. 4678 (changing to fixed latency would have been a disruptive departure from DDR SDRAM base), 4624 (on-chip DLL retained "to keep the backwards compatibility"), 4647-48 (similar), 4649 (Macri did not propose eliminating dual-edge clocking because of backward compatibility concerns), 4678-79 (JEDEC task group thought eliminating dual-edge clocking would have been "disruptive"); Kellogg, Tr. 5192-93 (describing consensus desire in 1998 to achieve an "evolutionary solution" that would sustain backward compatibility); Lee, Tr. 6805-06 (very difficult to design a controller that would be compatible with both dual-edge and single-edge clocking).

[614] *See* Macri, Tr. 4640-42, 4780-81 (*in camera*); *cf.* Krashinsky, Tr. 2829 (JEDEC task group rejected alternative to dual-edged clocking because of "the cost that it would be to implement one versus the other" and because the change in clocking rate would have been too "revolutionary").

[615] These documents show that the Future DRAM Task Group decided early on that the next generation of DRAM should "stay backward compatible if at all possible with DDR," CX 392 at 3, and reflect the desire to provide a "migration path" for producers of controllers, CX 379a at 9. The references, however, are too general to reveal how much those considerations shaped the group's specific technology choices. *See also* CX 132 at 4, CX 379a at 9, and CX 2745 at 7 (all indicating that DDR2 SDRAM should be based on DDR SDRAM); CX 2717 at 8, 13 (r(ga9Tdj2.96 0pTd(tion pTj3i 4d93.92 0 Td GrouptTd(se 3()Tj22 >rp7 Td(pro)Tj1.493 0 Td" for4)Tj1.62ap's0267 Tw 1.54r urgi

support," but did not explain the underlying reasons why dual-edge clocking was retained.[617] Based on the existing record, it is difficult to assess how substantially backward compatibility concerns contributed to lock-in in 2000.

In summary, there certainly is evidence that eliminating Rambus's patented technologies from the DDR2 SDRAM standard would have entailed some switching costs for some stakeholders, including, but not limited to, switching costs associated with the desire to preserve backward compatibility.[618] However, the record shows that JEDEC published the DDR2 SDRAM standard in 2002. The causal link between Rambus's course of conduct and the incorporation of its patente

We conclude that the record does not establish a causal link between Rambus's exclusionary conduct and JEDEC's adoption of DDR2 SDRAM.[621]

4. Rambus's Claim that its Acquisition of Monopoly Power Did Not Matter

Finally, Rambus claims that even if its course of conduct enabled it to acquire monopoly power, it cannot be held liable because Compla

not reasonable.[624] Ultimately, however, we need not rest on this evidence. Deceptive conduct that confers durable market power by its very essence harms competition, and claims that the offender has not yet behaved like a monopolist provide no shelter.[625] We therefore reject this argument as a matter of law.

V. <u>SPOLIATION</u>

Allegations that Rambus engaged in the spoliation of evidence have permeated these proceedings, as well as several private actions relating to Rambus's patent enforcement efforts.[626]

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[624] A comparison of Rambus royalty rates for DDR SDRAM and RDRAM strongly suggests that Rambus's DDR royalties have not been reasonable. Rambus has charged at least a 3.5% royalty on DDR SDRAM, *see, e.g.*, Rapp, Tr. 9853; CX 1680 at 4 (*in camera*), but generally has negotiated royalties between 1.0% and 2.0% for RDRAM. *See, e.g.*, CX 1592 at 21-23 (Samsung RDRAM License); CX 1646 at 10-11 (Micron RDRAM License); RX 538 at 20-22 (NEC RDRAM License); CX 1612 at 4-5 (Hyundai RDRAM License); CX 547 at 12; CX 1057. (RDRAM royalties cover all four of the technologies at issue in this proceeding, as well as additional proprietary technologies. *See, e.g.*, Horowitz, Tr. 8547-48*;* RX 2183; RX 81 at 8.) Thus, Rambus's 3.5% royalty for DDR SDRAM far exceeds the royalties that were negotiated for RDRAM in a setting in which licensees were aware of Rambus's patent position from the start and, consequently, were sheltered from hold-up.

Rambus attempts to establish the reasonableness of its royalties by comparing them to royalty rates charged for *other* technologies. *See* RB at 73; Teece, Tr. 10422-51. Rambus CEO Tate, however, testified that comparing royalty rates for different technology licenses mixes "apples and oranges" because "[t]he royalty rate for one patent and the royalty rate for another patent, even in the [semiconductor] industry, can vary tremendously based on the value of the patent and the applications involved."

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Many of the basic facts are not in dispute.[627] Rambus began formulating its document retention policy in early 1998 with the assistance of outside counsel,[628] and adopted a document retention policy in July 1998.[629] Rambus then conducted company-wide "shred days" in September 1998 and August 1999 that involved the destruction of significant quantities of documents.[630] Rambus destroyed a similarly large volume of documents in December 2000 when it moved to a new office building.[631] As part of its document destruction efforts, Rambus deleted e-mails,[632] erased computer backup tapes,[633] and instructed its outside patent counsel, Lester Vincent, to clean out his law firm's patent prosecution files so that they mirrored the PTO's file.[634]

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[627] Our discussion draws upon evidence developed in the *Infineon* litigation, pertaining to the nature and

The record shows that key Rambus executives and lawyers – including Richard Crisp,[635] Joel Karp,[636] Billy Garrett,[637] Anthony Diepenbrock,[638] and Lester Vincent[639] – destroyed documents. The record also shows that some of these documents related to subject matter pertinent to this proceeding, such as documents regarding Rambus's participation in JEDEC,[640] and Rambus's patent prosecution files.[641] Indeed, Rambus's document destruction efforts were so thorough and effective that neither Crisp nor Rambus's attorneys were able to find certain JEDEC-related documents when they subsequently searched for them.[642]

In order to establish pre-litigation spoliation, Complaint Counsel must show that Rambus destroyed potentially relevant documents at a time when litigation was reasonably foreseeable.[643] The destruction must have occurred with a culpable state of mind.[644] The appropriate remedy in

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[635] *See* Crisp, Tr. 3425, 3427-30; CX 2082 at 157-59 (deposition transcript at 841-43) (Crisp *Infineon* Dep.) *(in camera)* ("anything that I had on paper, I basically threw away"); CX 5059 (d1.96 Td(I Raoy07 0 Td((6 0 T)Tj22.037a4u Td(4
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any particular case typically will vary, depending on the spoliating party's degree of fault as well as the extent to which the other party is prejudiced.[645]

In the present case, we need not resolve whether Rambus engaged in spoliation because the record shows, by a preponderance of the evidence, that Rambus engaged in exclusionary conduct. Our findings stand firmly on the evidence that has survived. No remedy for the alleged spoliation is necessary, and we therefore do not undertake the inquiry required to resolve the spoliation issue.[646]

We stress, however, that Rambus's extensive document destruction campaign had the potential to deny the Commission an opportunity to examine thoroughly Rambus's conduct. In some instances, the Commission has relied on evidence that was preserved only fortuitously.[647] If the record in this case had been marginal, while simultaneously containing evidence that Rambus had destroyed potentially relevant documents, we would have pursued the spoliation inquiry to its conclusion and, if appropriate, imposed a remedy. The Commission has a broad range of remedies available to address spoliation, ranging from drawing adverse inferences to ordering that a proceeding be decided against the spoliating party. If spoliation were proven in a future case, the Commission would not hesitate to impose warranted sanctions, in keeping with its fundamental interest in preserving the integrity of its administrative proceedings.

VI. CONCLUSION

We find that Rambus engaged in exclusionary conduct that significantly contributed to its acquisition of monopoly power in four related markets. By hiding the potential that Rambus would be able to impose royalty obligations of its own choosing, and by silently using JEDEC to assemble a patent portfolio to cover the SDRAM and DDR SDRAM standards, Rambus's conduct significantly contributed to JEDEC's choice of Rambus's technologies for incorporation in the JEDEC DRAM standards and to JEDEC's failure to secure assurances regarding future

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[645] *See* Residential Funding Corp. v. DeGeorge Financial Corp., 306 F.3d 99, 107 (2d Cir. 2002); Schmid v. Milwaukee Electric Tool Corp., 13 F.3d

royalty rates – which, in turn, significantly contributed to Rambus's acquisition of monopoly power.

Rambus claims that the superiority of its patented technologies was responsible for their inclusion in JEDEC's DRAM standards. These claims are not established by the record. Nor does the record support Rambus's argument that, even after two JEDEC standards were adopted and substantial switching costs had accrued, JEDEC and its participants were not locked into the standards. Rambus now claims that we can and should blind ourselves to the link between its conduct and JEDEC's adoption of the SDRAM and DDR SDRAM standards, as well as to the link between JEDEC's standard-setting process and Rambus's acquisition of monopoly power. These claims fail, both as a matter of fact and as a matter of law. To hold otherwise would be to allow Rambus to exercise monopoly power gained through exclusionary conduct. We cannot abide that result, given the substantial competitive harm that Rambus's course of deceptive conduct has inflicted.

VII. REMEDY

Complaint Counsel seek an order preventing Rambus from enforcing, against JEDEC-compliant products, (1) any patents that claim priority based on applications filed before Rambus withdrew from JEDEC and (2) any existing licensing agreements.[648] Rambus argues that the Commission lacks authority to impose such a remedy and that the royalty rates set by its existing licenses already satisfy all remedial concerns.[649]

Both parties' arguments regarding remedy have been scant and, for the most part, reflective of opposing extremes.[650] Now that the Commission has found, and determined the scope of, liability, the Commission believes it would exercise its broad remedial powers most responsibly after additional briefing and, if necessary, oral argument devoted specifically to remedial issues.

The accompanying order establishes a briefing schedule. The parties' written presentations directed by the accompanying order will be confined to remedy; re-argument of issues of liability will not be permitted in those presentations. The Commission is most interested in the parties' views regarding possibilities for establishing reasonable royalty rates for JEDEC-compliant products affected by Rambus's exclusionary conduct. The parties should

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[648] CCAB at Attachment 2; CCRB at 95-100.

[649] RB at 128-33.

[650] *See generally* United States v. National Lead Co., 332 U.S. 319 (1947) (rejecting the imposition of compulsory, royalty-free licenses when they were not "necessary in order to enforce effectively the Anti-Trust Act," and finding that "licenses at uniform, reasonable royalties" would be sufficient to accomplish the discontinuance and prevention of the illegal restraints). For discussion of Rambus's existing royalty rates, *see supra* Section IV.C.4. e not "nV.3 0 Td(pu

address, without limitation: (1) means for the Commission to determine, based on the existing record, reasonable royalty rates for licensing all technologies applicable to JEDEC-compliant products and covered by relevant Rambus patents; (2) alternative mechanisms and procnd ceCp sVER 6j-13tedu